TABLE OF CONTENTS
Proceedings of RF Technology Expo 86
January 30 - February 1, 1986

Interactive Computer Aided Graphics Applied to RF Circuit Design
Alan Victor, Motorola Inc..... 1

New Hybrid Power Amplifier Modules Speed RF Systems Design
Eric A. Ulrich, Microwave Modules & Devices..... 11

Design Considerations for a 1 kW L-Band Radar Module
Orville B. Pearce, Microwave Modules & Devices..... 19

The Basics of RF Power Amplifier Design
Dan Peters, Falcon Communications..... 33

An Evolution of Optimization and Synthesis Programs for Personal Computers
Stephen E. Sussman-Fort, Ph.D., SPEFCO Software..... 49

"The Poor Man's Engineering Work Station" or "Cheap CAD"
Richard E. Kolbly, PE, Lockheed California..... 61

SAW Accelerometers: Integration of Thick and Thin Film Technologies
Tim B. Bonbrake, Magnavox and Carl A. Erikson, Anderson Labs..... 81

Improve Synthesized Transceiver Performance and Reliability by Simple Screening of the VCO Active Device
Jaime A. Borras, Motorola, Inc..... 87

A CAD Design Program for Analysis of Electro-Thermal Coupling in High Power RF Bipolar Transistors
Antonio Morawski and Boris Hikin, TRW Electronic Components..... 97

Microwave Integrated Receiver for the Morelos Mexican Satellite System
A. Serrano, J. L. Medina, D. Hiriart, CICESE Research Center.....113

High Efficiency Power Amplification with Optimally Loaded Harmonic Waveshaping
William McCalpin, Microwave Modules & Devices.....119

Modulation Techniques for Biotelemetry
Robert W. Vreeland, University of California.....127

Wide-Band High-Dynamic-Range Front-End Circuitry for AM Radio
E. H. Nordholt, H. C. Nauta, Delft University of Technology.....133

The Schottky Diode Mixer
Jack H. Lepoff, Hewlett-Packard.....139

Design of Coaxial High-Pass Filters Having Various Transfer Properties
Dick Wainwright, Cir-Q-Tel, Inc.....149

High Power Filters
Dick Wainwright, Cir-Q-Tel, Inc.....157

An IF Limiting Amplifier Design on "K" Soft Board
Steve Chambers, Acrian.....167

Design of Combline and Interdigital Bandpass Filters
Dick Wainwright, Cir-Q-Tel.....173

The PIN Diode -- Uses and Limitations
Jack H. Lepoff, Hewlett-Packard.....187

RF and Microwave Transistor Bias Considerations
Gary Franklin, Hewlett-Packard.....197

Practical Wideband RF Power Transformers, Combiners, and Splitters
Roderick K. Blocksome, Rockwell International.....207

High Power UHF Pulsed Push-Pull Amplifier Design
Joseph J. D'Agostino, Jr.....229

A 350 MHz Dual-Gate GaAs FET Frequency Multiplier
Gordon A. Olsen, Rockwell International.....239

Aiding Computer-Aided Design -- Curve Fitting With Any Number of Variables
Albert Pergande, Martin Marietta Aerospace.....245

Oscillator Design Using the Device Line Method and Load Pull Method
Gary Franklin, Hewlett-Packard.....251

Packaging Considerations for RF Transistors
Norman E. Dye, Motorola Inc.....261

Microstrip Miniture Transfer Switch
Dr. Rajeswari Chattopadhyay, Eswarappa, P. K. Atrey, Indian Telephone Industries, Ltd.....269

Mathematics of the Linvill Stability Criteria
Robert Gunderson, Hughes Aircraft Co.....273

Basic MODAMP^{tm} MMIC Circuit Techniques
William Mueller, Avantec Inc.....287

Design of Dielectrically Stabilized Oscillators Using Feedback Techniques
R. Partha, M. L. Sharma, Indian Telephone Industries, Ltd.....291

Iron Powder Cores for High Q Inductors
Jim Cox, Micrometals, Inc.....297

140 MHz Lumped Element 3dB Hybrid
Dr. Rajeswari Chattopadhyay, I. K. L. N. Murthy, Suresh K. R. Nayar, Indian Telephone Industries Ltd.....305

A Commutation Double-Balanced Mixer of High Dymanic Range
Edwin S. Oxner, Siliconix Inc.....309

Maximizing Crystal Oscillator Frequency Stability
Brian E. Rose, Q-Tech Corp.....325

Dielectric Resonator Filters for UHF and Microwave Applications
Dr. Marian L. Majewski, Royal Melbourne Institute of Technology.....335

Understanding RF Transistor Data Sheet Parameters
Norman E. Dye, Motorola Inc.....347

PIN Diode Attenuators and Vector Modulators at Intermediate Frequencies
N. R. W. Long, University College, London.....355

High Voltage HF/VHF Power Static Induction Transistor Amplifiers
Scott J. Butler and Robert J. Regan, GTE Laboratories.....365

An Evolution into SAW Resonators (Low Power Security -- FCC Part 15)
Ronald J. Coash, Notifier Co.....369

A Tracking Impedance Measurement System for Control of Tunable Networks
Virgil L. Newhouse, Rockwell International.....375

Choosing the Right Crystal and Oscillator for the Application
Brian E. Rose, Q-Tech Corp.....391

The Use of a Computer Model to Determine the Complex Parametric Relationships of a Crystal Oscillator Circuit
Gregory L. Weaver, Piezo Crystal Co.....399

Harmonic Filtering at UHF and Microwave Frequencies
Philip B. Snow, Tektronix Inc.....411

RF Technology for NMR
O. Mueller, D. Vatis, W. Edelstein, P. Bottomley, General Electric Co....419

The Q Factor of Microstrip Matching Network in RF Class C Amplifier Design
P. Gonord, S. Kan, J. P. Ruaud, Institut d'Electronique Fondamentale, Universite Paris - Sud.....433

SORF -- An RF Low Power SMD Alternative Package
Harry J. Swanson, Motorola Inc.....439

Unequal Power Split Hybrid Coupler
S. Pal, S. K. Saini, V. S. Rao, A. Bhaskaranarayana, ISRO Satellite Centre.....447

Spherical Dielectric Antenna
S. Pal, ISRO Satellite Centre.....451

Average Efficiency of Power Amplifiers
Frederick H. Raab, Ph.D., Green Mountain Radio Research Co.....473

A 405 MHz Phased Array Antenna for Atmospheric Wind Measurement
Daniel C. Law, NOAA Wave Propagation Lab.....487

Practical Considerations for Modulating or Pulling the Frequency of a Quartz Crystal Oscillator
John B. Fisher, Standard Crystal Corp.....491

S-Band Butler Matrix Feed Network
V. K. Lakshmeesha, Arvind Agarwal, L. Nicholas, S. Pal, ISRO Satellite Centre.....497

P.C. Mountable Miniature Helical Filter
V. K. Lakshmeesha, G. S. Seetha Raman, S. Pal, ISRO Satellite Centre.....503

S-Band High Performance Combline Filter
V. K. Lakshmeesha, U. Prabhakaran, S. Pal, ISRO Satellite Centre.....507

Noise Measurement Instrumentation
George Peter, Cornell University.....511

Temperature Compensation Circuit for Space Data Transmitters
S. Pal, V. S. Rao, N. U. M. Rao, B. Pichaiah, S. K. Saini, A. Bhaskaranarayana, ISRO Satellite Centre.....525

Testing of Narrowband Communications Receivers -- ACSB and SSB
Malcolm Levy, Racal-Dana Instruments, Inc.....533

Simple Approaches to Limiting Radiation From Foil-Shielded Computer Cables
Howard C. Rivenburg and John Juba, Jr., Atlantic Research Corp.....543

New Insights into "Old" Network Analysis Techniques
Lorenzo Freschet, Hewlett-Packard.....567

A Broadband Lumped Element Variable Attenuator
Dr. Rajeswari Chattopadhyay, I. K. L. N. Murthy, Eswarappa, Indian Telephone Industries Ltd.....573

Application Notes for Doubly Rotated Quartz Crystals
Lynn C. Heishman, Piezo Crystal Co.....575

RF Plastic Package Comparison Study
Kamil Gresko, Motorola, Inc.....577

Reliable Obstructed Path Coverage Determination
Bruce V. Ziemienski.....599

Spectral Shaping of Radio Frequency Waves
Jerry J. Norton.....609

Broadband HF Antenna Testing
David L. Faust and Moray B. King, Eyring Research Institute.....625

How To Build Simple and Not-So-Simple Test Equipment In Your Own Lab
Jim Weir, Radio Systems Technology.....633

Distributed 2-20 GHz Monolithic GaAs FET Amplifier Design
Gary G. Hawisher, EEsof, Inc. and Tim Aust, Hughes Aircraft.....643

RF TECHNOLOGY EXPO 86
INTERACTIVE COMPUTER AIDED GRAPHICS APPLIED TO RF CIRCUIT DESIGN

ALAN VICTOR

Introduction

This paper presents several programs which utilize the interactive graphics capability of a desk top computer to aid the RF circuit design engineer. High frequency amplifier design of class A power amplifiers, low noise design and stability analysis are discussed. Computer aided graphics is demonstrated which assist the designer in the appropriate tradeoffs. An interactive routine which handles the communications receiver cascade of noise and distortion is presented along with a "what-if-scenario" applied to a typical receiver system. Finally, a program which computerizes the Smith Chart and provides aid in broadband impedance matching is demonstrated.

The routines were developed on the Hewlett-Packard series 200 personal computer which features an excellent graphics oriented BASIC language and the capability of interactive control of program variables while the program is operating. These features are not necessarily limited to the series 200 computers of HP. In fact many of todays personal computers have excellent high resolution graphics and various forms of interactive control (i.e. light pens, paddles, joystick control and live keyboard). The routines to be discussed will concentrate on the following specific areas:

1. Class A power amplifier design
2. Small signal amplifier stability
3. Noise figure/ gain/ and VSWR optimization of amplifiers
4. Smith Chart and interactive graphics aid in broadband matching
5. Noise figure/ gain/ distortion of linear cascaded networks. Interaction aids in the optimization of a given cascade.

Class A Power Amplifier Design

Numerous occasions arise for the need of a small signal linear power amplifier. Normally the design criteria if the device is uncondltionally stable is to provide for simultaneous conjugate match at the input and output. If low noise performance is desired than the designer seeks to find the optimum source reflection coefficient and then conjugate match the output and maximize the amplifier transducer gain. At the same time the designer strives to minimize the input VSWR [1]. We will discuss these criteria in more detail; but for now the main interest is to provide maximum output power to the load while operating the device Class A. A good design approach to this problem was presented by Richter and

and again by D. Rosenzrin and M. Chorev [2], [3]. Their technique is based on choosing the optimum load conductance for a device operating class A at a given collector voltage and collector current. If the device is not to limit on voltage swing or peak output current then the optimum load conductance is given by

$$Glopt = Icq(ma.)/Vcc(volts).$$

If the load conductance is less than the Glopt then the maximum class A output power is given by

$$Pl(max) = (Vcc^2/2)\ Gl \quad \text{(current limited)}$$

and if the load conductance is greater then Gopt then

$$Pl(max) = (Icc^2/2\ Gl) \quad \text{(voltage limited).}$$

Power loci are plotted graphically on the Smith chart as constant conductance contours. The center center and radius as measured from the center of the unit circle chart are given by

$$r = Gln/(1+Gln) \quad \text{and} \quad \rho = 1/(1+Gln)$$

where Gin is the normalized load conductance. At the voltage and current specified the device S-parameters are measured. Given the S-parameters, constant output gain contours are calculated and also plotted on the Smith Chart as circular loci [1]. With the plot of power gain circles and power output circles displayed together it is now possible to visually see the trade-off between maximizing the power output and power gain. It is not uncommon to lose several dB of power output by simultaneously conjugate matching the device. Instead, maximizing the power output may only result in a few tenths of a dB loss in power gain. In [2] the authors show that the location of the optimum output load reflection coefficient is a susceptance contour on the unit circle Smith chart. This contour is the locus of tangency of optimum power output and all the respective gain contours and is shown in Figure (1).

With all this information shown graphically it is now possible to tune the load reflection coefficient and observe the tradeoff in power output, power gain, and potential input and output VSWR. This is achieved in the computer program by allowing the forced load reflection coefficient (* L) to be "tuned" interactively and observing

the location of the required source reflection coefficient conjugate matched input (* S). At the same time the actual load reflection coefficient (* L) for conjugate matched input is displayed thus allowing the designer to minimize the output VSWR. Figures (2) and (3) demonstrate that if the device were conjugate matched the output power would be reduced by 4.8 db from the maximum. On the other hand maximizing the power output only reduces the power gain by 1.1 db, clearly a good tradeoff!

Small Signal Amplifier Stability

The load and source reflection coefficient must be carefully chosen if the device is conditionally stable. Inspection of the Linvill stability factor C, [4] or the Rollet stability factor K, [5] aid in determining the probability of oscillation. Both the Linvill and Rollet stability factors are obtained from the measured Y parameters or S parameters respectfully. In addition to checking the value of C which must be less then 1 to ensure stability, the values of y11 and y22 must both be positive and real for all possible values of real source and load combinations. Using S parameters and the K factor a similar set of criteria exist. Many individuals look at the K factor alone and this is a necessary condition for stability but not sufficent [6]. The interactive graphics of the next routine demonstrate this vividly and Figures (4) through (6) show the results. In summary a good criterion for unconditional stability is given in [1,6] and repeated here for reference.

1. $K>1$ and $|\Delta| < 1$ where $|\Delta| = |s11*s22-s12*s21|$ or
2. $K>1$ and $B1 = 1 + |s11|^2 - |s22|^2 - |\Delta|^2 > 0$

The computer aided design routines presented here illustrate the stable regions of the Smith chart by circular regions. Depending on the location of these regions the inside of the circular regions may or may not provide a stable load or source reflection coefficient. Consider the previous figures (4,5,6). Interactive control of the load reflection coefficient (* L) allows you to position the load on either a constant VSWR circle or on a constant gain circle. As long as the forced load reflection coefficient remains inside the output stable region circle the source reflection coefficient (* S) and the actual load reflection coefficient (* L) remain positive and real. As the forced load reflection coefficient approaches the edge of the output stable region the source reflection coefficient approaches the edge of the unit circle

Smith chart. A movement of the load reflection around the outside of the stable circle will force the source reflection coefficient to trace out the complete outside edge of the Smith chart. Further movement of the load reflection coefficient outside of the stable region will force the source reflection coefficient to move outside the Smith Chart ($|\Gamma|>1$ implies negative real resistive component) and could produce amplifier instability. If the combination of forced load reflection coefficient and actual load reflection coefficient is still net positive and real then no oscillation will be present. On the other hand if this is not the case then both the input and output ports of the device are negative real and oscillation will occur. The interactive graphic nature of the program allows assessment of the amplifier stability as the load (or the source) reflection coefficient is varied.

Low Noise Amplifier Design

Device noise figure is a function of the source reflection coefficient. Minimization of noise figure and maximizing the amplifier gain is the desired design goal. Adler [7] defines a noise measure and Fukui [8] applies this concept or technique to aid in optimizing a low noise amplifier design. Interactive graphics provides another method for observing the tradeoffs involved. A plot of amplifier constant gain contours along with noise contours allows a visual tradeoff to be made [9].

Normally the approach taken is to seek the source reflection coefficient which minimizes the noise figure while maximizing the transistor transducer power gain. This results in minimizing the noise measure of the device. Unfortunately if the source reflection coefficient for minimum noise figure differs from the actual device input impedence then the input VSWR could suffer. One approach to this problem is to apply feedback around the device in an attempt to force the maximum device gain to coincide with the minimum noise figure point [10,11]. Another approach is to adjust the load reflection coefficent interactively and observe the source reflection coefficient movement. What we seek is a forced load reflection coefficient value which yields the maximum available gain and at the same time causes the source reflection coefficient to minimize the device noise figure. At the same time the actual load reflection coefficient should ideally be close to the forced load reflection coefficient in order to minimize the output VSWR. This approach has the benefit of minimizing the input VSWR and therefore preventing input mismatch loss from further degerading the system noise figure. Figures [7] and [8] illustrates the results for one device.

Computerizing the Smith Chart

The Smith chart is an indespensible graphical tool which solves a number of RF design related problems. The interactive graphics of a personal computer further enhances this tool and provides for additional insight into your design problem. A major application is in impedance matching, narrow band as well as broadband. A number of articles have addressed this application including computer oriented routines [12,13]. The routine demonstrated here provides the solution to the ladder matching network by solving the transmission matrix or chain matrix of each element in the ladder. The chain matrix of any of 12 different element types are included as subroutines. Both parallel and series forms of R,L,C, transmission lines,tuned circuits and ideal transformers are included. The benefits of interactive tuning are quite evident in this application, which allows the designer to literally tweak element values in the matching network with the Smith chart as the graphic background. Thus the designer can optimize VSWR and bandwidth. In addition the tune feature allows a feeling for element sensitivity as well as which components would lend themselves to optimization in matching say a broadband amplifier. As an example in applying this routine we demonstrate the impedance matching technique presented by Thomas [14,15] in his text. Figure [9] illustrates the Smith chart divided into 4 high Q regions. Depending on the region we wish to match to the center of the chart an appropriate network topology is selected. Figure [10] shows the tuning procedure as each element is "tweaked" and the final VSWR is reduced from 30:1 to less than 3:1.

The sensitivity of maintaining a low VSWR in a broadband match can also be investigated through interactive graphing and the Smith chart. The methodology for synthesizing in closed form optimum broadband matching networks is discussed in Chen's text and in Apel's work [16,17]. Figure [11] shows the results of applying [17] to the match of a GaAs FET and then varying one of the elements in the ladder match. The extent to which this element is changed before a VSWR of 2:1 or greater is exceeded becomes quickly apparent.

Interactive Computer Aided Graphics Applied to RF Circuit Design
RF Technology Expo 86

Noise Figure, Gain, and Distortion of Linear Cascaded Networks

Communication systems require the proper distribution of gain, noise, and linearity in order to provide the maximum dynamic range. This requires a proper tradeoff in each stage for noise figure, gain, and maximum signal handling ability before distortion sets in. One method for the characterization of a communucations receiver distortion is to use the intercept method [18]. This figure of merit coupled with a stage-by-stage description of noise figure, gain, and selectivity provides a complete description of the receiver performance [19,20]. A graphic presentation of each stage contribution to the total noise figure or distortion aids the designer in seeing which stage in the cascade is the most offensive. Then interactive tuning of each stage gain, noise figure or third order input intercept allows optimization as well as a sensitivity analysis of the receiving system dynamic range. Figure [12] shows a 9 stage cascade including RF amplifier, mixers and crystal filters. Figure [13] is a plot of the individual stage noise figure contribution and Figure [14] is a plot of intermodulation distortion contributions. At a glance the designer can see which stages are causing the distortion level to fall below a specified goal. By adjusting or tuning each stage an optimum gain, noise figure distribution will result. Any increase in gain, for example stage #, results in improved sensitivity but at the expense of degraded third order distortion due to larger input signal levels present at the earlier stages. A decrease in front-end gain in stage # lowers the third order distortion, but degrades the system noise figure and sensitivity. Thus, a lower system dynamic range occurs.

Conclusions

The RF design engineer will benefit from the use of todays personal computers, especially those which provide real-time interactive graphic solutions. This allows the engineer to seek the desired response and investigate the "what-if-scenerio". By providing this sort of "tune" function the designer can not only optimize for a given network response but also gain a feeling for the sensitivity of his design.

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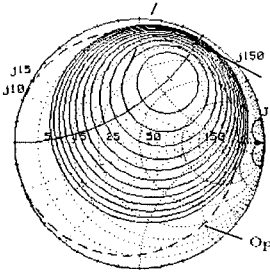
FIG 1 Power Gain Contours



S-Parameter, Class -A- Power Amplifier Design
Version 1.0
4/29/85

	1.11 .47 .965 (60.17	.783 (102.3	6.35	-5.76		
Input Scattering parameter data	2.21 .94 .932 (60.23	.766 (101.6	8.69	-3.42		
S11= .5464 (-81	3.32 1.41 .9 (60.33	.75 (100.9	9.85	-2.26		
S12= .0798 (33	4.43 1.88 .869 (60.48	.736 (100.1	10.6	-1.56		
S21= 2.8183 (119	5.53 2.35 .839 (60.66	.723 (99.39	11	-1.09		
S22= .4651 (-48	4.61 2.82 .81 (60.89	.712 (98.65	11.3	-.77		
	3.95 3.29 .782 (61.17	.702 (97.92	11.6	-.54		
Stability factor= 1.42875416389	3.46 3.76 .755 (61.48	.693 (97.2	11.7	-.372		
Maximum stable gain= 12.1092721374 dB	3.07 4.23 .729 (61.84	.684 (96.5	11.9	-.249		
Load Reflection Coefficent= .585784779614 (65.1388734015	2.77 4.7 .703 (62.25	.677 (95.82	11.9	-.159		
Source Reflection Coefficent= .648125859217 (92.5465324989	2.52 5.17 .679 (62.7	.67 (95.15	12	-.0954		
	2.31 5.64 .656 (63.19	.664 (94.51	12.1	-.0512		
Constant Output Transducer Gain Circles	2.13 6.11 .635 (63.74	.659 (93.88	12.1	-.0226		

Output Gain Circles relative (to S21^2) 9 dB

GI(dB)	Center Location	Radius	Operating Power Gain (dB)					
3.11	.586 (65.1	9.29E-9	12.1					
2.61	.534 (65.1	.246	11.6	1.98	6.58 .611 (64.34	.654 (93.27	12.1	-.00638
2.11	.486 (65.1	.348	11.1	1.84	7.05 .59 (64.99	.649 (92.68	12.1	-.000203
1.61	.442 (65.1	.426	10.6	1.73	7.52 .57 (65.68	.645 (92.11	12.1	-.00222
1.11	.401 (65.1	.491	10.1	1.63	7.99 .551 (66.44	.641 (91.56	12.1	-.011
.61	.363 (65.1	.547	9.61	1.54	8.46 .532 (67.25	.638 (91.02	12.1	-.0255
.11	.328 (65.1	.596	9.11	1.46	8.93 .514 (68.11	.635 (90.51	12.1	-.0443
-.39	.296 (65.1	.639	8.61	1.38	9.4 .497 (69.03	.632 (90.01	12	-.0672
-.89	.267 (65.1	.677	8.11	1.32	9.87 .48 (70.02	.629 (89.53	12	-.0923
-1.39	.241 (65.1	.711	7.61	1.26	10.3 .464 (71.06	.627 (89.07	12	-.122
-1.89	.217 (65.1	.742	7.11	1.2	10.8 .449 (72.17	.624 (89.62	12	-.153
-2.39	.195 (65.1	.769	6.61	1.15	11.3 .435 (73.34	.622 (88.19	11.9	-.187
-2.89	.175 (65.1	.793	6.11	1.11	11.8 .421 (74.58	.621 (87.78	11.9	-.221

POUT mW. GL mho	GLopt	GSopt	Power Gain dB	Delta dB Max
1.11 .47 .965 (60.17	.783 (102.3	6.35	-5.76	

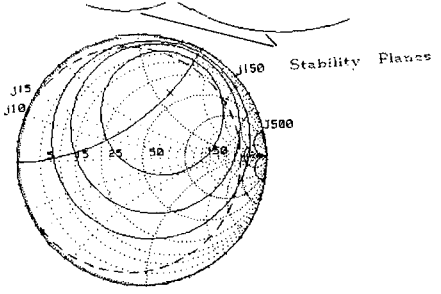


FIG2

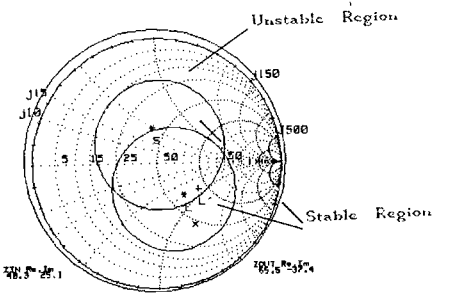


FIG 4

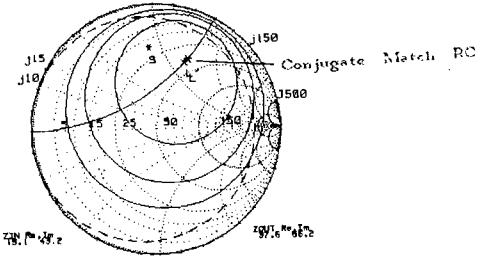


FIG 3

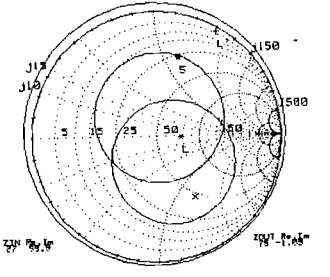


FIG 5

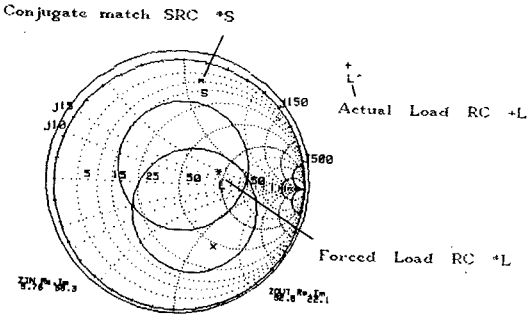


FIG 6

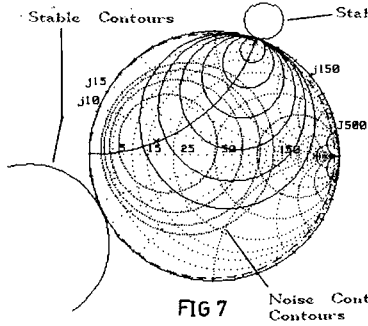


FIG 7 Noise Contours overlay power Contours

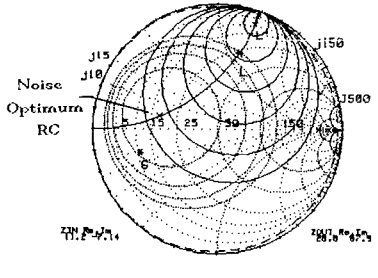
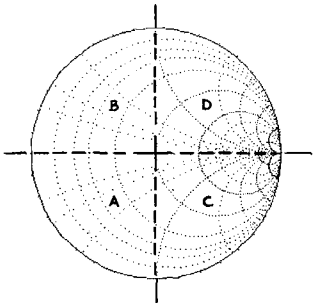
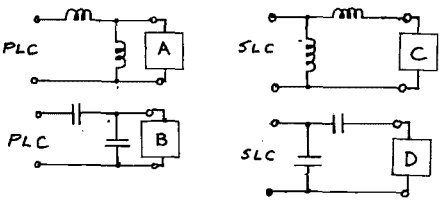


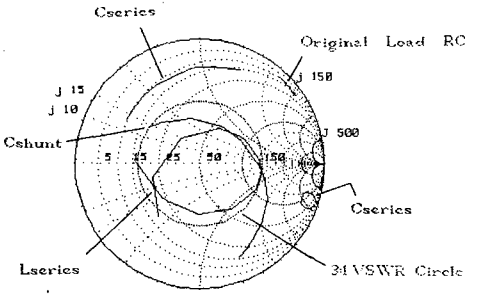
FIG8 Constant Noise Contours





Four Element Matching Networks for Maximum Bandwidth Potential

FIG9

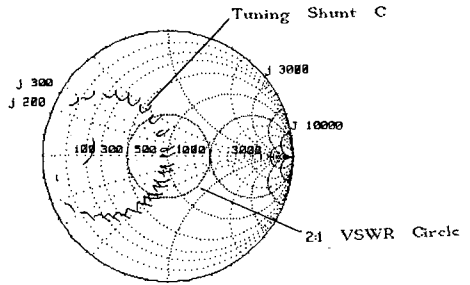


Frequency (Mhz)	Reflection Coefficent	Load VSWR	R1	I1
50	.5392 (-129.1	3.34	17.99	-21.23
51	.3994 (-163.6	2.33	21.82	-5.848
52	.2557 (126.5	1.687	34.11	15
53	.3199 (60.67	1.941	56.89	35.35
54	.4079 (30.8	2.378	89.5	44.85
55	.4815 (3.099	2.857	142.1	9.633
56	.498 (-9.617	2.984	141.3	-31.27
57	.4922 (-24.69	2.938	108.9	-59.1
58	.4679 (-54.85	2.59	58.4	-52.79
59	.4047 (-91.3	2.359	35.37	-34.22
60	.4133 (-137.5	2.409	23.29	-15.68
61	.5117 (178.6	3.096	16.15	.5387

Impedance Matching Network Starting From the Load End:

Component Description	Component Value
CAPACITOR_SERIES	32 pF.
CAPACITOR_SHUNT	68 pF.
CAPACITOR_SERIES	11 pF.
INDUCTOR_SERIES	810 nH.

FIG 10



Frequency (Mhz)	Reflection Coefficent	Lead VSWR	R1	X1
400	.1169 (-69.22	1.265	1060	-234.9
410	.1234 (-88.95	1.282	974.3	-246.2
420	.1326 (-102.7	1.304	913.1	-260.6
430	.1402 (-111.9	1.326	872	-251.5
440	.1447 (-117.7	1.338	847.4	-221.7
450	.1457 (-120.8	1.341	836.3	-214
460	.1442 (-121.3	1.337	836.5	-210.7
470	.1417 (-119.1	1.33	846.2	-213.8
480	.1405 (-114.3	1.327	863.3	-225.4
490	.1434 (-107.3	1.335	885.4	-247.4
500	.1535 (-99.29	1.363	909.9	-282.3

Impedance Matching Network Starting From the Load End:

Component Description	Component Value
CAPACITOR_SERIES	3.668 pF.
INDUCTOR_SHUNT	43.513 nH.
INDUCTOR_SERIES	139.933 nH.
CAPACITOR_SHUNT	.663 pF.

FIG11

++++++++++++++++++++ RECEIVER ++++++++++++++++++++++++++
++++++++++++++++++++ DATA REVIEW ++++++++++++++++++++++++
++

STAGE	NOISE FIGURE Db	GAIN Db	INPUT INTERCEPT(3) Dbm
1	18	100	0
2	1.5	12	10
3	4	-4	27
4	1.2	12	35
5	3	-3	100
6	8	-8	32
7	2.9	-2.9	100
8	1.9	11	35
9	1	-1	100

Rise Sensitivity is 10 Db
Receiver Noise Bandwidth is 2.4 Khz
Temperature is 298 Kelvin

30 MHZ HF COMMUNICATIONS RECEIVER

++++++++++++++++++++ RECEIVER ++++++++++++++++++++++++++
+++++++++++++++ PERFORMANCE WITH PRESENT ++++++++++++++++
++++++++++++++++++++ DESIGN DATA ++++++++++++++++++++++++

STAGE	NOISE FIGURE Db	SENS Dbm	uV	IIP(3) Dbm	IMR Dbm
2	7.268	-123.2	.1539	-12.03	74.11
3	11.27	-119.2	.2439	26.99	97.46
4	3.222	-127.3	.09658	14.94	94.83
5	6.222	-124.3	.1364	17.94	94.83
6	14.22	-116.3	.3427	24.98	94.19
7	17.12	-113.4	.4785	27.88	94.19
8	7.454	-123.1	.1572	16.81	93.27
9	8.454	-122.1	.1764	17.81	93.27

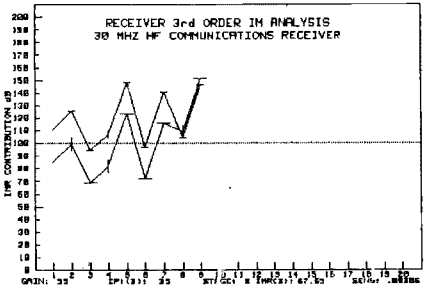
SYSTEM 3rd ORDER IMR IS= 93.27 Db
SYSTEM HALF I.F. REJECTION= 0 Db
SYSTEM SENSITIVITY= .1764 uV

++
++++++++++++++++ RECEIVER LINE-UP ++++++++++++++++++++++
++

STAGE	DESCRIPTION
1	Receiver Back End
2	IF preamp U 310
3	4 pole crystal filter
4	Mixer post-preamp
5	3 db pad
6	Passive mixer diode ring
7	3 db pad
8	RF preamplifier
9	T/R switch losses and low pass filter loss

FIG 12

FIG 13


RECEIVER 3rd ORDER IM ANALYSIS
30 MHZ HF COMMUNICATIONS RECEIVER
IMR CONTRIBUTION dB
GAIN: 33

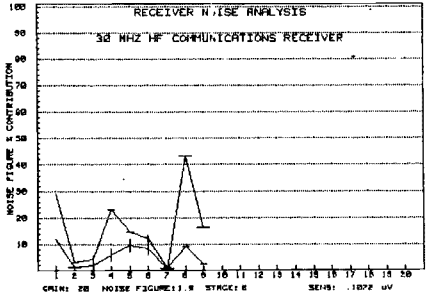

RECEIVER NOISE ANALYSIS
30 MHZ HF COMMUNICATIONS RECEIVER
NOISE FIGURE & CONTRIBUTION
GAIN: 28
STAGE: 8
SENS: .1872 uV

FIG 14

NEW HYBRID POWER AMPLIFIER MODULES SPEED RF SYSTEMS DESIGN

by

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ABSTRACT

For many years low to medium wideband RF amplifiers have been produced in TO-8, TO-12, or TO-39 packages and have become popular with users because of the wide bandwidths, flat gains, small sizes and unconditional stability they offer.

This paper will present the philosophy and design concepts offered in a new hybrid RF power module product line.

INTRODUCTION

For all the convenience and versatility TO style amplifier modules offer the user they still possess two main shortcomings:

1. RF power output is limited to about a half watt due to the relatively poor thermal conductivity of the Kovar header, and
2. Mounting of a TO style module to a printed circuit board requires physical clearance both above and beneath the board, thereby limiting the component packing density which one can achieve.

To address these two drawbacks Microwave Modules and Devices has developed a new family of Class A RF power amplifier modules, designated the HPM Series, which cover the frequency range of 5 MHz to 2 GHz and which can offer power outputs in the tens of watts. (Figure 1) They are designed in a "Drop-In" flange configuration which is ideal for efficient heat transfer and ease of circuit layout.

THERMAL CONSIDERATIONS

The RF output power of an amplifier packaged in the standard TO-8 header is limited primarily by the high RF transistor junction temperature due to the thermal conduction characteristics of the header. TO style amplifier modules are most commonly constructed of a ceramic substrate, either alumina (Al_2O_3) or beryllium oxide (BeO), attached to a Kovar header using gold-germanium solder. Kovar, an alloy of nickel, iron, and colbalt, is designed to match the thermal expansion characteristics of the ceramic substrate, thus preventing substrate cracking during temperature changes. While Kovar is an excellent mechanical match for ceramic substrates, it is an extremely poor thermal conductor (Table I). Beryllium oxide, on the other hand, is an excellent thermal conductor, having a thermal conductivity five to six times that of alumina. BeO substrates are typically used in medium power hybrid amplifiers to reduce the device junction temperature as much as possible. Its disadvantages, however, include a high cost when compared to alumina and a high toxicity hazard in a powdered or dust state.

A third substrate material, aluminum nitride (AlN), is just now beginning to become available. Aluminum nitride offers a thermal

conductivity near that of BeO without the toxicity problem of BeO. Its present cost, unfortunately, is not less than that of BeO, but, with improved production processes and economies of scale, the cost should come down.

To analyze the temperature problems inherent in packaging a one watt and higher RF amplifier into a TO-8 header the junction to mounting surface temperature rise can be computed for the three situations shown in Figure 2.

Figure 2a and 2b illustrates the cases of a 5 mil thick silicon bipolar transistor die eutectically attached to a 25 mil thick alumina (Figure 2a) or BeO (Figure 2b) substrate which is then soldered to a 50 mil thick Kovar header.

Figure 2c shows the cross section configuration used in the HPM Series product line. For comparison purposes, a 5 mil thick silicon bipolar die is again shown attached, in this case, to a 25 mil thick BeO substrate. The BeO substrate is gold-germanium soldered to a 1/8" thick flange of Elkonite® 10W3 material. Elkonite® 10W3 is a copper/tungsten powdered metal metallurgy material that is designed to match the thermal expansion characteristics of BeO while providing a high thermal conductivity (Table 1). Figure 3 shows a photograph of the HPM package. The thin film metallized BeO substrate is mounted inside the alumina "window-frame" by using gold-germanium solder and all circuit components are attached to the BeO substrate by using gold-tin solder. Interconnections are by 1 mil diameter gold bond wire.

Elkonite is a registered trademark of CMW, Inc.

Before calculating the temperature rise in all three cases, a number of assumptions will be made.

1. A semi-infinite lateral extent of the layers.
2. A 45° heat spreading angle.
3. A square heat source configuration.

With these assumptions made, the equation for the thermal resistance of a particular layer can be given as

$$R_{th} = \frac{T}{KW(W + 2T)} \quad (1)$$

Where:

T = material thickness

K = thermal conductivity

W = side dimension of the heat source

The silicon layer heat source dimension is chosen to be 6 mils square, which reflects the approximate active area of a 1 watt Class A RF transistor die.

Using the 45° heat spreading assumption, the heat source side dimension, W, is increased by twice the thickness of the material of the preceding layer. Therefore using Equation (1) the thermal resistances of the various materials can be calculated. The results are as follows:

R_{th} (Silicon) = 18.6°C/W

$R_{th}(Al_2O_3)$ = 29.6°C/W

R_{th}(BeO) = 4.6°C/W

R_{th}(Kovar) = 10.9°C/W

R_{th}(Elkonite®) = 1.5°C/W

Therefore, for the three cases, summing the thermal resistances:

R_{th} (TO-8, Al_2O_3) = 59.1°C/W

R_{th} (TO-8, BeO) = 34.1°C/W

R_{th} (HPM) = 24.7°C/W

We shall further assume that for 1 watt of Class A RF power, 4 watts total dissipation (25% efficiency) will be expended by the RF transistor. Therefore, the temperature rise of the transistor junctions for the three cases are as follows:

$\triangle T$ (TO-8, Al_2O_3) = 236.4°C

$\triangle T$ (TO-8, BeO) = 136.4°C

$\triangle T$ (HPM) = 98.8°C

With a mounting surface temperature of +50°C the junction temperature can then be computed to be:

T_j (TO-8, Al_2O_3) = 286.4°C

T_j (TO-8, BeO) = 186.4°C

T_j (HPM) = 148.8°C

The impact upon reliability of these three temperatures can be understood by using a graph of median time to failure (MTTF) versus junction temperature, the so-called "Arrhenius" relationship. Major device failure mechanisms have been shown to vary exponentially with temperature according to the equation

$$MTTF = C \exp (\Phi/KT)$$

where

C = a constant

Φ = activation energy

K = Boltzman's constant

T = temperature (°K)

Typical RF transistors under consideration use a gold metal system and have activation energies between 0.6 and 0.7 eV. If we plot the Arrhenius curve using a gold system activation energy (Figure 4), we observe that for a 20°C rise in junction temperature the device MTTF is reduced by approximately one half.

The projected MTTF of the silicon bipolar transistor used in the HPM package is found to be approximately four times greater than when mounted in a TO-8 header on a BeO substrate and one hundred times greater than when mounted in a TO-8 header on an alumina substrate. Because we have assumed that the packages are mounted to an infinite heat sink with no thermal resistance, the junction temperature of the TO-8 devices will actually be higher than those calculated. This is due to the thermally non-ideal mounting requirements inherent in TO devices.

MECHANICAL CONSIDERATIONS

TO style modules must be mounted from the back side of the microstrip PC board such that the package is in intimate contact with the ground plane. Failure to provide a positive contact between the microstrip ground plane and the package can result in gain resonances, VSWR degradation and unwanted oscillations, especially in high gain (~40dB) cascades.

Because of this requirement, clearance in the housing to which the PC board is mounted must be available both above and below the board. In high package density systems, this volume may not be available without causing the overall subsystem or system package to be larger than desired. In addition, rework and replacement is more difficult with modules mounted on the underside of PC boards. To address these drawbacks some manufacturers have developed surface mount type packages for amplifiers. However, at the present time, their use appears limited to amplifiers whose output power is less than 100 mW.

HPM AMPLIFIERS

The Microwave Modules and Devices HPM series provides an alternative to discrete device amplifiers for those users who enjoy the ease of design and use that existing TO style or surface mount amplifiers offer, but who require higher output power or lower distortion. The HPM product line is an attempt to solve the thermal and mechanical limitations inherent in the TO-8 style packages and is designed as a "Drop-In" component, not unlike existing flange mounted RF power transistors, which is ideal for efficient heat transfer. The "Drop-In" configuration also simplifies the circuit board and housing design.

The HPM product line presently consists of several models (Figure 5) which cover the frequency range of 5 MHz to 2 GHz with models under development that will offer power outputs in the tens of watts.

The HPM package is epoxy sealed and leak tested to ensure high reliability. For military applications requiring conformance to MIL-STD-883 a totally hermetic version is being developed. Figure 6 shows a photograph of a prototype hermetic package. This package is designed to be welded closed by using either laser or seam sealing techniques and will provide a leak rate better than 1×10^{-7} atm-cc/sec.

To illustrate the similarity in concept and integration with existing small signal cascadable amplifiers, Figure 7 shows a connectorized housing designed to accommodate up to 3 TO-8 modules driving an HPM module.

REFERENCES

1. "Handbook of Electronic Packaging" McGraw-Hill, 1969.
2. "Engineering Materials Handbook" Montell, First Edition, 1958.
3. "Handbook for Applied Engineering Science" Chemical Rubber Company, Second Edition, 1973.

TABLE 1
Thermal Conductivity and Thermal Expansion
of Various Materials

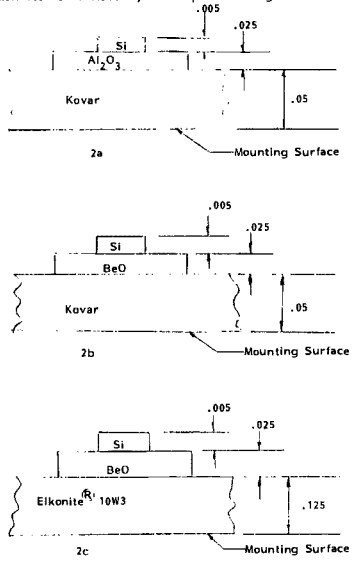
MATERIAL	THERMAL CONDUCTIVITY Watt/°C-in	THERMAL EXPANSION in/in x 10^{-7} /°C
99.6% Al_2O_3	0.80	65
99.5% BeO	5.1	90
Gold	7.5	142
Aluminum	6.4	236
Silver	10.6	197
Kovar (Fe, Ni, Co)	0.42	60
Silicon (@ +95°C)	2.8	35
Molybdenum	4.0	53
Elkonite® 10W3(Cu,W)	6.8	95
Copper	9.5	167
Tungsten	4.2	44

FIGURE 1

HPM Series Package

FIGURE 2

Cross Section View of Various Hybrid Amplifier Configurations



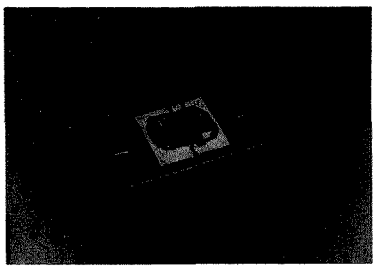


FIGURE 3

Inside View of HPM Series Amplifier

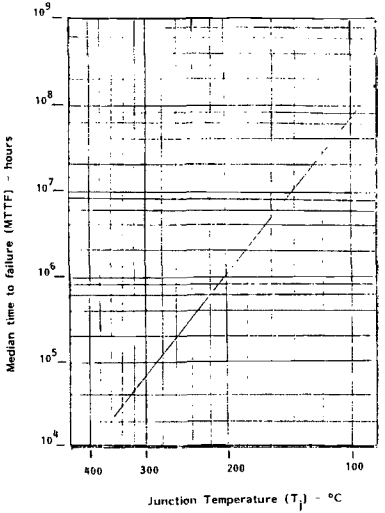


FIGURE 4

MTTF Versus Junction Temperature

FIGURE 5

Typical Performance Characteristics of HPM Product Line

MODEL	FREQUENCY RANGE	GAIN	POWER OUTPUT @ 1dB GAIN COMPRESSION	DC POWER
HPM 501	5-500	10 dB	1.5 Watts	+24V @ .6A
HPM 505	10-500	8 dB	6 Watts	+24V @ 1.2A
HPM 1002	20-1000	9 dB	3 Watts	+24V @ .8A
HPM 2000	50-2000	1[illegible] dB	.25 Watts	+15 @ .3A
HPM 2001	50-2000	10 dB	1.5 Watts	+15' @ .75A

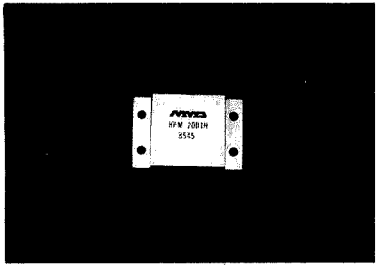


FIGURE 6

Prototype Hermetic HPM Package

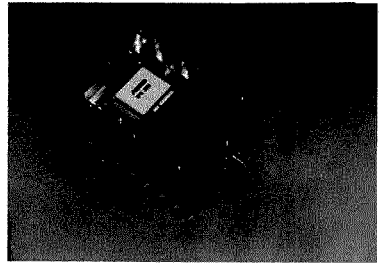


FIGURE 7

Connectorized HPM Enclosure with Capability for 3 TO-8 Style Amplifiers

DESIGN CONSIDERATIONS FOR A 1 KW L-BAND RADAR MODULE

by
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INTRODUCTION

Completely solid-state transmitters for very high power radar systems, such as the SPS-40, PAVE PAWS, or TPS 59 have clearly demonstrated several advantages over tube equipment:

- Overall reliability is greatly improved.
- System down time is decreased.
- Individual modular amplifiers can be replaced while the radar continues to operate.
- Very wide operational bandwidths are easy to achieve.
- Modular solid-state transmitters are ideally suited for phased array systems.

Even though the first solid-state radar systems were significant steps forward in the state-of-the-art, many areas can still be improved further. Microwave Modules & Devices (MMD) has found that an integrated technology approach to the modular amplifier design offers significant performance improvements. MMD's integrated approach includes optimization of the design of the transistor die, device packaging, and special matching components targeted for the specific amplifier program. Areas where performance improvements can be the most dramatic using this integrated approach are:

- Higher power output per module.
- Reduced module cost and improved manufacturability.
- Amplifier efficiency
- Module reliability.
- Ease of combining large numbers of amplifier modules.
- Thermal management.
- Significant increases in power output per cubic inch of module volume.
- Amplifier bandwidth.
- Harmonic reduction.

This paper will address some of these important performance areas as they apply to the design of the new MMD AC-1214-1000P L-Band radar modular building block. Performance improvements push the state-of-the-art forward and make solid construction of multi-kilowatt transmitters more practical than ever. A summary of the performance of the MMD AC-1214-1000P is shown in Table 1.

AMPLIFIER ARCHITECTURE

The 1 KW amplifier architecture (Fig. 1) is a modular structure with commonality that centers around a well designed 350

watt, building block, sub-module. A basic driver module delivers power to a single sub-module which then drives an array of four sub-modules via a 4-way divider. The sub-modules are then combined through a 4-way combiner and that output is put through an isolator for VSWR protection of the amplifier.

SUB-MODULE

The sub-module uses two separate transistors that are thermally independent. These two transistors are interconnected in a parallel configuration. Figure 2 illustrates the structure of the MMD sub-module. This block is optimized for use as a wideband power amplifier with 50 ohm interface impedance levels. As a result the sub-module becomes an easy to use building block throughout the amplifier. Some of the features of the MMD sub-module are listed in Table 2 and a performance summary is shown in Table 3. To realize a high performance, RF power module (see Fig. 3) that is reliable and reproducible, the design should start at the chip level and build from there. The design of the electrical and mechanical interfaces of the chip with the rest of the module are crucial to the final electrical performance and the long term reliability of the module. Starting a state-of-the-art module design using off-the-shelf RF power transistors often limits both performance and reliability. Following initial electrical ship interfaces, the wideband impedance matching circuitry must be configured.

PERFORMANCE OF MMD'S AC-1214-1000P

1 KILOWATT L-BAND MODULE

POWER OUTPUT:	1000 WATTS MIN.
FREQUENCY RANGE:	1.2 TO 1.4 GHZ
POWER INPUT:	1 WATT
EFFICIENCY:	20% MIN
PULSE WIDTH:	10 USEC
DUTY CYCLE:	5%
OPERATING VOLTAGE:	45 VOLTS
RISE TIME:	200 USEC MAX.
FALLTIME:	200 NSEC MAX.
DROOP:	.5DB MAX

Table 1.

FEATURES OF MMD

SUB MODULE

- 2.0:1 VSWR IN AND OUT
- SMALL SIZE
- EASY TO MANUFACTURE
- CONSISTENT ELECTRICAL PERFORMANCE
- WIDE BANDWIDTH AT HIGH POWER

Table 2.

PERFORMANCE OF MMD 350 WATT

SUB-MODULE

POWER OUTPUT:	350 WATTS MIN.
FREQUENCY RANGE:	1.20 TO 1.40 GHZ
GAIN:	7 DB MIN
EFFICIENCY:	40%
PULSE WIDTH:	10 J SEC
DUTY CYCLE:	5%
OPERATING VOLTAGE:	45 VOLTS
RISE TIME:	75 NANOSECONDS (SEE FIG 11)
FALL TIME:	40 NANOSECONDS (SEE FIGURE 11)
PULSE DROOP:	0.2 DB

Table 3.

Two approaches to the sub-module electrical design were considered; the first, was a push-pull configuration, and the second, a parrallel configuration. The push-pull design has the advantage of reduced even harmonics and higher input and output impedances at the device level, but the disadvantage of increased size and complexity. The parallel transistor design has the disadvantage of higher even harmonics and lower input and output impedances at the transistor, but parallel transistor configuration has advantages of smaller size and reduced complexity. Since two of the prime considerations were small physical size and large production quantities, the parallel transistor configuration was chosen for the sub-module design. Even harmonics can be dealt with without much difficulty because of the 15% bandwidth. The microstrip circuit design used for matching the devices is a simple low pass ladder-type network which is straight forward to design and construct. Since the input and output (load conjugate) impedances of the device are quite similar (and both are inductive), the matching circuit is basically the same for both input and output.

First, a simple ladder network is designed to match the impedance of one device referenced to ground (load). Figure 4 illustrates a simple "pi" type match from the device impedance to 15 ohms. Next, the two single ended matches are parallel to give 7.5 ohm impedance. The 7.5 impedance is then transformed to 50 ohms with a 20 ohm transmission line of the appropriate length as

shown in Figure 5. Care must be taken with the DC feed design for the best rise time performance, particularly on the input (emitter) side. The feeds should be connected to the lowest possible RF impedance point and have only enough inductance to avoid circuit detuning. As can be seen in Figure 5, the DC feed on both the input and output circuits are connected where the transistor matching networks are paralleled. This is the lowest impedance point where a single inductor can be used. As a result the inductance used to connect into these feed points can be kept to a minimum, thus minimizing the rise time (the rise time of the intrinsic transistors is less than 10 nanoseconds).

The mechanical chip interface is a primary reliability consideration. A major design goal of the modules is to minimize the thermal resistance between the chip and the baseplate. The lower the thermal resistance, the cooler the chip operates and therefore the greater the reliability. The sub-module configuration uses two active areas that are physically separate to better distribute the heat, resulting in lower active area temperaures and improved reliability.

When attempting to design a basic system building block, the ideal is to make all RF connections at the 50 ohm impedance level which is compatible with the system Zo.

By using the sub-module as a building block, the appropriate configuration of blocks can be arranged to construct the 1 KW amplifier as shown in Fig.1.

TRANSISTOR DIE SELECTION

The heart of any solid-state amplifier design is the semiconductor die and much attention must be paid to this area.

Four basic types of power semiconductor die are available for use at this frequency:

- GaAs MESFET
- Silicon vertical MOSFET
- Silicon Junction FET or SIT
- Silicon Bipolar

GaAs MESFETs are horizontal structures with all three terminals (gate, source, and drain) on the top surface. This creates a major problem with large high power devices for both surface interconnect metallization complexity and device wire bonding. Also GaAs material has a high thermal resistance compared to silicon as well as numerous crystal defect problems that result in very low yields for large area, high power devices.

The silicon vertical MOSFET device is very promising for lower frequencies, but higher device capacitances (compared to silicon bipolar) create significant stability, output matching

and/power transfer problems at L-Band. Several lower capacitance MOSFET designs have been announced but none has yet to be proven repeatable, manufacturable and reliable. Junction FETs (or SITs) presently available are not useful for 500 MHz because gain and efficiency are too low and the output capacitance is too high. Some new design concepts show promise, particularly for higher voltage operation but production quantity devices are not available.

This then leaves the silicon bipolar device, which in fact, proves to be an excellent solution. Recent processing technology improvements combined with new die geometries have resulted in large signal ft's of over 5 GHz from high power L-band devices.

Two basic types of silicon bipolar die configuration are available for pulse operation at L-Band. Die A (Fig. 6A) has two large base areas perpendicular to the input/output die bonding.

The common lead is bonded down the centerline of this die. The input bonding is staggered from front to back, alternating between the common lead bonds. Die B has many smaller base areas (Fig. 6B) which are arranged parallel to the input/output bonding. Both input and common lead bonds are arranged in an alternating pattern down the center line of the die.

Also to be chosen was the device terminal to be used as ground (common base vs common emitter). For both die types, common base is preferred due to higher gain and better thermal sharing over the device surface during pulse operation at these frequencies.

Advantages of die A are:

- More base area (and therefore emitter perimeter for power capability) per mil of die length.
- Better output capacitance/power ratio (0.4 pF/watt VS 0.5 pF/watt for die B)
- Fewer bond wires.

Disadvantages of die A are:

- Unsymmetrical input (emitter) bonding and wide (7 mil) base cells restrict upper frequency response.
- Limited pulse width/duty factor capability (100 use 5% maximum)

Advantages of die B are:

- Narrow die and numerous base bond wires give very low common lead inducture for improved ruggedness, stability, input/output isolation, efficiency, and upper capability.
- Spread base cell design allows operation from short pulse to CW due to better thermal balance.

Disadvantages of die B are primarily related to a slightly more complex structure to manufacture and assemble.

TRANSISTOR PACKAGING AND INTERNAL MATCHING

Three types of device internal matching were considered: 1) single ended, using a double input and a paralls output resonance matching (Fig. 7); 2) single ended, single input match (Fig. 4); and 3) the split push-pull using a single input match (Fig. 8). The high impedances of the more complex single ended device at least equalled using the four times impedance increase of the single input matched device when split and used push-pull. The disadvantages of the output matched construction must also be considered.

- The series resonance of L1 and C1 (Fig. 7), typically just below the low end of the band (about 1.1 GHz) causes serious oscillation problems when fast rise/fall times are employed. This usually shows up as a "noisy" spurious signal at 1.1 GHz only 20-30 dB down or as a distortion "glitch" on the detected pulse turn-off slope.

  The parallel tank circuit of the output match causes major output signal phase shifts when the device output capacitances change. This "phase modulator" effect can cause phase noise and power combining problems. The output capacitance is, unfortunately, a function of many things including voltage, power level, temperature, and die manufacturing variations.

- Failure of the DC blocking capacitor (C1) has historically been a reliability problem with this type of output matching structure.

Of the three internal matching techniques considered for the transistors, the single ended input matched device was chosen because it was the least complex, both internal to the transistor package and to external circuitry. It would also yield the smallest module size. The single input match chosen will sacrafice some bandwidth and an increase in even harmonics. Typical performance of a single transistor is shown in Table 4.

The die of each transistor is packaged in the BeO ceramic cavity shown in Fig. 9. Note the very wide input/output leads for low inductance of those interfaces. This allows low "Q" device impedances for good broadband performance when shunt tuned and operated into the matching networks. The leads are "captive sealed" between the device lid and the single layer ceramic ring for improved lead strength. Co-fired multi-level ceramic ring packages with exposed, non-captive leads were avoided due to high lead inductance and numerous lead failure problems. 40 mil thick

BeO ceramic is used for the package substrate for improved thermal resistance.

Frequency - 1.2 to 1.4 GHz
Pout - 200 Watt
Gain - 7.0
Efficiency - 45%

TYPICAL TRANSISTOR DATA

Table 4

THERMAL CONSIDERATIONS

Many variables effect the junction temperature of the devices used in the amplifier, including:

- amplifier efficiency and output power
- pulse width/duty factor
- die thermal response time
- die thermal balance ("hot spots")
- overall module baseplate temperature
- die to baseplate thermal resistance

A good indication of the presence of hot spots (and therefore high junction temperature) is the power droop over the length of each output pulse. A droop of 0.2 dB for 30 degrees C baseplate temperature will degrade to 0.5 at elevated temperature. A droop of 0.5 dB at 30 degrees C will degrade to more than 1.0 at elevated temperatures. Droop of over 1 dB is usually an indication of excessive junction temperature. The ultimate thermal test of any amplifier is a scan of all amplifier die with an infared microscope under actual operating conditions. Typical requirements might be a maximum junction temperature of 140 degrees C with a baseplate temperature of 85 degrees C. Thermal scans for pulse widths less than 5 usec are difficult due to risetime limitations of infared sensors, but are essential for verifying reliable amplifier design and construction.

DIVIDER/COMBINERS CONSIDERATIONS

To achieve the required 1 KW output power, four of the sub-modules must be combined, therefore a divider and combiner must be designed. Two basic types of combining schemes were considered; 1) the Wilkinson combiner and; 2) 90 degree 3 dB hybrid.

Advantages of a Wilkinson divider/combiner

- Excellent amplitude balance.
- Excellent phase balance
- Easy to manufacture basic circuit
- Low insertion loss
- Good port to port isolation

Disadvantages:

- No VSWR isolation at the divider.
- No reduction in back IMDs at combiner.
- Difficult to reduce or eliminate the effects of the capacitanc of isolation resistor.
- Small size can be difficult to achieve and still handle high power.

Advantages of 90 degree 3 dB hybrid:

- VSWR isolation at divider.
- Reduction in back IMDs at combiner.
- Improvement in harmonics.
- 50 ohm terminations are required therefore, capacitance of termination is less of a problem.
- with proper design small size can be achieved.
- Low insertion loss.
- Good port to port isolation.

Disadvantage:

- Amplitude imbalance.

There are several 90 degree 3 dB Hybrid configurations (branch line, backward wave, rat-race, wireline, etc.), but because physical size is of paramount importance the Sage tightly coupled wireline coupler was chosen. Fig. 10 shows the typical insertion loss of a wireline coupler and how the amplitude balance is typically less than 0.2 dB over the frequency band of 1.2 to 1.4 GHz. Fig. 11 is a plot of insertion loss versus frequency of a 4-way divider/combiner the amplitude balance between any of the four ports is less than 0.6 dB peak-to-peak. The physical size is 1.0"W x 4.00"L x .30H for the 4-way combiner including two of the three isolation termination (the output isolation termination is mounted to the bottom of the amplifier housing for better heatsinking).

A combiner and divider were coupled back to back and insertion loss measured and the data is shown in Fig. 12. which shows the insertion loss to be less than .6 dB for a divider and combiner connected back to back.

LOW LEVEL DRIVER MODULE

The block diagram for the driver is shown in Fig. 13. There are three stages that make up the driver plus two attenuators. The 2.0 dB attenuator at the input of the driver is for reducing the drive to the first stage for overdrive protectionand input VSWR improvement. The second stage provides the power to drive the third stage to approximately 100 watts. The 2.0 dB attenuator at the output of the third stage provides VSWR isolation between the output of the driver module and the input of the 350 watt sub-module driver stage. The performance of the drive stage is shown in Table 5:

Freq.	1.2 to 1.4 GHz
Pout	70 watts min.
Pin	1.0 watts
Vc	45 volts
Ic	9.0 amps (PK) max

INPUT RETURN LOSS -13dB max

TYPICAL PERFORMANCE DATA

LOW LEVEL DRIVER

TABLE 5

1.0KW AMPLIFIER PERFORMANCE

Table 6 is the tabulation of the performance of the 1 kW amplifier module for 1.0 watts input drive. It can be seen that the amplifier module meets or exceeds the design goal set down in Table 1.

CONCLUSION

Multikilowatt all solid state amplifiers are seeing increased popularity. With the availability of modular building blocks such as the 350 watt sub-module, these high power amplifiers are both practical and easy to assemble. The sub-module building block using an integrated design from the silicon out to the 50 ohm terminal can be totally optimized for specific program requirements. The module described above was targeted for narrow pulse width, (10 usec) low duty cycle (5%) application. The same design approach and integrated technology can be applied to long pulse, high duty cycle applications as well. The practical realization of both parallel combining of transistors and 90 degree combining within the amplifier truly provides a wideband, reproduceable 50 ohm block that can be used to build multikilowatt systems.

Freq. GHz	Pout W	Pin W	RL dB	Ic Amps (Avg)	Pulse Droop dB
1.2	1148	1.0	-20	4.4	0
1.3	1445	1.0	-12	5.2	-.3
1.4	1175	1.0	-16	4.2	0

Vc = 45 Volts

Duty Cycle = 4%

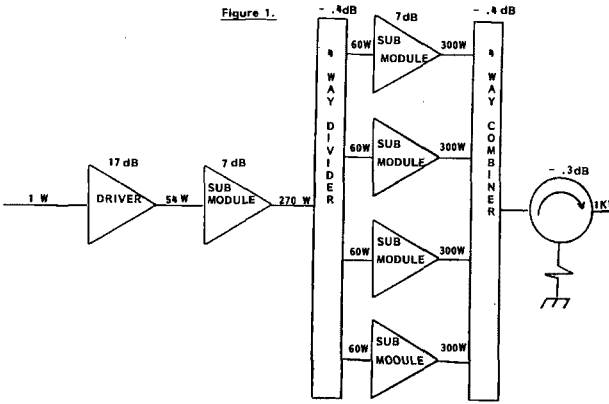
Pulse Width 7 use

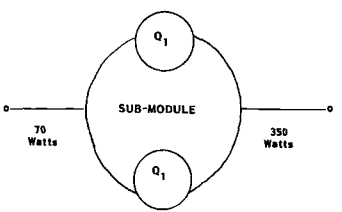
TYPICAL PERFORMANCE DATA

1KW L-BAND POWER AMP.

Table 6

Figure 1.





MMD 1.2 to 1.4 GHZ, 350 WATT, SUB-MODULE

Figure 2

CAIN VS FREQUENCY

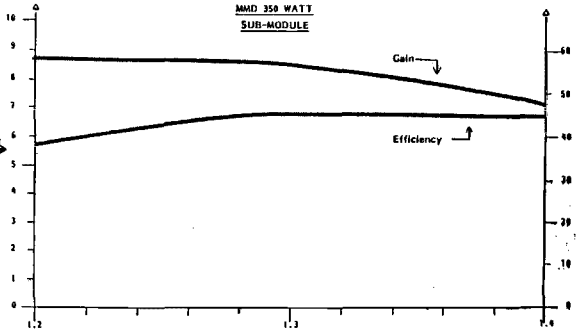
AND

EFFICIENCY VS FREQUENCY

OF

MMD 350 WATT

SUB-MODULE



Freq. (in GHZ)

Figure 3

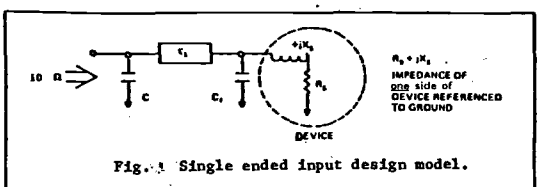
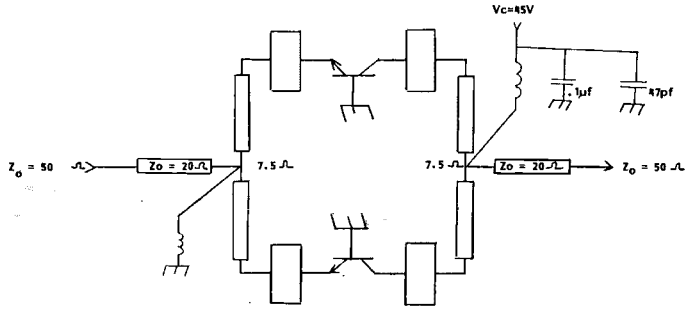


Fig. 4 Single ended input design model.



MMD 1.2 to 1.4 GHz 350 watt. SUB-MODULE

Figure 5

L-BAND DIE CONFIGURATIONS

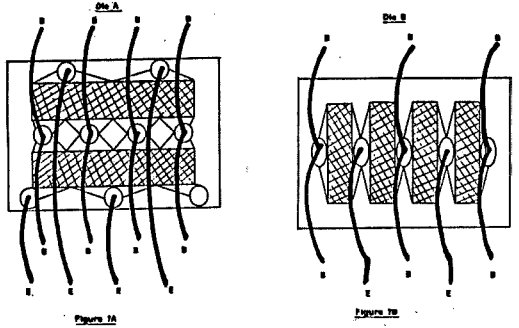


Figure 7A

Figure 7B

Figure 6

SINGLE ENDED DEVICE MATCHING

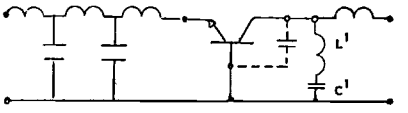


Figure 7.

SPLIT PUSH-PULL DEVICE MATCHING

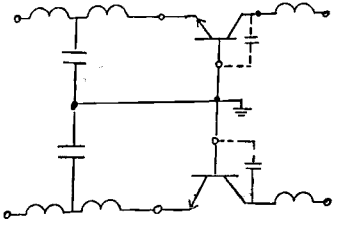


Figure 8

THE PACKAGE

USED FOR THE PUSH-PULL PAIR

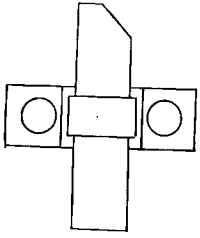


Figure 9

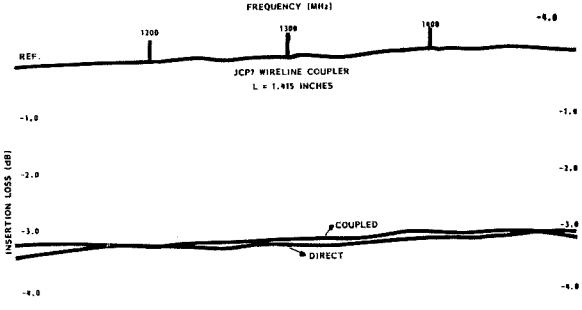
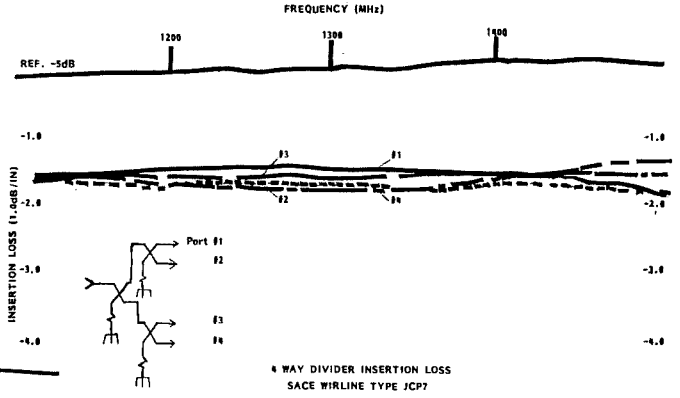


FIGURE 10



4 WAY DIVIDER INSERTION LOSS
SACE WIRLINE TYPE JCP7
LENGTH = 1.450 INCHES

FIGURE 11

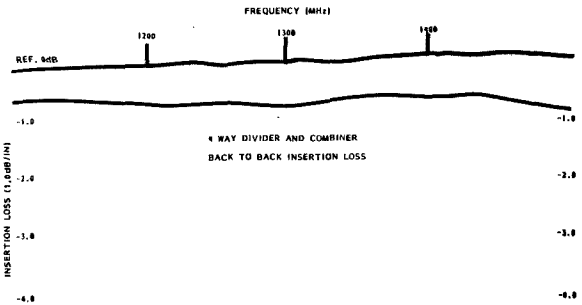
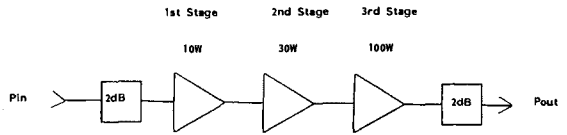


FIGURE 12



BLOCK DIAGRAM LOW LEVEL DRIVER

Figure 13

THE BASICS OF R. F. POWER AMPLIFIER DESIGN

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What I hope to do in this paper is to provide a basic idea of why RF power amplifier schematics look the way they do. The examples used are solid state 2 meter communications amplifiers. A frequency high enough to illustrate some points and low enough to use discrete components. We won't cover transmission lines, cavities, etc..

With low priced personal computers and low cost design software, you have to be foolish not to be using a computer for your design work. However, I will intentionally ignore computer design programs. Design programs present an interesting paradox. If you are familiar with designing amplifiers, they allow great insight into an optimum design as they allow you to run through and compare many designs quickly. On the other hand, if you are not familiar with the design process, they can mask what is going on. I am assuming you wouldn't be listening to a basic presentation, such as this, if you were already familiar with the design process and, hence, am ignoring computers.

We will not discuss "S" parameters, or the other tools for gain and stability calculations. Some people say such parameters are not useful for power amplifiers. I feel they are quite useful, but will not go into them in this paper. They are beyond the scope of this basic discussion and the subject is treated extensively in the literature [1,2,3,4,5] on small signal amplifiers. The techniques are the same for power amplifiers.

And, wonder of wonders, I won't even mention the Smith chart (Although I think I just did).

To begin, what is an amplifier? For our purposes, an amplifier is an assembly of components using input RF power to convert a source of DC power into output RF power of greater magnitude than the input RF power. This is not a definitive definition, so don't worry about the nuances of the wording.

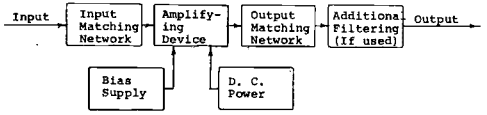
The important parts of a basic amplifier are shown in Figure 1. Let's take a few examples of typical amplifiers and build some schematics. We will start with a 146 MHz amplifier which we want to deliver 50 Watts into a 50 Ohm load, work off a 13.0 Volt supply, and use an FET as a grounded source amplifier.

First, lets consider the output network.

Using the basic $E = \sqrt{PR}$ (and incidentally, we are not going to use formulas that are much more complex than this), we find that to deliver 50 Watts to 50 Ohms, we must supply 50 Volts rms. Obviously, in order to get 50 volts rms from the 13.0 volt supply, the output network must act as a step-up voltage transformer. To state it a bit differently, the output network must transform the 50 Ohm load so that the transistor sees a lower impedance.

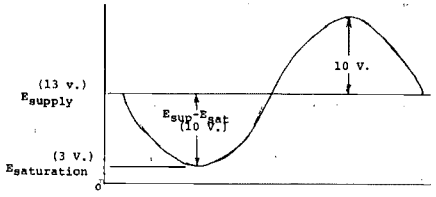
If we asaume the matching network includes tuned circuits of reasonable Q, the waveform of Figure 2 is is the maximum that we will see at the output (drain) of the FET. The output will swing from the supply voltage toward zero down to some minimum voltage limited by the transistor and will swing above the supply voltage approximately the same amount. If, for the sake of this example, we assume that E_{sat} is 3 Volts, we have a maximum voltage of 10 Volts peak (13 V. - 3 V.), or about 7 Volts rms. $E_{rms}=E_{peak}/\sqrt{2}$. To get our 50

Figure 1



BASIC R. F. POWER AMPLIFIER

Figure 2



DRAIN WAVEFORM - MAXIMUM OUTPUT

Watts, the transistor must see an impedance of:

$$R_L = \frac{E_{rms}^2}{P} = \frac{(E_{peak}/\sqrt{2})^2}{P} = \frac{E_{peak}^2}{2P} = \frac{(E_{supply}-E_{sat})^2}{2P} = \frac{(13-3)^2}{2 \cdot 50} = 1\,\Omega \qquad 1)$$

Thus, the output matching network must transform the 50 Ohms load down to present 1 Ohm to the transistor. If this were an audio amplifier, the output matching network might be a 1 Ohm to 50 Ohm transformer. Because we are designing an amplifier for communications purposes, we will want to add some filtering to the network and we can use narrow band networks.

Note that, other than to consider a saturation voltage, we haven't paid any attention to the transistor. We haven't worried whether it was bi-polar, an FET, or made out of "molded muckite". We have simply said that to get 50 Watts from a 10 Volt peak sine wave we have to present it with a load of 1 Ohm.

Also note that we haven't tried to "match" it's output impedance. Again, we simply determined that with a 13 Volt supply, and a device with a saturation voltage of 3 Volts, the transistor must "see" 1 Ohm to deliver 50 Watts.

There is a common misconception that power amplifiers are designed to "match" the output impedance of the transistor; or to us sophisticated RF types, you need a network that presents a "complex conjucate match".

This is not true, and is not true in most power work. If you want to build a toaster, you select the resistance of the heating element to draw the desired power at the voltage available. You do not select a resistance to "match" the source impedance of the power company generators. You would sure brown your toast in a hurry if you did.

Of course, we are not really ignoring the transistor. We are assuming that the device chosen is satisfactory for the supply voltage, has sufficient gain

for the application at the operating frequency, can deliver the required current, has sufficient dissipation capabilities and other parameters to assure adequate operating life, etc. In fact, long before you start with the specifics of a particular design, the chances are that you have spent many hours with data sheets deciding which devices are suitable for the application.

Also, the transistor input and output usually appears reactive and our networks will have to account for these reactances.

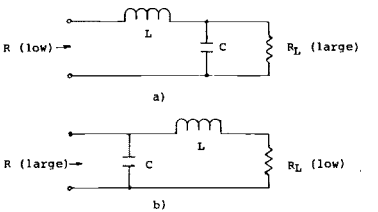
Back to the output network. There are many networks that will transform 50 Ohms to 1 Ohm, and the literature abounds with analyses [6,7,8,9,10,11,12,13,14] of them. For this example I will use a pair of basic "L" networks.

The "L' network (Figure 3a or 3b for the low-pass version and Figure 4a or 4b for the high pass), is a basic building block used in many situations. Although well covered in the literature, we will quickly derive the applicable formulas. I would like to take the time because it is such a basic building block. We will be using the circuit of Figure 3a as our example.

We picked a low pass version because in a well designed amplifier the only spurious signals created by the amplifier are harmonics. Why not use the matching network to help in their removal? If we are using the network to match unequal impedances (R_s not equal to R_p) the response of the network is peaked and a perfect match only occurs at the peak of the response. If the Q is low enough, the bandwidth can be reasonably large.

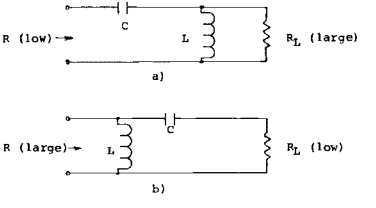
For zero insertion loss, the loaded Q of the series arm must equal the loaded Q of the shunt arm at the peak frequency.

Figure 3



BASIC "L" NETWORK - LOW-PASS CONFIGURATION

Figure 4



BASIC "L" NETWORK - HIGH-PASS CONFIGURATION

The design of a matching network lies in our ability to represent a series combination of components as an equivalent parallel combination, and vice versa (Fig. 5). At the conversion frequency, and it is valid at only one frequency, the series and parallel equivalents will have the same impedance. For Qs greater than one, the series equivalent resistance will always be smaller than the parallel equivalent resistance.

There are many ways to derive the proper values, but we will rely on the fact that the Qs must be equal. First, some familiar formulas.

For parallel components, $Q = \frac{R_L}{X_P}$ 2)

For series components, $Q = \frac{X_S}{R}$ 3)

The standard series to parallel transformation formulas, based on Q, are:

$$X_P = \left(1 + \frac{1}{Q^2}\right) X_S \quad 4)$$

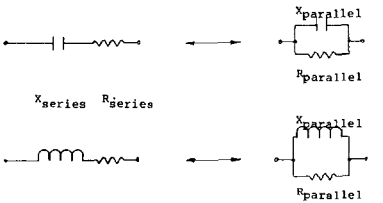
$$R_P = \left(1 + Q^2\right) R_S \quad 5)$$

Note that the Q used here is not the total Q of the network but rather the Q of just the two components being considered. In the case of an L network, with the Q of the series arm the same as the Q of the parallel arm, the network Q is 1/2 the Q of each arm, when matched at each end.

In our particular case we have the situation of Figure 6a. We are trying to make a 50 Ohm load appear to be 1 Ohm.

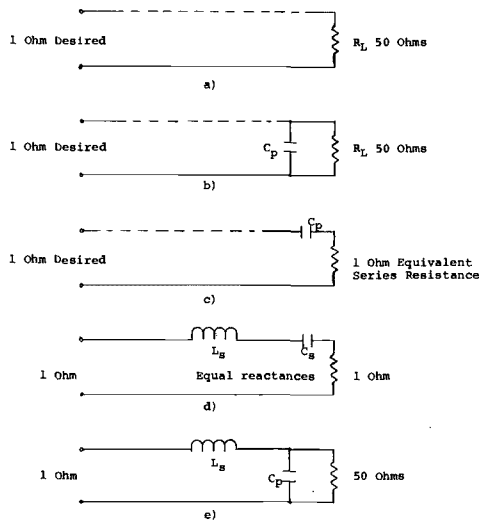
Place a capacitor across the load as in 6b. At any single frequency we can

Figure 5



SERIES / PARALLEL TRANSFORMS

Figure 6



DERIVATION OF BASIC "L" NETWORK

replace the combination of parallel capacitor and load with a series equivalent. If the right value of parallel capacitor was used, the equivalent series resistor can be made to be 1 Ohm. (Figure 6c)

If we now place an inductor in series, which has the same reactance magnitude as the computed series capacitor, the reactances will cancel and the impedance looking into the network will be our desired 1 Ohm. (Figure 6d)

Transforming the output section back to a parallel circuit, we have the finished network of Figure 6e. Now lets put some numbers on things. Rearranging series to parallel transformation formula 5), above, and solving for Q, we have.

$$Q = \sqrt{\frac{R_p}{R_s} - 1} \qquad 6)$$

In our case, $$Q = \sqrt{\frac{50}{1} - 1} = 7 \qquad 7)$$

From 2) the reactance of the parallel capacitor is,

$$X_p = \frac{R_p}{Q} = \frac{50}{7} = -j\,7.14\Omega \qquad 8)$$

And, from 3), the reactance of the series inductor is,

$$X_s = R_s \cdot Q = 1 \cdot 7 = j\,7\Omega \qquad 9)$$

Note that the reactance of the series inductor is not the same as that of the parallel capacitor; although in high Q cases it is often considered so for convenience.

The Q of the network is 1/2 the Q of either branch, or,

$$Q_{total} = Q_B/2 = Q_p/2 = 7/2 = 3.5$$

Lets calculate the component values at our selected operating frequency of 146 Mhz.

$$C = \frac{1}{\omega X_C} = \frac{1}{2\pi f X_C} = \frac{1}{2\pi \cdot 146\cdot 10^6 \cdot 7.1\Omega} = 153 pF \qquad 10)$$

$$L = \frac{X_L}{\omega} = \frac{X_L}{2\pi f} = \frac{7}{2\cdot\pi\cdot 146\cdot 10^6} = 7.6\ nH \qquad 11)$$

Note that the Q was determined only by the impedance ratio and the values were determined by Q, impedances and frequency. This is one disadvantage of the simple L network; we can't choose Q. Two elements simply do not give us enough degrees of freedom. By making our network a three element network, such as the T and π we can, with some limitations, design for a specific Q.

Four element networks give us one more degree of freedom and are often used for broadband matching. One version of a four element network is two cascaded L sections; transforming the load to some intermediate value with one section and matching the intermediate value to the final impedance with the second. Each section has a smaller step up and will operate at lower Q. Maximum bandwidth is achieved if the Q of each is the same. This occurs when:

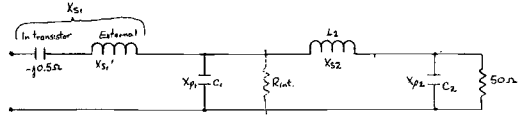
$$R_{Intermediate} = \sqrt{R_{Smaller} \times R_{Larger}} \qquad 12)$$

The process can be continued with three, four, or more, sections; although little is generally gained with more than three.

Lets recalculate our output network as a two section L network. For convenience, I have summarized the calculations in Figure 7. I have added a

Figure 7

$$R_L = \frac{(V_{DS} - V_{SAT})^2}{2 P_{out}} = \frac{(13-3)^2}{2\cdot 50} = 1\Omega \quad \text{for } P_{out} = 50W.$$



For maximum bandwidth $R = \sqrt{R_S R_L} = \sqrt{1\cdot 50} = 7.07\Omega$

$$Q = Q_1 = Q_2 = \sqrt{\frac{R_{int}}{R_m} - 1} = \sqrt{\frac{7.07}{1} - 1} = 2.46$$

$X_{S1} = Q\cdot R_S = 2.46\cdot 1 = 2.46\Omega$ $X_{S1}' = 2.46 + 0.5 = 2.96\Omega$	$L_1 = \frac{X_{S1}'}{\omega} = \frac{2.96}{2\cdot\pi\cdot 146\cdot 10^6} = 3.2\ nH$
$X_{P1} = \frac{R_{int}}{Q} = 2.86\Omega$	$C_1 = \frac{1}{\omega X_{P1}} = 381 pF$
$X_{S2} = Q R_{int} = 17.4\Omega$	$L_2 = \frac{X_{S2}}{\omega} = 18.9\ nH$
$X_{P2} = \frac{50}{Q} = 20.3\Omega$	$C_2 = \frac{1}{\omega X_{P2}} = 53.6 pF$

146 MHz OUTPUT MATCHING NETWORK USING TWIN "L" NETWORKS

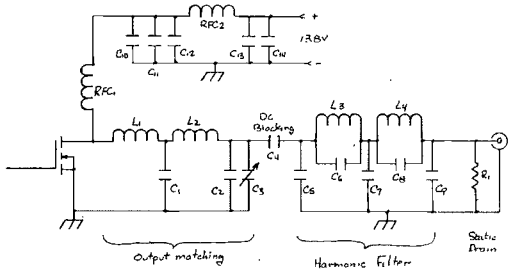
wrinkle and picked an F1260 MOSFET as our device. The data sheet indicates a series equivalent output reactance of -j.5 Ohms at 146 MHz. I absorbed this .5 Ohms by making the first inductor .5 Ohms larger. We could also have handled the reactance by resonating it with a shunt inductor (somewhat inconvenient for DC). At this power level and frequency bi-polar transistor outputs generally look inductive and a shunt C is common.

Figure 8 is a partial schematic showing what the output part of the amplifier we have been discussing might look like.

We are discussing power amplifiers and it might be useful to stop and discuss just what is different when compared to small signal amplifiers. The dividing line between small signal and power amplifiers is a fuzzy one. For example, I used to be very involved with wide dynamic range receiver front ends and when forced to use an RF amplifier might have designed it for over 10 Watts output; yet I considered it a small signal amplifier. On the other hand, I will consider a two Watt intermediate stage in a transmitter chain a power amplifier.

Rather than get bogged down with defining a dividing line, let us say our 50 Watt amplifier is a power amplifier and compare it with small signal amplifiers in the milliwatt range. One apparent difference is the impedance levels brought about by the power level and what this does to the components. For example the input inductor of our example calculates to be 3.2 nH. This is a pretty small inductance and represents a fraction of an inch of PC board trace. When dealing with values this small, simple questions like; where does the transistor tab stop and the inductor begin, become difficult to answer and

Figure 8



SCHEMATIC OF OUTPUT SECTION

cause a little more cut-and-try than we would like. Some people feel that a certain amount of "witchcraft" is involved in the design.

If a fraction of an inch of PC trace is a desired inductor in our circuit, how about the lengths needed just to connect the components together and which don't appear on the schematic?

Amplifier schematics liberally throw ground symbols around, implying that when we see the symbol we can assume there is no voltage at the point. Ha! Our fraction of an inch 3.2 nH represents almost 3 Ohms at 146 MHz. The transistor is delivering power into a 1 Ohm network. It doesn't take much ground length to be a goodly percentage of 1 Ohm. Very careful layout is required and even then the network is going to look different than calculated.

Capacitors act like values different than marked, due to lead inductance. When dealing with the high value capacitors dictated by the impedance levels involved in power amplifiers, leadless constructions like chip capacitors and metal cased micas are what you use. Even so, inductance is a consideration. A Motorola publication[15] estimates the metal cased mica capacitors used in VHF power amps, in the values they were discussing, have 1 to 2 nH in parasitic inductance and gives a formula for calculating an equivalent capacitor which will function as the desired value. The amplifier the author was designing required an 880 pF capacitor and the formula indicated that a 420 pF should be used, because of the effect of parasitic inductance. Hardly a small change!

Another significant design difference between small signal and power amplifiers is in the selection of Q. In small signal amplifiers, it is not uncommon to lower the Q of the output tuned circuits simply by paralleling them with resistors. The power lost by this procedure is generally not a consideration and the stability gained is a plus. This is generally not the procedure used in power amplifiers. If you want a specific Q, you design the network so that the desired Q is obtained with the normal loads.

We will cover more differences as we go, but I want to cover one more difference here, and that is the class of amplifier. Small signal amplifiers generally operate class A and occasionally drive into class AB with large signals. Power amplifiers can operate class A, AB, B or C. There is also a group of high efficiency amplifiers, such as classes D, E, F, G, H, and S which we won't even consider here.

Before briefly discussing the classes of amplifier, note that it wasn't necessary to worry about the class when we designed the output network. Whether operating class A, AB, B, or C our device must still see an impedance determined by the available voltage swing and desired power. I have made this point often today and do so because it is one of the most frequently misunderstood areas of power amplifier design. I will now let it rest.

Well, maybe not quite yet; because, I know some of you are going to go home and pull out the ARRL Radio Amateurs Handbook, that wonderful source of misinformation and oversimplification, and when you look in the section on power amplifier design you will find formulas different than we used. For example, their formula for the load resistance of a transistor amplifier ignores saturation resistance. This can lead to a significant error.

Their vacuum tube formula, as if there should be a difference, uses plate voltage, plate current, and a factor K which depends upon the class of

amplifier. The K is, in reality, a factor that ties in efficiency and if you were to play with the formula you could tie it back to our voltage swing power output formula. If you are designing for a particular power output, you don't need to know the efficiency to calculate the load impedance.

Unfortunately, they also get into that garbage about complex conjugate matching of the souce impedance and confuse the issue before trying to straighten it out. Remember our toaster example!

Now, I'll let it rest. Back to class of amplifier. In case some of you have forgotten, we will re-define the classes.

A Class A amplifier is one whos bias and drive are such that current is flowing for the entire 360° of the drive cycle. If you assume a zero source impedance the theoretical maximum efficiency is 50% at maximum output. Values in the 20% to 35% range are more likely. In a truly linear class A amplifier, the power lost in the device is lowest at maximum output. This is the most linear of the classes and also has the highest gain. Due to low efficiency, Class A is generally confined to low power amplifiers.

A class AB amplifier operates at bias and drive levels so the device is conducting for more than 180° but less than 360° of the drive cycle. The tuned circuits fill in the missing parts of the RF cycle (so called flywheel effect) and Class AB RF amplifiers can be used for linear work, such as required by SSB, and for SSB use Class AB amplifiers are the most commonly used. 50% to 60% efficiencies are not uncommon.

I would like to use this class to poke fun at another popular conception and that is you should always operate an amplifier at less than its designed output power for maximum life. There is some validity to this theory. At lower powers some components are stressed less. (I could tell you a story about disintergrating gate bonding wires in poorly designed FET's except we don't have time, and, secondly, I would probably cry a lot.) However, in general, you maximize the life of an amplifier by keeping the transistor temperatures as low as you can.

Falcon Communications makes a Class AB amplifier that delivers 100 Watts when drawing about 12 Amperes from a 13.8 volt supply. 12 Amps at 13.8 Volts is about 166 Watts and if we are getting 100 Watts out, that means we are losing about 66 Watts in the amplifier. Allowing for a few Watts in the DC wiring, the output matching network, and the output filter, we are losing a little over 60 Watts in the two transistors. If we say that 10 of the 12 Watts drive it takes to get 100 Watts out is also dumped in the transistors, we end up with the transistors having to get rid of a little over 70 Watts of heat when the amplifier is driven to full output.

The quiescent current of this amplifier is 6 Amps. Thus, we have 6 x 13.8 or about 83 Watts of heat to get rid of if we have no drive but are keyed up. Almost all of the 83 Watts is dumped in the transistors. Thus, the transistors will run hotter at no output than they do at full output.

The point of the story is to caution you against blanket generalities.

A Class B amplifier is biased so the device is just cut off. Current, thus, flows for 180° of the drive cycle. 65% efficiency can be achieved. It is reasonably linear.

Although the definition of Class B calls for operation just at cut off, in

practice any amplifier operating near cut off is considered Class B. For example, a bi-polar transistor power amplifier operating with no bias and low base-to-ground DC resistance is generally considered Class B. This would not be a linear amplifier.

A Class C amplifier is biased beyond cut off. Thus, current flows for less, and generally considerably less, than 180° of the input drive cycle. Class C amplifiers have the highest efficiency, approaching 80%, and the lowest gain of the basic classes. They are very non-linear and used for CW, FM and other services where linearity is not important. They also generate the highest level of harmonics.

When applied to vacuum tubes there are sub classes, such as AB_1 and AB_2. The 1 means you never drive the tube hard enough to draw DC grid current, and the 2 means you do.

Class C vacuum tube amplifiers are almost always driven hard enough to draw grid current but the 2 subscript is seldom used.

For some reason, I hear the 1 and 2 subscripts occasionally applied to solid state amplifiers. They have no meaning. With bi-polar transistors you will have DC base current for all classes. If you draw DC gate current in a MOSFET device you had better get your wallet out because you just destroyed it.

The difference in designing for the different classes is primarily one of using knowledge of the conduction angle to be able to calculate the DC current, efficiency and gain. Time prevents going into the specifics. Once again, the topic is well covered in the literature[16,17].

Next, I would like to briefly cover the input matching network. Here, we are primarily performing an impedance matching function. We are transforming the impedance seen looking into the device to some desired impedance. If we are designing a single stage amplifier, the impedance we desire is generally one of the standard system impedances, such as 50 Ohms, 72 Ohms, 100 Ohms, etc. If we are dealing with a multistage amplifier, the input network of one stage is actually the output network of the preceeding stage. We will limit our discussion to single stage amplifiers, and 50 Ohm systems.

The F1260 MOSFET we have selected for our example amplifier has an input impedance whose real part is about 1 Ohm at the 146 MHz we are using in our example. Thus, the input matching network could be very similar to the output network and we won't go through any calculations.

The schematic of a 50 Watt, 2 Meter amplifier we manufacture is shown in Figure 9. We will use this schematic rather than a hypothetical example to finish our discussion of why the schematics look the way they do.

The input network is a double L, consisting of PC trace and L1 as the inductors and C6, C7 and C9, C10 as the capacitors. C5 is a compensating capacitor added to give a wider range of adjustment. C9 and C10 are metal cased micas for low lead inductance. R5 is just a static drain in this amplifier. In others it could be a swamping resistor. The amplifier has a T/R relay and provision to plug in a receive preamplifier.

Bias is applied to the FET through R3. Because no DC current is involved, R3 is large (10K). Again, if swamping is needed for any reason, R3 could be small. Bias comes from a regulated 8 Volt supply turned on at the same time as

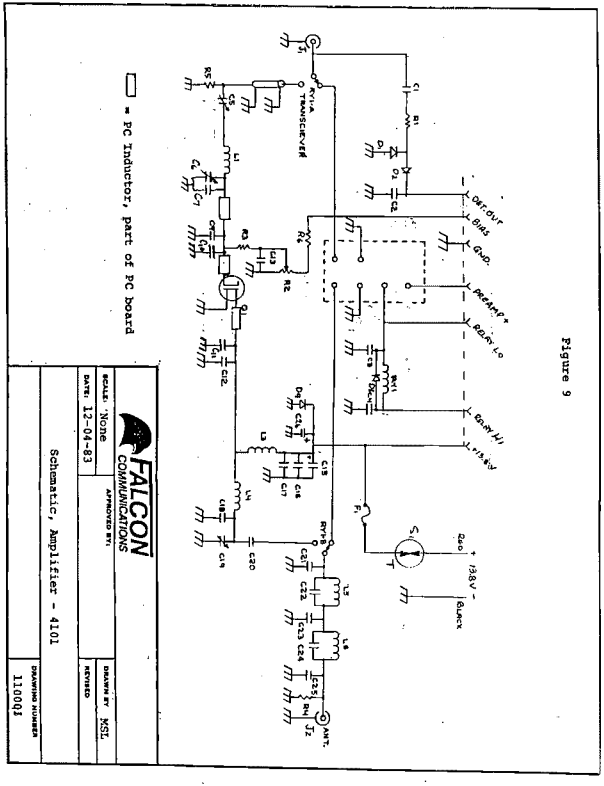


Figure 9

the T/R relay. The output matching network is our familiar double L and I will leave it up to you to find it.

In this amplifier, C20 is simply a d. c. blocking capacitor to keep d. c. out of the antenna. It could easily have been made part of the output matching network.

Following the amplifier is a 2 section "m" derived low pass filter. In this day of modern filter design, using an "m" derived filter may seem a bit archaic. After all the more modern designs do offer sharper roll-offs. Let me defend the choice.

This amplifier is designed as an add-on to a customers transceiver and since we don't know what transceiver might be used we have no way of knowing what frequencies the spurious signals coming out of that transceiver might be located at. Thus, the amplifier designer's task is to design the amplifier for minimum output of any spurious that the amplifier might generate, namely harmonics; with the first, and dominant, one being the second harmonic.

Though the more modern filters can be made to initially roll off steeper, the old "m" derived can put a beautiful notch right where you need it, at 2f. In addition, the efficiency of that notch is less dependendent upon load impedance than the slope of some of the modern filters. The defense rests.

Lets discuss the rest of the components and get on to another example. L3, a choke to feed DC to the transistor, is connected close to Q1 at a low impedance (low voltage) point. L3 is bypassed with four bypass capacitors. Two 470 pF, for high frequency bypassing, a 1 uF, for mid frequency bypassing, and a 1000 uF for low frequency bypassing. The gain of the transistor goes up

significantly as frequency goes down and proper bypassing is necessary to prevent oscillation.

D4 is a reverae voltage protection diode which blows the fuse if the aupply voltage is connected wrong. A less spectacular way to do the job is to connect a diode in aeries with the aupply line. However, lets look back at our example. We aasumed a 13.0 Volt aupply (13.8 Volts running a little low, less the drop in the #12 wire supply lines, less the drop across the fuse) less the 3 Volt saturation voltage; gave us a 10 Volt peak swing. If we add a aeries diode, the 10 Volts goes down another 0.8 Volts or so. This costs power. Hence, the shunt diode.

S1 is a thermostat mounted on the heat sink, which shuts the amplifier down if things get too hot. C1, R1, D1, D2, and C2 form a detector to sense the presence of input RF and turn the amplifier on. R4 is another static drain. The puriats uae a choke here.

There is no temperature compensation in the bias circuit. It is not needed in MOSFET amplifiers of this power level. The amplifier was placed in a temperature chamber and tested over the range of -40 to +60° C. The quiescent current varied only 0.2 Amps across the entire range. Room temperature current was 3 Amps. Current drawn at the 50 Watt point didn't vary significantly.

I think we have stared at this 50 Watt amplifier long enough. How about higher power? The power we can design for is, of course, limited by the available devices. At VHF, using a 13.8 Volt supply, 60 Watts is about where the industry is at with MOSFET devices, and 80 Watts with bipolar devices. At higher supply voltages 150 Watts is obtainable. At low frequencies, Motorola has the grand-daddy of them all. A MOSFET device delivering 600 Watts up to 100 MHz. As frequency goes up, power comes down, with 50 Watts being about the limit at 450 MHz. 120 Watts at 500MHz is available in push-pull packages.

If we want more power we have to use multiple devices connected together. One technique is to use a group of lower power amplifiers and combine their output in combining networks. Combining networks[18,19] are a topic unto themselves and we won't go into them here. Let me simply say that in practice they are more complex than you would be led to believe by the simplified discussion in the texts. We will simply look at devices connected in parallel and push-pull. First parallel.

Lets say we want an amplifier that will deliver 150 Watts at 146 MHz and use a 13.0 Volt supply. Lets use a pair of bi-polar devices, the MRF247, and assume the saturation voltage is 2 Volts.

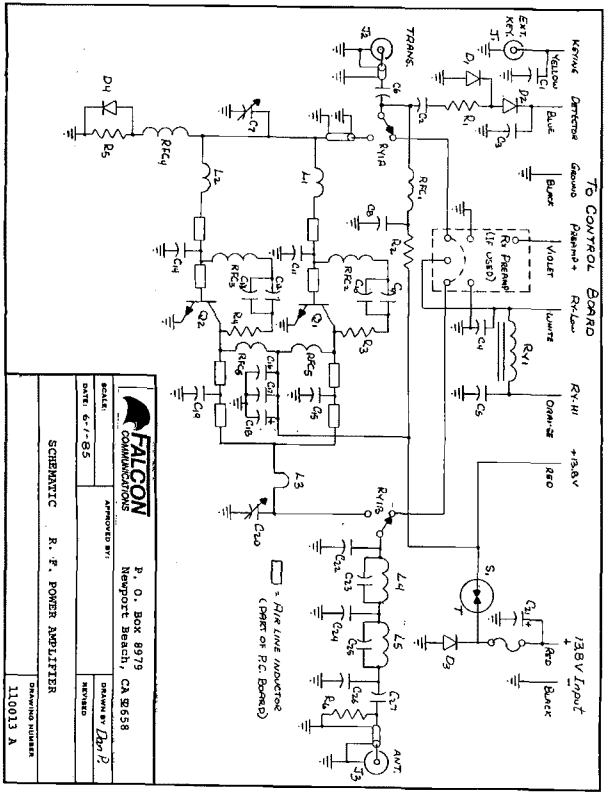
Going back to our reliable formula for load impedance we find that the transistors must see:

$$R_L = \frac{(E_{supply} - E_{sat})^2}{2P} = \frac{(13-2)^2}{2 \cdot 150} = 0.4\,\Omega \qquad 13)$$

This is a low impedance and trying to get two transistors tied together such that the impedance in the connecting lines is a small fraction of this is almost impossible.

The trick is to tie them together at a higher impedance point and then use matching networks for the individual transistors to get to a lower impedance. This has a number of advantages, not the least of which is that it works, and the networks allow some physical separation between the transistors.

Figure 10 is the schematic of a Falcon 150 Watt 2 Meter amplifier using



this technique. You will see many similarities with the previous amplifier: low pass filter in the output, T/R relay, pre-amp provision, etc. The big difference is that there are now two transistors. If you will look at the collector of one of the transistors, you will see we have an L section and part of a second before we parallel with the other transistor. Looking at the input reveals a similar situation. Thats really all there is to it.

Not seen on the schematic is some circuitry internal to the transistor. The input impedance of large bi-polar RF power transistors is very low at these frequencies, so low as to make matching difficult. The manufacturers, thus, very kindly build matching networks into the transistor to raise the input impedance to a workable level. THe MRF247 has a T network consisting of the inductance of the bonding wires and a built-in MOS capacitor in the input of each of the eight cells that make up the device. Even with the internal matching the input impedance is low. The MRF247, in our application, has a series equivalent input impedance of 0.45 +J 0.85 Ohms.

You lose some potential power capability parallelling transistors because there is no guarantee that the two transistors are carrying an equal share of the load and the one carrying the greatest amount becomes the limiting factor. There are a number of things that help. One is to use transistors in matched pairs. Some companies do, some don't. You could also make some of the non common network elements variable. We don't do either on this model; but we do occasionally add a fixed capacitor across one of the transistors when we sense an inbalance in test.

The gain of bi-polar transistors increases much more than MOSFETs as

frequency goes down. This results in a great tendency to oscillate at low frequencies. RFC2, C9, C10, R3 and RFC3, C12, C13, R4 form feedback loops that keep the low frequency gain down. Because we are dealing with bi-polar transistors, which require bias current, our bias supply needs to be low impedance. Also, because of the well known variations of bias requirements with temperature, the bias voltage must vary with temperature.

The bias is the voltage developed across D4, which receives its current through R2, RFC1, RY1a, and RFC4. R5 is a factory adjust to set up the desired quiescent current. If the diode can be considered to be at the same temperature as the transistor this type of bias tracks reasonably well. Some of the tricks used are to use a stud mounted diode mounted on the heat sink, near the transistors, or to mount the diode right on the transistor. We don't do either. The diode is simply a 1N4001 mounted on the PC board.

This simple bias scheme is definitely a compromise. The normal bias stabilization methods used at low power require a DC resistance in either the collector or emitter circuits. Sufficient resistance to effectively stabilize the quiescent would consume a great deal of power and, when we are operating at a low supply voltage, waste enough voltage as to make getting our desired power output difficult. In addition, we don't want to lift the emitter off of ground for RF reasons. Keeping it at an RF ground is difficult enough. They didn't put four emitter tabs on the MRF247 for the fun of it.

There is some help on bias stability built into the transistor. The device is in reality many transistors internally connected in parallel. To prevent current hogging, hot spots and a number of other nasty problems, the manufacturer adds a small resistance in the emitter of each of these many transistors. If you are not familiar with the term, this is known as "emitter ballasting".

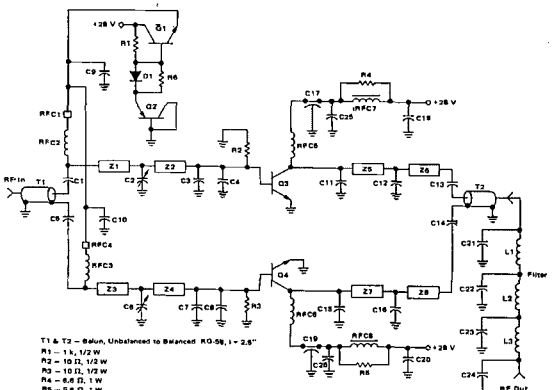
There is an additional problem with our simple bias scheme. The input RF is rectified by the transistor base-emitter junction, creating a current opposing the bias current. If the bias source is not stiff enough this can bias you toward Class B, or even C, with the attendant loss of linearity and gain. In the amplifier under review, R2 is 50 Ohms and R5 typically about 2 Ohms and we can still lose about 20% in power gain under some circumstances. It is also important that RFC4 have a low DC resistance.

The final schematic we will take a look at is of a push-pull amplifier. Because we do not make a push-pull amplifier, I have borrowed a schematic from a Motorola Engineering Bulletin[20]. It is shown in Figure 11.

Push-pull at RF is not different in principle from push-pull at audio. You take the input signal and produce two signals 180° out of phase and apply them to two amplifying devices. The two resulting 180° out of phase output signals are combined in a transformer or other device to give the output.

At HF the 180° signals are generally generated and combined with physically identifiable transformers. Years ago, these were generally air cored transformers. Today, toroidal cored transformers are common. For wide bandwidth, the so called transmission line transformer on a toroidal core is common. At VHF and UHF, wound transformers are impractical and baluns made out of lengths of coaxial cable are common. That is what is used in this 420-450 MHz amplifier (T1 and T2). First note that they used matching networks to

Figure 11



T1 & T2 – Balun, Unbalanced to Balanced RG-58, l = 2.8"
R1 – 1 k, 1/2 W
R2 – 10 Ω, 1/2 W
R3 – 10 Ω, 1/2 W
R4 – 6.8 Ω, 1 W
R5 – 9.8 Ω, 1 W
R6 – 2.7 Ω, 1/4 W
Z1 & Z3 – Microstrip – W = 200 mils, l = 1.8"
Z2 & Z4 – Microstrip – W = 200 mils, l = 300 mils
Z5 & Z8 – Microstrip – W = 150 mils, l = 300 mils
Z6 & Z8 – Microstrip – W = 150 mils, l = 1.4"
RFC1, 4 – Ferrocube Bead 56-590-65-3B
RFC2,3 – 0.18 μH Cambion Molded Coil
RFC5, 6 – 1 Turn #20 Enamaled Wire Wound on 6/16" Bolt
RFC7, 8 – VK-200 20/4B
C1, 3, 4, 5, 6, 11, 15 – Underwood 40 pF
C12, 16 – Underwood 25 pF
C19, 14, 22, 23 – Underwood 16 pF
C9, 10, 18, 20 – 1 μF Tantalum
C21, 24 – Underwood 10 pF
C2, 8 – Arco 403
C17, 19 – Underwood J102, 1000 pF Feed Thru
C25, 26 – 0.1 μF, Erie Red Cap
L1 – 24 nH, #14 Wire, l = 1.2"
L2 – 12 nH, #14 Wire, l = 0.8"
L3 – 24 nH, #14 Wire, l = 1.2"
Board – Q10, εR = 5, t = 0.062", l = 8.0", W = 4.0"
Q1 – 2N5192
Q2 – 2N5194
Q3 – MRF309
Q4 – MRF309
D1 – 1N4001

100 WATT 420-450 MHz PUSH-PULL AMPLIFIER

build the impedances up to workable levels before doing any combining. Second, notice the bias circuit (Q1, Q2, D1). This arrangement gives you a stiff source, without as high a DC power loss as was necessary with the simple diode arrangement of the previous schematic.

Some advantages of the push-pull configuration, compared to using two devices in parallel, are:

1) Easier input and output matching due to higher impedance levels.

2) Suppression of even harmonics. This is the classic advantage cited for push-pull stages. However, there are some traps. For example, if in a Class C stage you have capacitive coupling between each device and the output, you may find that the second harmonic is much higher than in the equivalent single ended stage.

3) Collector by-passing is less critical. This is true but don't get carried away.

4) Emitter grounding is less critical. In a push-pull stage it is the emitter-to-emitter path that is more important than the emitter-to-ground path. If you mount the two devices in the same package, where the emitter-to-emitter leads can be real short you can reduce problems considerably. The push-pull package is becoming more common in VHF and UHF devices.

5) The load sharing is better than the equivalent two devices in parallel.

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END

AN EVOLUTION OF OPTIMIZATION AND SYNTHESIS PROGRAMS FOR PERSONAL COMPUTERS

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ABSTRACT

Two personal-computer programs for RF/microwave applications - CIAO for analysis and optimization, and DESIGN for matching network synthesis - have undergone substantial revision since their introduction over a year ago. CIAO is now a much more powerful program, with the inclusion of rapid sparse-matrix techniques, a choice of three different optimization algorithms, and high resolution graphics output. DESIGN has a greatly improved user interface and, with the inclusion of a fine-tuning option, is now able to consistently synthesize lumped and distributed matching networks with response errors on the order of a small fraction of a dB. This paper discusses the evolution of CIAO and DESIGN to their present states.

I. INTRODUCTION

CIAO: Circuit Analysis and Optimization on Personal Computers

CIAO, a program for MS-DOS and CP/M personal computers, performs the analysis and optimization of microwave and RF networks in the frequency domain. The initial version of the program was first demonstrated at RF Technology Expo '85 [1]. Since that time, a number of features have been added to the program, significantly improving its capabilities and performance. After a brief review of the original CIAO, we shall present a discussion of the evolution of CIAO to its current state. A circuit optimization example will illustrate the many benefits of CIAO's upgrading.

DESIGN: Automated Matching Network Design on Personal Computers

After the discusaion of CIAO, we shall present the newest version of DESIGN, a program for performing the automated synthesis of lumped and distributed matching networks between real sources and complex loads. DESIGN has been improved over its previous release [1] by enhancing the user interface and by adding a fine-tuning option, which enables virtually all matching network designs to meet specifications to within a small fraction of a dB. An example will illustrate the capabilities of the new DESIGN.

II. The Evolution of CIAO

The Capabilities of CIAO: Original Version

CIAO can analyze and optimize circuits comprising the following elements: resistors; capacitors; inductors; (lossy) transmission lines; controlled sources (with delay); one-ports, two-ports and three-ports described by tables of S, Y, or Z parameters; and gyrators. Scattering parameters for the circuit are calculated between either real or complex loads over a frequency band. The magnitude, phase, and/or phase-shape of any number of the S-parameters may be optimized to achieve specified design goals. Generally, for optimization, new sets of element values are found to minimize the error between the calculated and desired S-parameter values.

In the original version of CIAO, the Fletcher-Reeves [2] gradient optimizer was available, highly efficient and accurate adjoint techniques [3] were used to calculate the gradients required by the optimizer, and a "dense" linear equation solver was used in the analysis routines. There was no graphics output. The new CIAO offers a choice of three optimizers, a sparse matrix solver, and simultaneous text and high resolution graphics on a single screen. The benefits of these additions will now be described.

The New CIAO: Three Available Optimizers

CIAO now offers a choice of two gradient algorithms and one random-grid algorithm for circuit optimization. For a given network problem, one method will prove superior to the others; sometimes the best results can be achieved

by applying one algorithm and then switching to another.

The available gradient optimizers are the Fletcher-Reeves (F-R) and Fletcher-Powell (F-P) [4] methods. Both of these use information obtained from the gradient of the error function to search for the minimum. When far from a minimum, F-R and F-P both behave like a steepest-descent method and converge at about the same rate. When close to a minimum, F-P converges faster than F-R because F-P starts acting more like a Newton-Raphson method, which has a quadratic rate of convergence. These properties of the F-R and F-P methods apply exactly only to functions with "locally quadratic" behavior. In practical circuit problems, the error function may or may not have this characteristic. Experience has shown us, however, that F-P is usually superior to F-R, although there are instances where F-R does work better.

CIAO also provides the choice of the Nelder-Mead (N-M) [5] random-grid-search method. In this algorithm, the error function is evaluated several times for a range of element values - i.e. over a "grid" in the vector space of optimizable element values - and from this a "better" set of circuit parameters is deduced. N-M, like most random-grid methods, is generally able to avoid convergence to local minima, although sometimes the number of function evaluations required becomes large. The algorithm is also very effective in those circuit problems where the response is not too sensitive to small changes in the network parameters. Such a situation arises, for example, when optimizing the passband of a lossless, doubly-terminated filter or matching network. This is so because the first-order sensitivity of S21 to the component values of such a network is zero at frequencies corresponding to maximum transfer of power between the source and load [6].

CIAO, with its three optimizers, provides sufficient flexibility to handle the most difficult circuit optimization problems.

The New CIAO: Sparse Matrix Techniques

Both the analysis and optimization performed in CIAO involve repeatedly constructing and solving the linear nodal equations of a circuit to obtain scattering parameters. The conventional means of solving linear equations, such as Gaussian elimination or LU factorization, generally requires a number of mathematical operations proportional to n^3, i.e. the cube of the number of nodes in the circuit. Many of these mathematical operations involve multiplications by zero, because the typical nodal admittance matrix Y is sparse, i.e. contains only a small percentage of nonzero entries. For example, the percentage density of nonzero entries in Y for a ten-node ladder network is 28%, while for a twenty-node ladder the density falls to under 15%. Clearly, if the useless multiplications by zero were eliminated in solving the linear equations, a great increase in processing speed would be realized.

Sparse matrix techniques consist of specialized algorithms for solving linear equations by working only on the nonzero entries of the coefficient matrix. For typical nodal equations, the number of mathematical operations required for solution is linearly proportional to n, the number of nodes. Obviously, an enormous saving in processing time is realized by using sparse

matrix methods in circuit analysis and optimization.

CIAO now employs a sophisticated sparse matrix equation-solving algorithm, and the resulting increase in processing speed has been impressive, as compared to the original CIAO, which used the conventional "dense" solver. For example, with the sparse solver, the analysis and optimization speeds for various ladder networks improved as follows: (1) four-node network - ran 1.04 times faster; (2) ten-node network - ran twice as fast; (3) twenty-one node network - ran ten times faster. Generally, the larger and sparser the network, the greater will be the advantage that sparse matrix techniques realize over dense solvers.

The New CIAO: Graphics Output and Other Enhancements

CIAO's normal screen-output mode now provides simultaneous text and high-resolution graphics output. In CIAO's graphics mode, which is the default option, the upper half of the screen displays the text output. This consists of the program queries directed to the user, and the analysis and optimization results for the circuit. The user may redirect this text output to the printer. The graphics output from CIAO appears in the bottom half of the screen.

The graphics output is generated automatically by CIAO according to certain default options. By including the appropriate command in the data file, the user may override the defaults either to plot the magnitude or phase of any scattering parameter, or to suppress graphics output altogether. When the graphics mode is activated, a plot is generated for the initial analysis of the circuit and for each optimizing iteration after the initial analysis. After three plots are constructed on the coordinate axes, the graph is erased and a new set of axes is constructed, possibly with a different ordinate scale. As the iterations proceed, another three plots are drawn. At this point, the graph is refreshed again. The process repeats until the desired number of iterations is completed. Each plot of a group of three is distinguishable by the intensity of the trace on the screen, and by either dot, cross, or box marks on the plot at the frequency points specified in the data file.

Hardcopy output of the screen's graphics images is possible via the GRAPHICS.COM program, which comes with most MS-DOS 2.x operating systems. Before running CIAO, one need only execute GRAPHICS.COM; then at any time during or after a CIAO execution, Shift-PrtSc will dump the screen image to the printer.

Automatic Updating of Data Files. Whenever an optimization is concluded or interrupted, the user may, in response to screen query, direct CIAO to save to disk a new data file with the current values of the optimizable circuit elements. This feature makes it very easy to start, stop, and resume an optimization of a circuit - even changing the optimization algorithm along the way, if so desired.

Improved Interrupt Handling. CIAO's analysis and optimization maybe interrupted instantly by holding down any key. Execution may be then terminated with a final analysis or continued, as desired.

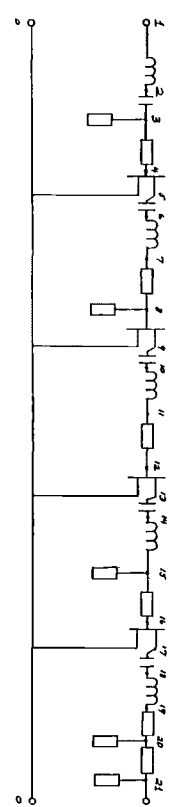
III. An Optimization Example for the New CIAO

Presented below are a data file, circuit diagram, and partial program output for an optimization example run using the new CIAO. The data file contains comments which explain the optimization process for the circuit. (Comment lines are denoted by an apostrophe being the first character on the line; blank lines are also allowed. CIAO also permits text comments to be appended to any line.) The circuit is described in a nodal-interconnect format and the optimizable parameters are denoted by an asterisk appended to the element codes.

```
'   CIAO DATA FILE:  OPTIMIZATION OF A FOUR-STAGE GaAs FET AMPLIFIER
'   ---- ---- ----  ---------- -- - ---- ---- ---- --- ---------

'CIAO is used here to optimize a four-stage, 21-node amplifier to
'(1) a prescribed S11 magnitude and phase (for noise figure), (2)
'a flat 30 dB gain for S21, and (3) an S22 magnitude of below
'0.20.  The initial design of the amplifier displays a
'satisfactory match for S22, a poor match for S11, and a maximum
'gain error for S21 of 4.3 dB.  The optimized design still
'displays a satisfactory match for S22, a greatly improved match
'for S11, and a maximum gain error for S21 of 0.4 dB.

'The optimization was stopped after 4 Nelder-Mead iterations,
'which required a total of 91 function evaluations.  In this
'particular example, neither Fletcher-Powell nor Fletcher-Reeves
'alone is able to achieve results anywhere nearly as good as those
'achieved with Nelder-Mead.

'       TYPE of OPTIMIZATION:  Nelder-Mead
'       RUN-TIME for the INITIAL ANALYSIS:  2.1 sec. per frequency point
'       TOTAL RUN-TIME for ITR. 0 - 4  (91 fn. eval.):  19 min. 11 sec.

'Using the dense solver of the original CIAO, the above run-times
'increase by a factor of TEN.
'- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -

ind 1 2 .05e-9
cap 2 3 8.2e-12
   'For trl, ost: Zo, Length (deg.) Freq.

trl_* 3 0 4 0      50  69.48          7.5e9
ost_* 3 0 50 49.72 7.5e9
two 4 0 5 0 table1

cap 5 6 8.2e-12
ind 6 7 .05e-9
trl_* 7 0 8 0 50 75.6 7.5e9
ost_* 8 0 50 43.3 7.5e9
two 8 0 9 0 table2

cap 9 10 8.2e-12
ind 10 11 .05e-9
trl_* 11 0 12 0 50 61.98 7.5e9
two 12 0 13 0 table3

cap 13 14 8.2e-12
ind 14 15 .05e-9
ost_* 15 0 50 59.33 7.5e9
trl_* 15 0 16 0 50 31.43 7.5e9
two 16 0 17 0 table3

cap 17 18 8.2e-12
ind 18 19 .05e-9
trl_* 19 0 20 0 50 48.24 7.65e9
ost_* 20 0 50 50.89 7.65e9
trl_* 20 0 21 0 50 57.24 7.65e9
ost_* 21 0 50 21.31 7.65e9

port1 1 0 50
port2 21 0 50
perform twoport optimization table9
'Optimization goal: match circuit S-Parameters to those of table 9
end

'frequencies                Mag./Phase weights for Sij
7.250e9 7.750e9  0.1e9  \  645.2/.1  0  1/0  10e4/0.,0.2/0
end

table1 sparam (first device)
50  (Reference impedance for S parameters)
.79 -137  .04 33  1.50 59  .75 -74
.79 -139  .04 34  1.48 58  .76 -76
.79 -139  .04 35  1.45 57  .76 -77
.79 -140  .04 36  1.42 57  .77 -78
.79 -141  .03 37  1.39 56  .77 -79
.79 -142  .03 38  1.37 55  .78 -81

table2 sparam (second device)
50
.78 -135  .03 68  1.88 59  .75 -81
.78 -136  .03 70  1.84 58  .76 -82
.78 -137  .03 72  1.80 57  .76 -83
```

```
.78 -138  .03 74  1.77 57  .77 -85
.79 -139  .03 75  1.74 56  .77 -86
.79 -140  .03 77  1.70 55  .78 -87

table3 sparam  (third and fourth devices)
50
.78 -147  .155 -37.6  1.14 -33.0  .76 -129
.78 -148  .157 -43.8  1.13 -34.9  .76 -130
.78 -149  .158 -49.7  1.11 -36.7  .76 -130
.78 -150  .159 -55.4  1.10 -38.5  .76 -131
.78 -151  .160 -60.9  1.09 -40.2  .76 -132
.78 -152  .160 -66.1  1.07 -41.9  .76 -133

table9 sparam  (optimizing table)
'match s11 for noise figure; s21 for 30dB gain; s22 for min. value
.86 -19  0 0  31.622 0  0 0
.89 -29  0 0  31.622 0  0 0
.90 -39  0 0  31.622 0  0 0
.91 -47  0 0  31.622 0  0 0
.87 -54  0 0  31.622 0  0 0
.86 -62  0 0  31.622 0  0 0
end
'- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

The circuit diagram and (partial) program output are given on the next two pages.



CMW Example: 4-Stage GaAs FET Amplifier

CIAO Output for 4-Stage Amplifier Example

CIRCUIT ANALYSIS and OPTIMIZATION PROGRAM

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Initial Analysis

Freq. (Hz)	S11 Mag.	S11 Ang.	S12 Mag.	S12 Ang.	S21 Mag.	S21 Ang.	S22 Mag.	S22 Ang.	S21 dB	K Fact
7.250E+009	0.78	-36	-67.8dB	-58.5	51.934	-32.3	0.08	-66	34.3	9.1
7.350E+009	0.76	-45	-68.5dB	-90.5	44.087	-60.7	0.11	-59	32.9	12.6
7.450E+009	0.74	-49	-69.5dB	-116.9	36.102	-83.9	0.10	-66	31.2	18.5
7.550E+009	0.74	-55	-70.3dB	-145.3	30.748	-107.5	0.07	-87	29.8	24.2
7.650E+009	0.73	-57	-73.7dB	-171.5	25.733	-130.1	0.01	-114	28.2	43.6
7.750E+009	0.74	-62	-75.0dB	163.0	20.689	-153.6	0.07	57	26.3	60.1

Iteration number: 0 - using 1 function evaluation(s).
Error function: 147.877

Magnitude errors [11,12,21,22]: 1.20E+001 0.00E+000 1.24E+002 0.00E+000
Phase errors [11,12,21,22]: 1.20E+001 0.00E+000 0.00E+000 0.00E+000

Variable	Value
1	4.97200E+001
2	6.94800E+001
3	7.56000E+001
4	4.33000E+001
5	6.19800E+001
6	5.93300E+001
7	3.14300E+001
8	4.82400E+001
9	5.08900E+001
10	5.72400E+001
11	2.13100E+001

Iteration number: 1 - using 28 function evaluation(s).
Error function: 90.539

Magnitude errors [11,12,21,22]: 1.47E+000 0.00E+000 8.03E+001 5.04E-001
Phase errors [11,12,21,22]: 8.23E+000 0.00E+000 0.00E+000 0.00E+000

Variable	Value
1	4.65707E+001
2	7.47423E+001
3	6.98742E+001
4	4.65794E+001
5	5.96321E+001
6	5.75146E+001
7	3.50699E+001
8	5.09605E+001
9	4.91413E+001
10	6.15752E+001
11	1.96960E+001

CIAO Output (cont'd)

Iteration number: 2 - using 9 function evaluation(s).
Error function: 6.292

Iteration number: 3 - using 51 function evaluation(s).
Error function: 4.938

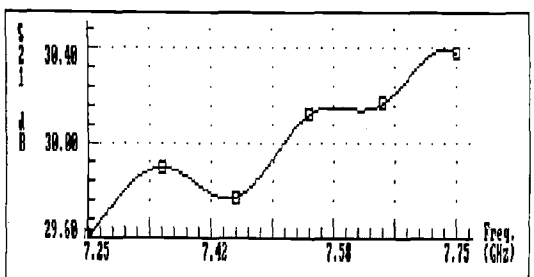
Iteration number: 4 - using 2 function evaluation(s).
Error function: 4.281

Magnitude errors [11,12,21,22]: 5.04E-001 0.00E+000 8.80E-001 0.00E+000
Phase errors [11,12,21,22]: 2.90E+000 0.00E+000 0.00E+000 0.00E+000

Variable	Value
1	4.68837E+001
2	7.71597E+001
3	5.97823E+001
4	4.47366E+001
5	5.52477E+001
6	5.71373E+001
7	3.31566E+001
8	5.31364E+001
9	5.30837E+001
10	5.39265E+001
11	2.40746E+001

Final Analysis

Freq. (Hz)	S11 Mag.	S11 Ang.	S12 Mag.	S12 Ang.	S21 Mag.	S21 Ang.	S22 Mag.	S22 Ang.	S21 dB	K Fact
7.250E+009	0.86	-28	-72.5dB	10.9	30.217	37.1	0.15	156	29.6	17.7
7.350E+009	0.89	-37	-71.5dB	-13.5	31.259	16.3	0.07	95	29.9	12.5
7.450E+009	0.91	-43	-70.8dB	-37.7	30.810	-4.7	0.08	10	29.8	10.0
7.550E+009	0.93	-49	-69.9dB	-63.0	32.078	-25.2	0.13	-33	30.1	6.7
7.650E+009	0.90	-56	-71.8dB	-89.0	32.238	-47.6	0.16	-57	30.2	10.7
7.750E+009	0.92	-62	-70.9dB	-117.9	33.011	-74.5	0.17	-77	30.4	8.0



IV. The Evolution of DESIGN

The Capabilities of DESIGN: Original Version

DESIGN synthesizes lossless lumped and distributed matching networks to provide a specified S21 magnitude response between a real source and a complex load impedance. The method is discussed in [1] and is based on the work of Carlin and Komiak [7]. The most important advantages of DESIGN are: (1) no equivalent circuit models need be constructed for the source and load - only a simple numerical description of the source and load is required as data for the synthesis; (2) the designs are "simpler in structure and superior in frequency response to [classical] equiripple designs" [8]; and (3) no parasitic absorptions or Norton/Kuroda transformations are required in the synthesis.

The original DESIGN was generally able to synthesize networks that were at most a few dB within the S21 requirements across the frequency band. In any event, the response was close enough to specifications to enable a circuit optimizer (such as CIAO) to reduce the error to a small value. The new DESIGN has enhancements which eliminates the need for such optimization after the synthesis.

The New DESIGN

DESIGN now has an internal fine-tuning option, as well as certain algorithmic enhancements, which enable the program, by itself, to design its networks with response errors not exceeding a small fraction of a dB. The fine-tuning option is actually a special purpose optimizer that has been built into the program. The other enhancements mainly involve the proper initial selection of the network topology to guarantee the success of the synthesis for all choices of the source and load. Finally, the user interface has been improved.

The example which follows will illustrate the new DESIGN's ease of use and excellent accuracy in synthesizing matching networks.

V. A Synthesis Example for the New DESIGN

We first summarize below the requirements for the matching network to be designed. This is followed by a statement concerning the options used in the DESIGN program. The user must select an appropriate value for the network degree; DESIGN suggests values for the other options. (Most often the defaults suffice.) Then the results of the synthesis are presented before and after the fine-tuning optimization. Finally, a copy of the actual printout of the program is given, along with a schematic of the networks and a plot of the frequency response.

MATCHING NETWORK DESIGN REQUIREMENTS

- Device Considered: Raytheon RLC832 Low Noise GaAs FET - Matching S11 to 50 ohms for maximum unilateral transducer gain
- Source Impedance: 50 ohms
- Number of Frequency Points: 5
- Load Description: Reflection coefficient with 50 ohm reference resistance

Frequency (GHz)	Load (Refl. Coef.) magnitude	phase-deg	Desired S21 Magnitude of Matching Network	
6.0	.78	-89	0.578	(-4.76 dB)
7.0	.75	-103	0.659	(-3.62 dB)
8.0	.73	-117	0.746	(-2.55 dB)
9.0	.70	-131	0.865	(-1.26 dB)
10.0	.67	-144	1.000	(0.00 dB)

OPTIONS SELECTED in DESIGN DATA INPUT

- Desired degree of matching network: ----- 5
- Bandpass or Lowpass matching network structure: ----- L
- Defaults used for all other options.

DESIGN RESULTS: (Preliminary, before fine-tuning)

- Lumped Circuit, S21 matched across frequency band to within 0.40 dB
- Distributed Circuit, S21 matched across band to within 0.48 dB

DESIGN RESULTS: (Final, after fine-tuning)

- Lumped Circuit, S21 matched across frequency band to within 0.06 dB
- Distributed Circuit, S21 matched across band to within 0.07 dB

The next few pages contain a condensed version of DESIGN's printout, the circuit schematics, and a frequency response plot.

DESIGN Output for Matching Network Design Example

```
MATCHING NETWORK DESIGN PROGRAM

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Degree of network to be designed:  5
Source resistance (ohms): 5.00E+001

Load Frequencies (Hz)          Magnitude   Angle      Desired |S21| (mag)
 6.000E+009                    7.80E-001   -89.0            0.578
 7.000E+009                    7.50E-001   -103.0           0.659
 8.000E+009                    7.30E-001   -117.0           0.746
 9.000E+009                    7.00E-001   -131.0           0.865
 1.000E+010                    6.70E-001   -144.0           1.000

MATCHING NETWORK DESIGN BEGINS:   The Resistance Excursion Optimization

          ... hold down any key to interrupt optimization ...

Iteration     Function Evaluations     RMS % Error of |S21|**2 Across Passband
    0                 1                        62.589
    1                 5                        10.263
    2                 3                         3.886
Error function has changed by less than 0.50 percent.
Do you wish to continue optimization?  (Y/N): y

Optimization continues ...

    3             2                          3.886
    4             1                          3.684
    5             2                          3.450
    6             2                          3.325
    7             1                          3.176
    8             2                          3.163
Error function has changed by less than 0.35 percent.
Do you wish to continue optimization?  (Y/N): n

RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE   50 OHM SOURCE
                TO THE COMPLEX-LOAD.

  The Lumped Element Design              The Distributed Element Design

Series Inductor: 2.299E-010 H      TRL: 120.0 ohms,   5.53 deg at 8.000E+009 Hz
Shunt Capacitor: 3.726E-013 F      OST:  25.0 ohms,  25.09 deg at 8.000E+009 Hz
Series Inductor: 8.046E-010 H      TRL: 120.0 ohms,  19.78 deg at 8.000E+009 Hz
Shunt Capacitor: 7.328E-013 F      OST:  25.0 ohms,  42.64 deg at 8.000E+009 Hz
Series Inductor: 5.514E-010 H      TRL: 120.0 ohms,  13.35 deg at 8.000E+009 Hz

   A circuit analysis follows ...

Freq. (Hz)    S21 in dB:   Desired    Lumped Design    Distributed Design
----                       -------    -------------    ------------------
6.000E+009                   -4.76        -5.16             -4.94
7.000E+009                   -3.62        -3.68             -3.46
8.000E+009                   -2.55        -2.26             -2.07
9.000E+009                   -1.26        -1.08             -0.86
1.000E+010                    0.00        -0.29             -0.07
```
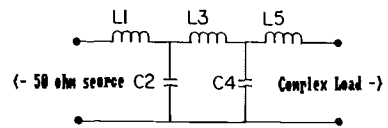

Design Output for Matching Network Design Example (cont'd)

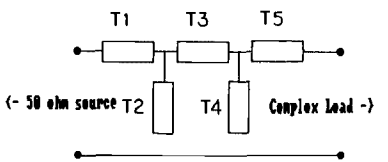
```
Optimize the (L)umped or (D)istributed design or (Q)uit - (L/D/Q): l
Optimization proceeds - hold down any key to stop ...

        Function Evaluation No.:   82

 Maximum Response Error in dB (=  0.86

Design refinemsnt completed - hit (cr) to continue ...

RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE   50 OHM SOURCE
                TO THE COMPLEX-LOAD.

  The Lumped Element Design

Series Inductor: 2.129E-010 H        A circuit analysis follows ...
Shunt Capacitor: 3.757E-013 F
Series Inductor: 1.881E-009 H   Freq. (Hz)   S21 in dB:  Desired    Lumped Design
Shunt Capacitor: 7.858E-013 F   ----                    -------    -------------
Series Inductor: 6.554E-010 H   6.000E+009                -4.76        -4.77
                                7.000E+009                -3.62        -3.61
                                8.000E+009                -2.55        -2.54
                                9.000E+009                -1.26        -1.28
                                1.000E+010                 0.00        -0.06

Optimize the (D)istributed design or (Q)uit - (D/Q): d
Optimization proceeds - hold down any key to stop ...

        Function Evaluation No.:   94

 Maximum Response Error in dB (=  0.07

Design refinement completed - hit (cr) to continue ...

RESULTS: MATCHING NETWORK ELEMENT VALUES FROM THE   50 OHM SOURCE
                TO THE COMPLEX-LOAD.

                The Distributed Element Design

                TRL: 120.0 ohms,   5.22 deg at 8.000E+009 Hz
                OST:  25.0 ohms,  23.76 deg at 8.000E+009 Hz
                TRL: 120.0 ohms,  22.98 deg at 8.000E+009 Hz
                OST:  25.0 ohms,  43.20 deg at 8.000E+009 Hz
                TRL: 120.0 ohms,  13.84 deg at 8.000E+009 Hz

  A circuit analysis follows ...

Freq. (Hz)    S21 in dB:  Desired    Distributed Design
----                      -------    ------------------
6.000E+009                -4.76        -4.83
7.000E+009                -3.62        -3.61
8.000E+009                -2.55        -2.49
9.000E+009                -1.26        -1.28
1.000E+010                 0.00        -0.07
```

Lumped Matching Network from DESIGN



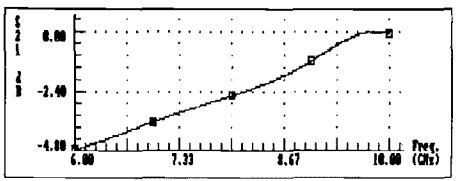
L1: 2.129e-10 H
C2: 3.757e-13 F
L3: 1.881e-09 H
C4: 7.858e-13 F
L5: 6.554e-10 H

Distributed Matching Network from DESIGN



T1: 120 ohms, 5.22 deg @ 8 GHz
T2 25 ohms, 23.76 deg @ 8 GHz
T3: 120 ohms, 22.98 deg @ 8 GHz
T4: 25 ohms, 43.20 deg @ 8 GHz
T5: 120 ohms, 13.84 deg @ 8 GHz

Lumped and Distributed Frequency Response is Coincident with Desired S21 Shape



VI. Conclusion

The evolution of two programs for RF and microwave circuit analysis, optimization, and synthesis has been presented. We expect to continue to improve CIAO and DESIGN to include additional features and speed enhancements.

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"THE POOR MAN'S ENGINEERING WORK STATION"
or
"CHEAP CAD"

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THE POOR MAN'S ENGINEERING WORK STATION

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INTRODUCTION

The current literature is full of discussion of the new "Engineering Work Station" or facilities for Computer-Aided Design (CAD). The working RF design engineer reads of these devices with great anticipation, but soon realizes that these are beyond the normal means of a limited personal or engineering budget. Terms like "silicon compiler" and "gate array design" and "standard cells" are resplendent in the literature. Most working engineers probably will not design integrated circuits or semicustom integrated circuits. The purpose of this paper is to show that the working-level RF design engineer, on a limited budget, can provide an effective facility to simplify his engineering duties.

As a practical matter, few companies are going to allocate tens of thousands of dollars to individual engineers unless an immediate increase in productivity can be shown. It has been my experience that if a computer is not immediately available it loses a great deal of its functionality. If we have to sign up or go across the hall (or across the plant!) to use a computer, we are likely not to bother, and either rely on our experience or just "SWAG" it. Since most companies are unwilling or unable to supply a personal computer to each working engineer who desires one, it is up to each of us to provide our own computational resources, just as we did with slide rules and calculators. This paper will show how to use the "low end" home and personal

computers to accomplish most of the computational tasks that are required. By using our experience and intelligence in an interactive manner, we can reduce significantly our design "work load" and produce better products in less time.

SOME DEFINITIONS:

Engineering workstation: A collection of equipment that allows the engineer to design and test circuits. For the purpose of this paper, the engineering workstation is a computer-equipped location where a design engineer will spend a significant portion of his work day.

Personal computer: A computer that is immediately available to an individual, of fairly low cost and relatively low processing power. This paper shall be limited to those computers that fall within the normal range of discretionary income for individuals, in general less that two thousand dollars.

Working engineer: The engineer whose primary task is to produce designs. This is the individual who does not have significant personnel or programmatic management duties.

HARDWARE:

For purposes of comparision, lets see what hardware might be availble to accomplish our needs. Just as most of us have some form of personal transportation, we shall have to have some sort of personal "computing engine".

Similar to the small motorcycles, there are the "home computers", such as the Commodore 64's and the Atari 800XL. With a little judicious shopping, these can be found for less that a hundred dollars. Although these are definitely in the class of "motorcycle" computers, they still have 64 kilobytes of memo and a built-in BASIC interpter. A low-cost computer is ve capable of doing sophisticated engineering analysis - includi using the Method of Moments to calculate wire antenna inp impedance [1]. All of the examples in this paper can be modifi to operate on these little "home computers", such as the Ata with a minimum of effort.

A more typical "personal engineering computer" (PEC) cou be desicribed as having 64K or more of memory, dual disk driv and operating under either the 8-bit CP/M operating system or t 16-bit MS-DOS operating system. A computer such as this wil represent an investment of something between $600 and $200 dollars, depending on how hard one is willing to shop. C course, it is possible to spend more, but the purpose of thi paper is to show how computers that can be purchased by a individual engineer or a tight departmental budget can d significant work.

SYSTEM SOFTWARE:

To operate any computer, you will need a certain amount o programs, or software. We have already mentioned the operatin system, in most cases either CP/M or MS-DOS (or one of thei close relatives). Between these two operating systems most o the personal computers are covered. This operating syste software is generally provided with the computer, and is used t provide basic file handling and program loading.

In addition to the operating system or file handler, yo need some sort of 'translator'. Although for many years FORTRA was widely used, it is not as readily available for persona

computers as BASIC. In most cases, programs written in FORTRAN can be translated to BASIC with a minimum of effort. The only snag in this process (well-known to RF designers) is the lack of COMPLEX data types in BASIC. If BASIC had complex data types, it would be a much more useful language for us. Usually BASIC has been provided with your computer - it might be called MBASIC, GWBASIC, BASICA, APPLESOFT BASIC, etc. but they all tend to be variations of Microsoft's MBASIC V5.2 which has become a de facto standard for small computer BASIC interpeters. By staying with the Microsoft BASIC and its variants, we are assured of:

1 - Ease of program modification and debugging.

2 - A high degree of portability between machines.

3 - A common data file structure that many programs can use.

So far we have discussed the "system software" that comes with each computer. We still cannot do any useful design work until we have applications software - those programs that actually calculate and display the information we use. Where are these programs coming from? As all of you are undoubtedly aware, RF design programs are not as popular as word processors. Yet there are many sources of low cost or free software that are directly applicable or easily modified to our needs.

Low- or no-cost software is available from a variety of sources. Most of the programs I use regularly in my duties as a practicing RF engineer have been published in technical magazines. RF Design Magazine is one of the better sources of programs. Other good sources include EDN, Ham Radio, Microwave Journal, etc. The bibliography has several references. The important thing to remember is (to quote Tom Lehr) - "let nothing escape your eyes..." Read or scan as many of the publications as possible and start a clipping file.

Another good source of programs is in manufacturer's application notes. These notes are generally tailored to a specific machine, but I have found them to be easily adopted to other computers. As an example, the now obsolete Hewlett-Packard 9100-series of desktop calculators had excellent discussions of programs that could be used for filter design, transmission line calculations, etc and were easily adapted to BASIC. These programs (and calculators!) often turn up at flea markets, swap meets and house organ classified advertising.

The US Government and universities have a number of catalogs available that describe programs that have been written and are available for a small fee or free. CAED, an excellent microstrip design package (written in FORTRAN) is availble from the US Government [2]. Again, most of these programs are tailored to a specific machine or application, but many of them have wide application. A classic example is the circuit analysis program, SPICE, written and distributed by the University of California [3]. It take a little snooping to find these sources, but other engineers and libraries can be a big help.

A few companies provide low-cost (defined as under $100) software for engineers. Others, with their full-page advertisements, make us envious, but in general, they tend to be out of range to our budgets. All of us would like to have a program like SPICE2 running on our computers, but cannot justify

the cost of many hundreds or thousands of dollars. A more acceptable substitute are "canned" programs such as ACNAP and DCNAP [4,5] from BV Engineering. These companies provide programs at reasonable cost for our requirements. One company, DYNACOMP [6], provides programs in BASIC source form, so they can be modified for a specific application.

The microcomputer publishing industry has been publishing hundreds of books on using your personal computer for everything from cat breeding to sports handicapping. There are several volumes available of programs for engineering computing, but in general, I have found these not to be of much use. A few exceptions are worth noting. F.R. Ruckdeschel's BASIC Scientific Subroutines (Volumes I & II) [7] should be in every engineer's library. These books are a collection of well-documented programs for many of the mathematical operations that are required for serious engineering work. These programs and subroutines are presented with unique line numbers so they can be used directly - a helpful feature. These subroutines can be purchased already on disk at a nominal cost [8]. Another very useful publication is Antenna Design using Personal Computers by David S. Pozar [9]. This little xpublication is a collection of programs for path analysis, transmission line and antenna design, with a good explanation of the theory involved and a comparison of results with calculated values. Also, these programs are availble on disk [10]. A last example of an excellent publication for the engineer engaged in computer-aided design is Circuit Design using Personal Computers by T. R. Cuthbert [11]. This volume has numerous programs for design (as opposed to analysis) for the small computer, and includes an excellent discussion of optimization, which is often neglected in CAD articles and publications.

A final source of suitable applications software for our "poor man's work station" is ourselves. Although it takes a bit of effort, writing a program to solve a particular design problem can be a fun. Possibly a fellow engineer has a similar requirement to yours and already has a suitable program or one that can be modified. An example of "home brew" engineering programs are included in Appendix A of this paper. Both were written by members of the San Bernardino Microwave Society to solve a specific application, and have been widely distributed and modified by others. Most engineers that write these programs are happy to share them, so always ask, and always give credit where credit is due. In general, these are not the slick finished products that would be available from publishers, but are useful.

PRACTICAL CONSIDERATIONS:

Now that we have discussed the sources of programs that are availbe to the RF design engineer, let's discuss some of the problems we can encounter.

First of all, just because all BASIC programs are similar, they are not identical! In general, when getting a program from another machine, it is necessary to make some minor conversions. Such things as file opening and closing, data formats, and minor syntax variations can drive you up the wall. Multiple statement delimiters, "extra" functions, etc., all have to be resolved and

corrected. If you are getting a disk-based program from a different (foreign) machine, try to get the program in ASCII format. As a practical matter, I save all of my programs in ASCII instead of the more compact binary format, just to simplify the conversion between different machines. A side benefit of this method of storage allows you to edit and print the source listings with an editor or word processor.

If you are writing programs, try to include provision for storing and loading infomation from disk - this will save you the trouble of typing a circuit over and over. A little effort at this stage can make a program much more professional and easier to use. Data files can be designed that can be used by many programs. I use the format of printing to file the independent variable, followed by dependent variables, e.g. frequency, real part of impedance, imaginary part of impedance in actual values, such as Hz, ohms, etc. Try to avoid the use of specific multipliers, such as GHz; it is then difficult to use your program in a wide variety of situations. Make an effort to maintain consistency whenever possible. When dealing with arrays of data, such as network analysis programs, data files should have a header that specifies the dimensions of the array. It is very easy to forget these parameters when you are working with many different projects.

SOME EXAMPLES

Network Analysis: One of the recurring tasks for the RF design engineer is predicting the performance of a circuit and modifying it until it meets requirements. The normal process is to rely on our experience, etc. to get an initial design, breadboard, measure performance, and "tweak and trim" until the desired performance is achieved. Computer aided design is a much more difficult task than computer-aided analysis. In design, we input the desired performance and the output is a circuit. In analysis, the circuit is input and the output is performance. Most small computer programs use an input circuit and calculate performance. Computer -aided design programs are available [12] but I have found that convergence on an acceptable design by interaction is a faster and more comfortable approach.

As an example, the process for design and evaluation of a simple diplexer will be demonstrated. This diplexer is to split the FM broadcast band (88-108 MHz) and the 2-meter amateur radio band (144-148 MHz) from a common source. Since this is intended for very low-cost applications (mobile reception) we decide to use a simple set of Butterworth filter circuits (*Figure 1*). After coming up with this "quick and dirty" circuit, we load NET85.ASC (Appendix B) and analyze the circuit over the bands of interest. The results of this anaylsis are shown in Figure 2. Inspection of this data indicates that fabrication could be simplified by using standard circuit elements shown in Figure 3. Continuing to work with NET85, we add these changes and obtain the performance shown in Figure 4. Since our only intent is to build one of these for the car belonging to the president's son, we conclude this is an adequate design.

The NET85 program is derived from a program that was originally described in EDN magazine[13]. It was written in a BASIC-like language and has been translated to GWBASIC (Appendix

8). The program has been extensively modified to allow for creation and saving of the program data. Examples of input and output data files are also shown in Appendix B. The files are then plotted on a low-cost commercial plotting package [14].

EXAMPLE II: MICROWAVE ANTENNA DESIGN

One of the more tedious tasks facing engineers is the occasional design of an antenna. As RF engineers we are often called to come up with at least a rough design for an antenna (How big a dish do we need to receive OSCAR VII?). Appendix B2 has a straight-forward program to design a suitable Cassegrain or prime-focus reflector antenna. Once a suitable design is reached, other BASIC language programs can be used for more detailed analysis [9]. The results can then be presented by using one of many available graphing or plotting programs [14]. When using these relatively simple programs it is important to remember that most of them are based on geometric optic considerations, so do not compensate for edge effects, etc., and will likely provide incorrect answers for small antennas. In general, the higher the antenna gain, the easier it is to predict its performance. There are some programs available [9] that go beyond geometric considerations, but large physical optics or method of moment solutions tend to be beyond personal computers. However, it may be possible to reduce a fairly complex program program to parts that will run on a personal computer. The computation-intensive parts, such as the solution of the complex matricies, could be allowed to run overnight. Most of these programs are availble in FORTRAN [15] and could be loaded and compiled on a MS-DOS based PC, as there are FORTRAN compilers available that can deal with COMPLEX data types. It is possible to translate these programs to BASIC, but it is left as an excercise to the reader to accomplish this.

OTHER APPLICATIONS:

The duties of the RF designer generally include a large portion of 'administrative' duties. These include reports, memoranda, statements of work, project tracking, procurement documents, etc. Most of us find these tasks at best a burden and at worst an imposition. Until management sees fit to provide us with adequate administrative and paraprofessional support, these tasks will remain with us. Our "poor man's engineering work station' can be pressed into service to support these functions. By including some form of text editor or word processing software, reports and memos can be generated quickly and in a more readable form. By relieving the work of preparing documents, I have found that using a small desktop computer increases my engineering productivity significantly. In addition, most engineers would rather design than perform administrative tasks, so the editing function alone makes a personal desktop computer worthwhile.

Procurement actions, schedules, parts and wire lists, etc. can be efficiently maintained using one of the many microcomputer data base managers. As an example, I used a data base on an old microcomputer to maintain a wire list for a large transmitter. By simply inquiring the disk, I could get a list of all the locations a particular signal could be found or all signals on a

particular connector or terminal block.

These applications are well known, and it is not my intention to go into great detail, but sometimes we overlook the 'support functions' that take up so much time. If we can develop more time for design work, it enables us to be more effective as engineers.

CONCLUSIONS:

This paper has presented one engineer's view of the use of obsolescent technology to make his job easier and more productive. As the cost of computing power continues to decline, we will have the power of supermini computers available to us. In the meantime, the latest technology may not be available. I have tried to show with a few examples how we can use existing low-end hardware combined with relatively simple software to greatly speed up our efforts as design engineers. The key is the *immediate availability of a computer*. It *is better to have an* old, slow machine immediately availble to us for a quick evaluation, than a large mainframe that we have to schedule well in advance. The programs and examples I have presented are not necessarily the most efficient or accurate. They are programs that I have used and refined over the years to accomplish specific tasks. There are many things that can be done by the user to make these programs more efficent or easier to use. As an example, an option could easily by added to allow input to NET85.ASC as reactance values, rather than component values. This change would be very helpful, but I never "got around tuit". The bibliography lists several sources of software, but I make no claims for its accuracy or completeness.

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APPENDIX A

USER-WRITTEN BASIC DESIGN PROGRAMS

A.1 DISH.ASC This program was written by Chuck Swedblom of the San Bernardino Microwave Society for design and analysis of Cassegrain-reflector antennas. It is based on ray-trace optics.

```
10 '
20 ' PARABOLIC ANTENNA DESIGN PROGRAM
30 '
40 ' Written by C. Swedblom, WA6EXV January 13, 1981 (not Friday)
50 '
60 ' Revised: March 26, 1981
70 '
80 'Modified for Microsoft Basic by R. Kolbly, K6HIJ April 3, 1981
90 '  (Friday after a Society Meeting!)
100 '
110 CLS$=CHR$(27)+"E"
120 PI=3.14159288
130 DIM X(100)
140  M$="###.##"
150  D$="###"
160 PRINT CLS$
170 PRINT "Select area of interest"
180 PRINT
190 PRINT "     1.  Calculate f/D and Gain of a Parabolic Dish."
200 PRINT "     2.  Design Sub Reflector for Cassegrain feed."
210 PRINT "     3.  Return to Basic"
220 INPUT "Your Choice";ME
230 IF ME < 1 THEN 260
240 IF ME > 3 THEN 260
250 ON ME GOTO 290,700,1390
260 PRINT CLS$
270 PRINT "Values between 1 and 3 only!"
280 GOTO 170
290 ' Calculate f/D
300 '
310 PRINT CLS$
320 INPUT "Diameter of the Dish in Inches";DIA
330 PRINT
340 INPUT "Depth of Dish, same units as Diameter";CR
350 PRINT
360 INPUT "Frequency of Interest, in MHz";MHZ
370 PRINT
380 INPUT "Efficency of the Dish in %";EFF
390  FDR=DIA/(16*CR)
400  LAMDA=30000/(2.54*MHZ)
410  GAIN=(PI*DIA/LAMDA)^2*EFF/100
420  GAIN=10/LOG(10)*LOG(GAIN)
430 '
440 ' Print Results
450 '
460 'INPUT "Port #",N (For output of Chuck's Basic)
470 PRINT CLS$
480 PRINT "             PARABOLIC DISH f/D and GAIN"
490 PRINT "             --------------------------"
500 PRINT:PRINT
510 PRINT "Diameter of the Parabolic Dish.......";
520 PRINT USING M$;DIA;:PRINT " In."
530 PRINT
540 PRINT "The f/D Ratio of the Parabolic Dish...";
550 PRINT USING M$;FDR
560 PRINT
570 PRINT "The Gain of the Parabolic Dish.......";
580 PRINT USING M$;GAIN;:PRINT " dB at ";MHZ;" MHz"
590 PRINT "    with an Efficiency of ...........";
600 PRINT USING D$;EFF;:PRINT " %"
610 '
620 ' Calculate Distance to the focal point
630 '
640  FR=FDR*DIA
650 PRINT
660 PRINT "The distance to the focal point is....";
670 PRINT USING M$;FR;:PRINT " Inches"
680 PRINT:PRINT:PRINT:PRINT:PRINT
690 END
700 '
710 ' Calculate the size and location of a Sub Reflector for a
720 ' Cassegrain fed Parabolic Dish.
730 '
740 PRINT CLS$
750 INPUT "f/D of the Real Dish in Inches";FDR
760 PRINT
770 INPUT "f/D of the Virtual Dish";FDV
780 PRINT
790 INPUT "Diameter of the Real Dish in Inches";DIA
800 PRINT
810 INPUT "Ratio of Sub Ref Dia. to Diameter, not over .3";FSR
820 PRINT
830  FR=FDR*DIA
840  FV=FDV*DIA
850  CR=DIA^2/(16*FR)
860  CV=DIA^2/(16*FV)
870  DSR=DIA*FSR
880  M=DSR*(FR-CR)/DIA
890  L=DSR*(FV-CV)/DIA
900  A=(L+M)/2*(FV-FR)/(FV+FR)
910  E=(L+M)/(2*A)
920  THETA=2*ATN((DIA/2)/(FV-CV))
930  BLOCK=DIA*DIA-DSR*DSR
940  GAINSR=10/LOG(10)*LOG(BLOCK)
950  GAINRE=10/LOG(10)*LOG(DIA*DIA)
960  BLK=GAINRE-GAINSR
970  THETA=THETA*180/PI
980 'output the Data
```

```
990 '
1000 '
1010 PRINT CLS$
1020 PRINT "                PARABOLIC DISH/SUB-REFLECTOR"
1030 PRINT "                ----------------------------"
1040 PRINT:PRINT
1050 PRINT "Diameter of Dish.............................";
1060 PRINT USING M$;DIA;:PRINT "In."
1070 PRINT "i/D of Real Dish.............................";
1080 PRINT USING M$;FDR
1090 PRINT "f/D of Virtual Dish..........................";
1100 PRINT USING M$;FDV
1110 PRINT "Focal Point of Real Dish.....................";
1120 PRINT USING M$;FR;:PRINT " In."
1130 PRINT "Focal Point of Virtual Dish..................";
1140 PRINT USING M$;FV;:PRINT " In."
1150 PRINT "Diameter of Sub-Reflector....................";
1160 PRINT USING M$;DSR;:PRINT " In."
1170 PRINT "Location of Sub-Reflector....................";
1180 PRINT USING M$;FR-M;:PRINT " Inches from Org."
1190 PRINT "Location of Feed Horn........................";
1200 PRINT USING M$;(FR-M)-L;:PRINT " Inches from Org."
1210 PRINT "Feed Beam Width..............................";
1220 PRINT USING M$;THETA;:PRINT " Deg."
1230 PRINT "Reduction in Gain due to Sub-Reflector.......";
1240 PRINT USING M$;BLK;:PRINT " dB."
1250 PRINT:PRINT:PRINT
1260 '
1270 ' Print X-Y Coordinates of Hyperbolidal Sub-Reflector
1280 '
1290 INPUT "Enter increment for Sub Ref. X-Y Cordinates";INC
1300 PRINT TAB(5);"X-Y Co-ord. for Hyperbolidal Sub-Ref."
1310 PRINT
1320 PRINT TAB(10);"Y-Co-ord.";TAB(28);"X-Co-ord."
1330 PRINT
1340 FOR Y=0 TO DSR/2 STEP INC
1350 X(Y)=SQR(A*A+(Y*Y)/(E*E-1))
1360 Z=X(Y)-X(0)
1370 PRINT TAB(10);:PRINT USING M$;Y;:PRINT TAB(28);
1380 PRINT USING M$;Z
1390 NEXT Y
1400 END
```

A.2 STRIPLIN.ASC This program is for design of microstrip lines

and has been continously refined. Again, it is user-written.

```
10 REM THIS PROGRAM CALCULATES THE WIDTH OF A MICROSTRIP LINE
20 REM FOR A GIVEN IMPEDANCE OF WILL CALCULATE THE IMPEDANCE
30 REM OF A MICROSTRIP LINE OF A GIVEN WIDTH
40 REM
50 REM WRITTEN BY C. SWEDBLOM, WA6EXV 12 JUNE 1979
60 REM MODIFIED BY DICK KOLBLY, K6HIJ 16 SEPT 1979
70 REM DIELECTRIC CONSTANTS ADDED K6HIJ 10 MARCH 1981
80 REM   W=WIDTH OF MICROSTRIP LINE
90 REM   H=THICKNESS OF SUBSTRATE MATERIAL
100 REM   T=THICKNESS OF MICROSTRIP LINE
110 REM  F=FREQUENCY
120 REM  E=DIELECTRIC CONSTANT OF SUBSTRATE MATER
130 REM  E1=DIELECTRIC CONSTANT AT DC
140 REM  E2=DIELECTRIC CONSTANT AT F0
150 REM  Z=CHARACTERISTIC IMPEDANCE OF MICROSTRIP
160 REM  Z1=CHARACTERISTIC IMPEDANCE AT DC
170 REM  Z2=DESIRED IMPEDANCE
180 REM  L=WAVELENGTH
190 REM  D1=IMPEDANCE ERROR FACTOR
200 REM
210 D1=.0001
220 P1=3.141592654
230 PRINT "1 OZ Cu=.0013 in, 2 Oz Cu=.0027"
240 PRINT "(1) AIR              (e=1.00)"
250 PRINT "(2) G10 FIBERGLASS (e=4.80)"
260 PRINT "(3) TEFLON/GLASS   (e=2.55)"
270 PRINT "(4) REXOLITE         (e=2.54)"
280 PRINT "(5) TEFLON           (e=2.10)"
290 PRINT "(6) FORMICA XX       (e=4.04)"
295 PRINT "(7) DUROID           (e=2.23)"
300 INPUT "(8) OTHER";K:IF K=0 OR K=8 THEN 310 ELS
310 INPUT"TYPE OF MATERIAL AND ER";A$,E
320 IF K=1 THEN A$="AIR":E=1!
330 IF K=2 THEN A$="G10":E=4.8
340 IF K=3 THEN A$="TEFLON/FIBERGLASS":E=2.55
350 IF K=3 THEN A$="REXOLITE":E=2.54
360 IF K=5 THEN A$="TEFLON":E=2.1
370 IF K=6 THEN A$="FORMICA XX":E=4.04
375 IF K=7 THEN A$="DUROID":E=2.23
380 IF K<0 OR K>8 THEN 300
390 INPUT"FREQUENCY (GHZ)";F
400 INPUT"SUBSTRATE THICKNESS";H
410 INPUT "LINE THICKNESS";T
420 PRINT "DO YOU WANT"
430 PRINT
440 PRINT"1.  MICROSTRIP WIDTH"
450 PRINT"2.  IMPEDANCE OF MICROSTRIP LINE?"
460 PRINT
470 INPUT X
480 IF X=2 THEN 680
490 INPUT "DESIRED IMPEDANCE=";Z2
500 W=1
510 GOSUB 740
520 GOSUB 820
530 PRINT Z
540 R=Z/Z2
550 IF ABS((1-R)/(1+R))<=D1 THEN 620
560 REM CALCULATE NEW WIDTH
570 W=W*R*R
580 GOTO 510
590 REM
600 REM ADJUST WIDTH FOR THICKNESS OF LINE
```

```
610 REM
620 GOSUB 1010
630 W=W-W1
640 GOTO 1090
650 REM
660 REM CALCULATE IMPEDANCE FROM LINE WIDTH
670 REM
680 INPUT"LINE WIDTH =";W
690 GOSUB 1010
700 W=W+W1
710 GOSUB 740
720 GOSUB 820
730 GOTO 1090
740 REM
750 REM SUBROUTINE TO CALCULATE P
760 REM
770 IF W/H<=1 THEN 800
780 P=2*P1/((W/H)+2.42-(.44*H/W)+EXP(8*LOG(1-(H/W))))
790 RETURN
800 P=LOG((8*H/W)+W/(4*H))
810 RETURN
820 REM
830 REM SUBROUTINE TO CALUCLATE E1,E2 AND Z
840 REM
850 E3=((E-1)/2*(1/SQR(1+(10*H/W))-1))
860 E1=E+E3
870 REM
880 REM CALCULATE EFFECTIVE ER
890 REM
900 REM DISPERSION EQUATION FROM GETSINGER
910 REM
920 Z1=60*P/SQR(E1)
930 G=.6+(.009*Z1)
940 D=Z1/(2.54*4*P1*H)
950 E2=E+(E3/(1+G*EXP(2*LOG(F/D))))
960 REM
970 REM CALCULATE IMPEDANCE,Z
980 REM
990 Z=60*P/SQR(E2)
1000 RETURN
1010 REM
1020 REM SUBROUTINE TO CORRECT LINE WIDTH FOR THICKNESS
1030 REM
1040 IF W/H<.15915 THEN 1070
1050 W1=(T/P1)*(1+LOG(2*H/T))
1060 RETURN
1070 W1=(T/P1)*(1+LOG((4*P1*W)/T))
1080 RETURN
1090 REM
1100 REM PRINT OUT RESULTS
1110 REM
1120 L=(11.811/F)/SQR(E2)
1130 REM
1140 REM THESE ARE RESERVED FOR PRINT FORMATS
1150 REM
1160 PRINT:PRINT:PRINT
1170 PRINT"  TYPE OF MATERIAL----------";A$
1180 PRINT"  DIELECTRIC CONSTANT----------";E
1190 PRINT"  EFFECTIVE DIELECTRIC CONSTANT-----";E2
1200 PRINT"  OPERATING FREQUENCY----------";F;" GHZ"
1210 PRINT"  IMPEDANCE OF MICROSTRIP----------";Z;" OHMS"
1220 PRINT"  WIDTH OF MICROSTRIP----------";W;" INCHES"
1230 PRINT"  THICKNESS OF SUBSTRATE----------";H;" INCHES"
1240 PRINT"  THICKNESS OF MICROSTRIP LINE------";T;" INCHES"
1250 PRINT"  WAVELENGTH----------";L;" INCHES"
1260 PRINT"  QUARTER WAVELENGTH----------";L/4;" INCHES"
1270 PRINT:PRINT:PRINT
1280 INPUT"ANOTHER RUN";Q$:Q$=LEFT$(Q$,1)
1290 IF Q$="Y" THEN 1300 ELSE END
1300 IF X=1 THEN GOTO 490 ELSE GOTO 680
```

APPENDIX B

NET85. ASC - A useful network analysis program derived from literature, but extensively modified by users for particular needs, including file storage of circuits and results of analysis.

```
10 ' *** NET*85 ***
20 ' SEE EDN FEB 4, 1981 PP 126-133
30 ' TRANSLATED TO MICROSOFT BASIC BY R.B. KOLBLY
35 ' DISK FILES FOR SAVING AND RESTORING NETWORKS ADDED
36 ' DATA FILE OUTPUT CAPABILITY ADDED
40 ' GOLDEN RULE SYSTEMS - FEBRUARY 22,1985
50 P$=
 "FREQ= ##.####^^^^  AMPL= ##.##^^^^  20LOG= ####.#  PHASE= ####.#"
60 K=INT(FRE(A)/4)-23
70 X=INT((SQR(169+24*K)-26)/12)-1
80 PRINT USING "You have a maximum of ## Nodes Available";X
90 INPUT "Number of Nodes Desired (CR=10)";Y
100 IF X>=10 AND Y=0 THEN X=10:GOTO 140
110 IF X<10 AND Y=0 THEN X=Y:GOTO 140
120 IF Y>X THEN PRINT USING "Maximum of ### nodes!";X:GOTO 90
130 IF Y<X THEN X=Y
140 DIM A(X,X),B(X,X),P(X,X),Q(X,X),R(X,X)
150 DIM S(X,X),I(2*X),FL$(4,2)
160 DIM T(2*X),M(2*X),N(2*X),O(2*X),L(2*X),Z(2*X)
170 PRINT USING "You have selected a maximum of ## nodes";X
180 FOR J=1 TO X
190 FOR I=1 TO X
200 P(I,J)=0
210 Q(I,J)=0
220 R(I,J)=0
230 S(I,J)=0
240 NEXT I
250 NEXT J
260 NODES=X:X=1:T(X)=0
270 N=0
280 PRINT "1   RESISTOR"
290 PRINT "2   CAPACITOR"
300 PRINT "3   INDUCTOR"
310 PRINT "4   TRANSMISSION LINE"
320 PRINT "5   SHORTED STUB"
330 PRINT "6   OPEN STUB"
340 PRINT "7   OPERATIONAL AMPLIFIER"
350 PRINT "8   NPN TRANSISTOR"
360 PRINT "9   FIELD-EFFECT TRANSISTOR"
370 PRINT "10  STOP"
380 PRINT "11  ANALYZE NETWORK"
390 PRINT "12  ENABLE/DISABLE PRINTER"
391 PRINT "13  RESTORE NETWORK FROM DISK"
392 PRINT "14  SAVE NETWORK TO DISK"
393 PRINT "15  GENERATE ASCII NETWORK FILE"
400 PRINT "16  LOAD NETWORK VALUES FROM ASCII FI
410 PRINT
420 R6=0:INPUT "SELECT FROM LIST (<CR> FOR MENU)'
430 IF R6=1 THEN PRINT "(1) RESISTOR":GOTO 730
440 IF R6=2 THEN PRINT "(2) CAPACITOR":GOTO 810
450 IF R6=3 THEN PRINT "(3) INDUCTOR":GOTO 770
460 IF R6=4 THEN PRINT "(4) TRANSMISSION LINE":G(
470 IF R6=5 THEN PRINT "(5) SHORTED STUB":GOTO 6!
480 IF R6=6 THEN PRINT "(6) OPEN STUB":GOTO 710
490 IF R6=7 THEN PRINT "(7) OP AMP":GOTO 990
500 IF R6=8 THEN PRINT "(8) NPN TRANSISTOR":GOTO
510 IF R6=9 THEN PRINT "(9) FET TRANSISTOR":GOTO
520 IF R6=10 THEN PRINT "(10) PROGRAM FINISH":ST(
530 IF R6=11 THEN PRINT "(11) ANALYSIS":GOTO 106(
540 IF R6=12 THEN INPUT "(12) HARDCOPY OUTPUT (Y/
    :H$=LEFT$(H$,1): GOTO 420
541 IF R6=13 THEN PRINT "(13) RESTORE NETWORK TO
    :GOTO 3000
542 IF R6=14 THEN PRINT "(14) SAVE NETWORK TO DI!
543 IF R6=15 THEN PRINT "(15) GENERATE ASCII NETW
    :GOTO 5000
544 IF R6=16 THEN PRINT "(16) LOAD NETWORK FROM A
    :GOTO 4000
550 GOTO 280
560 T(X)=1:INPUT "SHIELD IN";M(X):REM *** TRANSMI
570 INPUT "CENTER IN";I(X):INPUT "CENTER OUT";O(X
580 INPUT "SHIELD OUT";N(X):GOTO 610
590 INPUT "NODE A";M(X)
600 INPUT "NODE B";N(X)
610 INPUT "Z0";Z(X)
620 INPUT "QUARTER-WAVE FREQUENCY (HZ)";L(X)
630 IF I(X)>N THEN N=I(X)
640 IF M(X)>N THEN N=M(X)
650 IF N(X)>N THEN N=N(X)
660 IF O(X)>N THEN N=O(X)
670 X=X+1:T(X)=0
680 GOTO 420
690 T(X)=3: REM *** SHORTED STUB ***
700 GOTO 590
710 T(X)=2: REM *** OPEN STUB ***
720 GOTO 590
730 INPUT "NODE A";I:INPUT "NODE B";J:INPUT "RESI!
740 V=1/V
750 GOSUB 1430
760 GOTO 420
770 INPUT "NODE A";I:INPUT "NODE B";J:INPUT "INDU(
780 V=1/V
790 GOSUB 1360
800 GOTO 420
810 INPUT "NODE A";I:INPUT "NODE B";J
    :INPUT "CAPACITANCE (FARADS)";V
820 GOSUB 1480
830 GOTO 420
840 INPUT "GATE";K:INPUT "SOURCE";J:INPUT "DRAIN";
```

```
   INPUT "GAIN(MHO)";V
850 L=J
860 GOSUB 1530
870 GOTO 420
880 INPUT "BASE";K:INPUT "EMITTER";J:INPUT "COLLECTOR";I:
   INPUT "BETA";R5
890 INPUT "Rbe (OHMS)";V
900 V=1/V
910 L=I
920 I=K
930 GOSUB 1430
940 I=L
950 L=J
960 V=V*R5
970 GOSUB 1530
980 GOTO 420
990 INPUT "+IN";K:INPUT "-IN";L:INPUT "-OUT";1:REM *** OP-AMP ***
1000 INPUT "+OUT";J:INPUT "GAIN(V/V)";R5:
    INPUT "OUTPUT RESISTANCE(OHMS)";V
1010 V=1/V
1020 GOSUB 1430
1030 V=V*R5
1040 GOSUB 1530
1050 GOTO 420
1060 INPUT "INPUT NODE";E:INPUT "OUTPUT NODE";F:N=N-1
1070 INPUT "START,STOP FREQUENCIES (HZ)";G,H
1080 INPUT "# OF DATA POINTS";M
1090 INPUT "FREQUENCY SWEEP-LOG=0(LINEAR=1)";R6
1091 PFG=0:INPUT "Do you want output data files";Q$:Q$=LEFT$(Q$,1)
1092 IF Q$="Y" OR Q$="y" THEN GOSUB 7000
1100 D=(H-G)/(M-1)
1110 R4=EXP(LOG(H/G)/(M-1))
1120 R0=G:R9=0
1130 R9=R9+1
1140 W=2*3.14159*R0
1150 O=E:Z=F
1160 GOSUB 2470
1170 GOSUB 2200
1180 V=R5:U=Z
1190 IF (E+F)/2=INT((E+F)/2) THEN 1210
1200 U=U-180
1210 O=E:Z=E
1220 GOSUB 2200
1230 U=U-Z
1240 IF V=0 THEN R7=-999:GOTO 1270
1250 IF R5=0 THEN R7=9999:GOTO 1270
1260 V=V/R5:R7=8.68589*LOG(V)
1270 IF U>180 THEN U=U-360
1280 IF U<-180 THEN U=U+360
1290 PRINT USING P$;R0,V,R7,U
1300 IF H$="Y" THEN LPRINT USING P$;R0,V,R7,U
1302 IF PFG=0 THEN GOTO 1310
1304 GOSUB 7200
1310 IF R6=0 THEN R0=R0*R4
1320 IF R6<>0 THEN R0=R0+D
1330 IF R9<>M THEN 1130
1340 N=N+1
1350 CLOSE:GOTO 420
1360 R(I,I)=R(I,I)+V:REM INDL
1370 R(J,J)=R(J,J)+V
1380 R(I,J)=R(I,J)-V
1390 R(J,I)=R(J,I)-V
1400 IF I>N THEN N=I
1410 IF J>N THEN N=J
1420 RETURN
1430 P(I,I)=P(I,I)+V:REM RESL
1440 P(J,J)=P(J,J)+V
1450 P(I,J)=P(J,J)-V
1460 P(J,I)=P(J,I)-V
1470 GOTO 1400
1480 Q(I,I)=Q(I,I)+V
1490 Q(J,J)=Q(J,J)+V:REM CAPL
1500 Q(I,J)=Q(I,J)-V
1510 Q(J,I)=Q(J,I)-V
1520 GOTO 1400
1530 P(I,K)=P(I,K)+V:REM TRANS
1540 P(J,L)=P(J,L)+V
1550 P(J,K)=P(J,K)-V
1560 P(I,L)=P(I,L)-V
1570 IF K>N THEN N=K
1580 IF L>K THEN N=L
1590 GOTO 1400
1600 IF N>1 THEN 1630: REM COMP
1610 O=A(1,1):Z=B(1,1)
1620 RETURN
1630 O=1
1640 Z=0
1650 K=1
1660 L=K
1670 S=ABS(A(K,K))+ABS(B(K,K))
1680 I=K-1
1690 I=I+1
1700 T=ABS(A(I,K))+ABS(B(I,K))
1710 IF S>=T THEN 1730
1720 L=I:S=T
1730 IF I<>N THEN 1690
1740 IF L=K THEN 1800
1750 J=0
1760 J=J+1
1770 S=-A(K,J):A(K,J)=A(L,J):A(L,J)=S
1780 A=-B(K,J):B(K,J)=B(L,J):B(L,J)=A
1790 IF J<>N THEN 1760
1800 L=K+1:I=L-1
1810 I=I+1
1820 A=A(K,K)*A(K,K)+B(K,K)*B(K,K)
1830 S=(A(I,K)*A(K,K)+B(I,K)*B(K,K))/A
1840 B(I,K)=(A(K,K)*B(I,K)-A(I,K)*B(K,K))/A
1850 A(I,K)=S
1860 IF I<>N THEN 1810
1870 C=K-1
```

```
1880 IF C=0 THEN 1960
1890 J=L-1
1900 J=J+1:I=0
1910 I=I+1
1920 A(K,J)=A(K,J)-A(K,I)*A(I,J)+B(K,I)*B(I,J)
1930 B(K,J)=B(K,J)-B(K,I)*A(I,J)-A(K,I)*B(I,J)
1940 IF C<>I THEN 1910
1950 IF J><N THEN 1900
1960 C=K
1970 K=K+1:I=K-1
1980 I=I+1:J=0
1990 J=J+1
2000 A(I,K)=A(I,K)-A(I,J)*A(J,K)+B(I,J)*B(J,K)
2010 B(I,K)=B(I,K)-B(I,J)*A(J,K)-A(I,J)*B(J,K)
2020 IF J<>C THEN 1990
2030 IF I<>N THEN 1980
2040 IF K<>N THEN 1660
2050 L=1
2060 C=INT(N/2)
2070 IF N=2*C THEN 2100
2080 L=0
2090 O=A(N,N):Z=B(N,N)
2100 I=0
2110 I=I+1
2120 J=N-I+L
2130 S=A(I,I)*A(J,J)-B(I,I)*B(J,J)
2140 A=A(I,I)*B(J,J)+A(J,J)*B(I,I)
2150 T=O*S-Z*A
2160 Z=Z*S+O*A
2170 O=T
2180 IF I<>C THEN 2110
2190 RETURN
2200 R5=N:REM DET
2210 N=N-1
2220 I=0
2230 K=0
2240 K=K+1
2250 IF K<>O THEN 2270
2260 I=1
2270 J=0:L=0
2280 L=L+1
2290 IF L<>Z THEN 2310
2300 J=1
2310 A(K,L)=P(K+I,L+J)
2320 B(K,L)=W*Q(K+I,L+J)-R(K+I,L+J)/W+S(K+I,L+J)
2330 IF L<>N THEN 2280
2340 IF K<>N THEN 2240
2350 GOSUB 1600
2360 N=R5
2370 R5=SQR(O*O+Z*Z)
2380 Y=Z
2390 IF O=0 THEN 2450
2400 Z=180/3.14159*ATN(Z/O)
2410 IF O>0 THEN RETURN
2420 Z=Z+SGN(Y)*180
2430 IF Y=0 THEN Z=180
2440 RETURN
2450 Z=90*SGN(Y)
2460 RETURN
2470 IF T(1)=0 THEN RETURN
2480 X=0
2490 R1=0
2500 R1=R1+1:R2=0
2510 R2=R2+1
2520 S(R1,R2)=0
2530 IF R2<>N+1 THEN 2510
2540 IF R1<>N+1 THEN 2500
2550 X=X+1
2560 IF X>20 THEN RETURN
2570 IF T(X)=0 THEN RETURN
2580 IF T(X)=1 THEN 2640
2590 IF T(X)=2 THEN 2830
2600 R1=-1/(Z(X)*TAN(.25*W/L(X)))
2610 Q=M(X):R=N(X)
2620 GOSUB 2870
2630 GOTO 2550
2640 R1=-1/(Z(X)*TAN(.25*W/L(X)))
2650 Q=M(X):R=I(X)
2660 GOSUB 2870
2670 Q=N(X):R=O(X):GOSUB 2870
2680 R1=1/(Z(X)*SIN(.25*W/L(X)))
2690 P=I(X)
2700 R=N(X)
2710 S(R,P)=S(R,P)-R1
2720 S(P,R)=S(P,R)-R1
2730 R=O(X)
2740 S(R,P)=S(R,P)+R1
2750 S(P,R)=S(P,R)+R1
2760 P=M(X)
2770 S(R,P)=S(R,P)-R1
2780 S(P,R)=S(P,R)-R1
2790 R=N(X)
2800 S(R,P)=S(R,P)+R1
2810 S(P,R)=S(P,R)+R1
2820 GOTO 2550
2830 R2=1/(Z(X)*TAN(.25*W/L(X)))
2840 R3=1/(Z(X)*SIN(.25*W/L(X)))
2850 R1=R3*R3/R2-R2
2860 GOTO 2610
2870 S(Q,Q)=S(Q,Q)+R1
2880 S(R,R)=S(R,R)+R1
2890 S(Q,R)=S(Q,R)-R1
2900 S(R,Q)=S(R,Q)-R1
2910 RETURN
2920 END
3000 INPUT "NAME OF FILE TO LOAD <CR> FOR DIRECTORY";F$:
     ' LOAD FROM FILE
3010 IF LEN(F$)=0 THEN FILES:GOTO 3000
3020 IF F$="B:" THEN FILES "B:*.*":GOTO 3000
3030 IF F$="A:" THEN FILES "A:*.*":GOTO 3000
```

```
3040 OPEN "I",#1,F$
3050 INPUT #I,X
3060 ERASE A,B,P,Q,R,S,I,T,M,N,O,L,Z
3070 DIM A(X,X),B(X,X),P(X,X),Q(X,X),R(X,X)
3080 DIM S(X,X),I(2*X)
3090 DIM T(2*X),M(2*X),N(2*X),O(2*X),L(2*X),Z(2*X)
3095 INPUT #I,N
3100 FOR J=1 TO X
3110 INPUT #1,I(J),T(J),M(J),N(J),O(J),L(J),Z(J)
3120 FOR K=1 TO X
3130 INPUT #1,A(J,K),B(J,K),P(J,K),Q(J,K),R(J,K),S(J,K)
3140 NEXT K
3150 NEXT J
3160 CLOSE #1
3170 NODES=X:GOTO 420
3500 INPUT "NAME OF FILE TO SAVE <CR> FOR DIRECTORY";F$:
     ' SAVE INTO FILE
3510 IF LEN(F$)=0 THEN FILES:GOTO 3500
3520 IF F$="B:" THEN FILES "B:*.*":GOTO 3500
3530 IF F$="A:" THEN FILES "A:*.*":GOTO 3500
3540 OPEN "O",#1,F$
3550 PRINT #1,NODES,N
3600 FOR J=1 TO NODES
3610 PRINT #1,I(J),T(J),M(J),N(J),O(J),L(J),Z(J)
3620 FOR K=1 TO NODES
3630 PRINT #1,A(J,K),B(J,K),P(J,K),Q(J,K),R(J,K),S(J,K)
3640 NEXT K
3650 NEXT J
3660 CLOSE #1
3670 GOTO 420
4000 INPUT "Name of file to load <cr> for directory";F$
4010 IF LEN(F$)=0 THEN FILES:GOTO 4000
4020 OPEN "I",#1,F$
4030 IF EOF(1) THEN CLOSE:GOTO 420
4035 R6$="":INPUT #1,R6$:R6$=LEFT$(R6$,1)
4040 IF R6$="1" THEN GOTO 4320
4050 IF R6$="2" THEN GOTO 4400
4060 IF R6$="3" THEN GOTO 4360
4070 IF R6$="4" THEN GOTO 4150
4080 IF R6$="5" THEN GOTO 4280
4090 IF R6$="6" THEN GOTO 4300
4100 IF R6$="7" THEN GOTO 4580
4110 IF R6$="8" THEN GOTO 4470
4120 IF R6$="9" THEN GOTO 4430
4130 IF EOF(1) THEN 420
4140 GOTO 4030
4150 T(X)=1:INPUT #1,M$:M(X)=VAL(M$):REM *** TRANSMISSION LINE ***
4160 INPUT #1,I$:I(X)=VAL(I$):INPUT #1,O$:O(X)=VAL(O$)
4170 INPUT #1,N$:N(X)=VAL(N$):GOTO 4200
4180 INPUT #1,M$:M(X)=VAL(M$)
4190 INPUT #1,N$:N(X)=VAL(N$)
4200 INPUT #1,Z$:Z(X)=VAL(Z$)
4210 INPUT #1,L$:L(X)=VAL(L$)
4220 IF I(X)>N THEN N=I(X)
4230 IF M(X)>N THEN N=M(X)
4240 IF N(X)>N THEN N=N(X)
4250 IF O(X)>N THEN N=O(X)
4260 X=X+1:T(X)=0
4270 GOTO 4030
4280 T(X)=3: REM *** SHORTED STUB ***
4290 GOTO 4180
4300 T(X)=2: REM *** OPEN STUB ***
4310 GOTO 4180
4320 INPUT #1,I$:I=VAL(I$):
     INPUT #1,J$:J=VAL(J$):INPUT #1,V$:V=VAL(V$)
4330 V=1/V
4340 GOSUB 1430
4350 GOTO 4030
4360 INPUT #1,I$:I=VAL(I$):
     INPUT #1,J$:J=VAL(J$):INPUT #1,V$:V=VAL(V$)
4370 V=1/V
4380 GOSUB 1360
4390 GOTO 4030
4400 INPUT #1,I$:I=VAL(I$):
     INPUT #1,J$:J=VAL(J$):INPUT #1,V$:V=VAL(V$)
4410 GOSUB 1480
4420 GOTO 4030
4430 INPUT #1,K$:K=VAL(K$):INPUT #1,J$:J=VAL(J$):INPUT #I,I$:
     I=VAL(I$):INPUT #1,V$:V=VAL(V$)
4440 L=J
4450 GOSUB 1530
4460 GOTO 4030
4470 INPUT #I "BASE";K:INPUT #I,J$:J=VAL(J$):INPUT #1,I$:
     I=VAL(I$):INPUT #1,R$:R5=VAL(R$)
4480 INPUT #1,V$:V=VAL(V$)
4490 V=1/V
4500 L=I
4510 I=K
4520 GOSUB 1430
4530 I=L
4540 L=J
4550 V=V*R5
4560 GOSUB 1530
4570 GOTO 4030
4580 INPUT #1,K$:K=VAL(K$):INPUT #1,L$:L=VAL(L$):
     INPUT #1,I$:I=VAL(I$)
4590 INPUT #1,J$:J=VAL(J$):INPUT #1,R$:R5=VAL(R$):
     INPUT #1,V$:V=VAL(V$)
4600 V=1/V
4610 GOSUB 1430
4620 V=V*R5
4630 GOSUB 1530
4640 GOTO 4030
5000 INPUT "Name of file (<cr> for Directory)";F$
5010 IF LEN(F$)=0 THEN FILES:GOTO 5000
5020 OPEN "O",#1,F$
5200 PRINT "1   RESISTOR"
5210 PRINT "2   CAPACITOR"
5220 PRINT "3   INDUCTOR"
5230 PRINT "4   TRANSMISSION LINE"
```

```
5240 PRINT "5    SHORTED STUB"
5250 PRINT "6    OPEN STUB"
5260 PRINT "7    OPERATIONAL AMPLIFIER"
5270 PRINT "8    NPN TRANSISTOR"
5280 PRINT "9    FIELD-EFFECT TRANSISTOR"
5290 PRINT "10   STOP"
5360 R6=0:INPUT "SELECT FROM LIST";R6:R6$=STR$(R6)
5370 IF R6=1 THEN PRINT "(1) RESISTOR":GOTO 5690
5380 IF R6=2 THEN PRINT "(2) CAPACITOR":GOTO 5770
5390 IF R6=3 THEN PRINT "(3) INDUCTOR":GOTO 5730
5400 IF R6=4 THEN PRINT "(4) TRANSMISSION LINB":GOTO 5520
5410 IF R6=5 THEN PRINT "(5) SHORTED STUB":GOTO 5650
5420 IF R6=6 THEN PRINT "(6) OPEN STUB":GOTO 5670
5430 IF R6=7 THEN PRINT "(7) OP AMP":GOTO 5950
5440 IF R6=8 THEN PRINT "(8) NPN TRANSISTOR":GOTO 5840
5450 IF R6=9 THEN PRINT "(9) FET TRANSISTOR":GOTO 5800
5460 IF R6=10 THEN PRINT "(10) FILE COMPLETED":CLOSE #1:GOTO 420
5510 GOTO 5360
5520 INPUT "SHIELD IN";M$:REM *** TRANSMISSION LINE ***
5530 INPUT "CENTER 1N";I$:INPUT "CENTER OUT";O$
5531 PRINT #1,R6$+" * TRANSMISSION L1NE"
5532 PRINT #1,M$
5533 PRINT #1,I$
5534 PRINT #1,O$
5540 INPUT "SHIELD OUT";N$:PRINT #1,N$:GOTO 5570
5550 INPUT "NODE A";M$:PRINT #1,M$
5560 INPUT "NODE B";N$:PRINT #1 N$
5570 INPUT "Z0";Z$:PRINT #1,Z$
5580 INPUT "QUARTER-WAVE FREQUENCY (HZ)";L$:PRINT #1,L$
5640 GOTO 5360
5650 REM *** SHORTED STUB ***
5655 PRINT #1,R6$+" * SHORTED STUB"
5660 GOTO 5550
5670 PRINT #I,R6$+" * OPEN STUB":REM *** OPEN STUB ***
5680 GOTO 5550
5690 INPUT "NODE A";I$:INPUT "NODE B";J$:
     INPUT "RESISTANCE (OHMS)";V$
5700 PRINT #1,R6$+" * RESISTOR"
5702 PRINT #1,I$
5704 PRINT #1,J$
5706 PRINT #1,V$
5720 GOTO 5360
5730 INPUT "NODE A";1$:INPUT "NODE B";J$:
     INPUT "INDUCTANCE (H)";V$
5740 PRINT #1,R6$+" * INDUCTOR"
5742 PRINT #1,I$
5744 PRINT #1,J$
5746 PRINT #1,V$
5760 GOTO 5360
5770 INPUT "NODE A";I$:INPUT "NODE B";J$:
     INPUT "CAPACITANCE (FARADS)";V$
5775 PRINT #1,R6$+" * CAPACITOR"
5790 GOTO 5742
5800 INPUT "GATE";K$:INPUT "SOURCE";J$:INPUT "DRAIN";I$:
     INPUT "GAIN(MHO)";V$
5810 PRINT #1,R6$+" * FET"
5812 PRINT #1,K$
5814 PRINT #1,J$
5816 PRINT #1,1$
5818 PRINT #1,V$
5830 GOTO 5360
5840 INPUT "BASE";K$:INPUT "EMITTER";J$:INPUT "COLLECTOR";I$:
     INPUT "BETA";R5$
5850 INPUT "Rbe (OHMS)";V$
5860 PRINT #1,R6$+" * NPN TRANSISTOR"
5861 PRINT #1,K$
5862 PRINT #1,J$
5863 PRINT #1,1$
5864 PRINT #1,R5$
5865 PRINT #I,V$
5940 GOTO 5360
5950 INPUT "+IN";K$:INPUT "-IN";L$:INPUT "-OUT";I$:REM *** OP-AMP ***
5960 INPUT "+OUT";J$:INPUT "GAIN(V/V)";R5$:
     INPUT "OUTPUT RESISTANCE(OHMS)";V$
5970 PRINT #1,R6$+" * OP-AMP"
5972 PRINT #1,K$
5974 PRINT #1,L$
5976 PRINT #1,I$
5978 PRINT #1,J$
5980 PRINT #1,R5$
5990 PRINT #1,V$
6010 GOTO 5360
7000 ' SUBROUTINES FOR FILE HANDLING
7010 FOR J=1 TO 4:READ FL$(J,1):FL$(J,2)="N":NEXT J
7020 FOR J=1 TO 4
7030 IF FL$(J,2)="Y" THEN GOTO 7050
7040 PRINT STR$(J)+"- "+FL$(J,1)
7050 NEXT J
7060 PRINT
7070 INPUT "Choice (enter <cr> or 0 to exit)";C:C=INT(C)
7080 IF FL$(C,2)="Y" THEN PRINT "Already Selected!":GOTO 7070
7090 IF C=0 THEN RESTORE:RETURN
7100 PFG=1:INPUT "Name of Data File (<cr> for Directory)";F$
7110 IF LEN(F$)=0 THEN FILES:GOTO 7100
7120 FL$(C,2)="Y":OPEN "O",C,F$
7130 GOTO 7020
7140 DATA "Amplitude versus Frequency","Phase versus Frequency"
7150 DATA "Amplitude,Phase vs. Frequency","Amplitude vs. Phase"
7160 CLOSE
7200 FOR JJ=1 TO 4
7210 IF FL$(JJ,2)="N" THEN GOTO 7270
7220 ON JJ GOTO 7230,7240,7250,7260
7230 WRITE #1,R0,V:GOTO 7270
7240 WRITE #2,R0,U:GOTO 7270
7250 WRITE #3,R0,V,U:GOTO 7270
7260 WRITE #4,V,U
7270 NEXT JJ
7280 RETURN
```

APPENDIX B.2 Example of circuit data file for input to the program NET85.ASC. This file can be generated by the program itself or generated or modified by any text editor. The /* */ are delimiters for remarks and are not added by the program. They have been added for explanation of the file structure. Note that the file structure is the same as is input from the keyboard.

```
 1 * RESISTOR          /* Type of element (1 is a resistor) */
1                      /* Node A  */
2                      /* Node B  */
50
 1 * RESISTOR
4
7
50
 1 * RESISTOR
6
7
50
 2 * CAPACITOR
3
7
58E-12                  /* Value of capacitor in farads (58 pf */
 2 * CAPACITOR
2
5
23E-12
 2 * CAPACITOR
5
6
23E-12
 3 * INDUCTOR
2
3
72E-9                   /* This is a 72 nh inductor */
 3 * INDUCTOR
3
4
72E-9
 3 * INDUCTOR
5
7
28E-9
```

APPENDIX B.3 Sample output file from NET85.ASC. This data can be edited with any text editor, added to a report, or used by a plotting program, such as PCPLOT2 (BV Engineering, Riverside, CA):

(The first number is frequency, the second is amplitude.)

```
8E+07,3.543465E-02
8.269104E+07,3.831959E-02
8.54726E+07,4.173018E-02
8.834772E+07,4.599374E-02
9.131957E+07,.0516254
9.439138E+07,5.930689E-02
9.756651E+07,7.032793E-02
1.008485E+08,8.579546E-02
1.042408E+08,.1073953
1.077473E+08,.1368522
1.113717E+08,.1755944
1.15118E+08,.2237623
1.189903E+08,.2785856
1.229929E+08,.3333452
1.271301E+08,.3794872
1.314065E+08,.4116778
1.358268E+08,.430391
1.403957E+08,.4395925
1.45118E+08,.4434264
1.499998E+08,.4447783
```

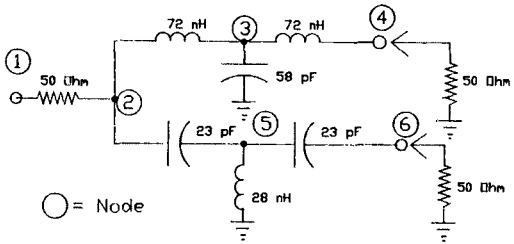

FIGURE 1

Prototype Diplexer Design

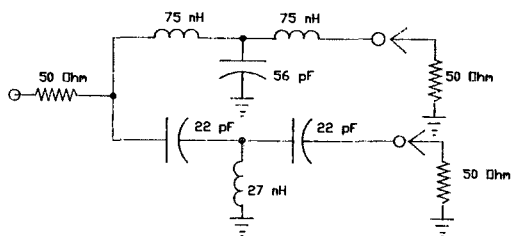

FIGURE 3

Diplexer Design using RETMA Values

LOW-PASS SECTION

FREQ=	8.0000E+07	AMPL=	4.56E-01	20LOG=	-6.8	PHASE=	-105.7
FREQ=	8.5000E+07	AMPL=	4.52E-01	20LOG=	-6.9	PHASE=	-113.1
FREQ=	9.0000E+07	AMPL=	4.49E-01	20LOG=	-7.0	PHASE=	-120.9
FREQ=	9.5000E+07	AMPL=	4.48E-01	20LOG=	-7.0	PHASE=	-129.1
FREQ=	1.0000E+08	AMPL=	4.47E-01	20LOG=	-7.0	PHASE=	-138.1
FREQ=	1.0500E+08	AMPL=	4.46E-01	20LOG=	-7.0	PHASE=	-148.2
FREQ=	1.1000E+08	AMPL=	4.42E-01	20LOG=	-7.1	PHASE=	-160.0
FREQ=	1.1500E+08	AMPL=	4.27E-01	20LOG=	-7.4	PHASE=	-173.6
FREQ=	1.2000E+08	AMPL=	3.94E-01	20LOG=	-8.1	PHASE=	171.2
FREQ=	1.2500E+08	AMPL=	3.40E-01	20LOG=	-9.4	PHASE=	155.7
FREQ=	1.3000E+08	AMPL=	2.75E-01	20LOG=	-11.2	PHASE=	142.0
FREQ=	1.3500E+08	AMPL=	2.13E-01	20LOG=	-13.4	PHASE=	131.6
FREQ=	1.4000E+08	AMPL=	1.62E-01	20LOG=	-15.8	PHASE=	124.7
FREQ=	1.4500E+08	AMPL=	1.25E-01	20LOG=	-18.1	PHASE=	121.1
FREQ=	1.5000E+08	AMPL=	9.77E-02	20LOG=	-20.2	PHASE=	120.1

HIGH-PASS SECTION

FREQ=	8.0000E+07	AMPL=	3.54E-02	20LOG=	-29.0	PHASE=	-136.8
FREQ=	8.5000E+07	AMPL=	4.11E-02	20LOG=	-27.7	PHASE=	-134.5
FREQ=	9.0000E+07	AMPL=	4.89E-02	20LOG=	-26.2	PHASE=	-130.4
FREQ=	9.5000E+07	AMPL=	6.12E-02	20LOG=	-24.3	PHASE=	-125.5
FREQ=	1.0000E+08	AMPL=	8.13E-02	20LOG=	-21.8	PHASE=	-121.8
FREQ=	1.0500E+08	AMPL=	1.13E-01	20LOG=	-18.9	PHASE=	-121.4
FREQ=	1.1000E+08	AMPL=	1.60E-01	20LOG=	-15.9	PHASE=	-125.3
FREQ=	1.1500E+08	AMPL=	2.22E-01	20LOG=	-13.1	PHASE=	-133.9
FREQ=	1.2000E+08	AMPL=	2.93E-01	20LOG=	-10.7	PHASE=	-146.4
FREQ=	1.2500E+08	AMPL=	3.57E-01	20LOG=	-8.9	PHASE=	-161.1
FREQ=	1.3000E+08	AMPL=	4.03E-01	20LOG=	-7.9	PHASE=	-175.9
FREQ=	1.3500E+08	AMPL=	4.28E-01	20LOG=	-7.4	PHASE=	171.0
FREQ=	1.4000E+08	AMPL=	4.39E-01	20LOG=	-7.1	PHASE=	160.1
FREQ=	1.4500E+08	AMPL=	4.43E-01	20LOG=	-7.1	PHASE=	151.0
FREQ=	1.5000E+08	AMPL=	4.45E-01	20LOG=	-7.0	PHASE=	143.4

FIGURE 2 - CALCULATED VALUES OF DIPLEXER

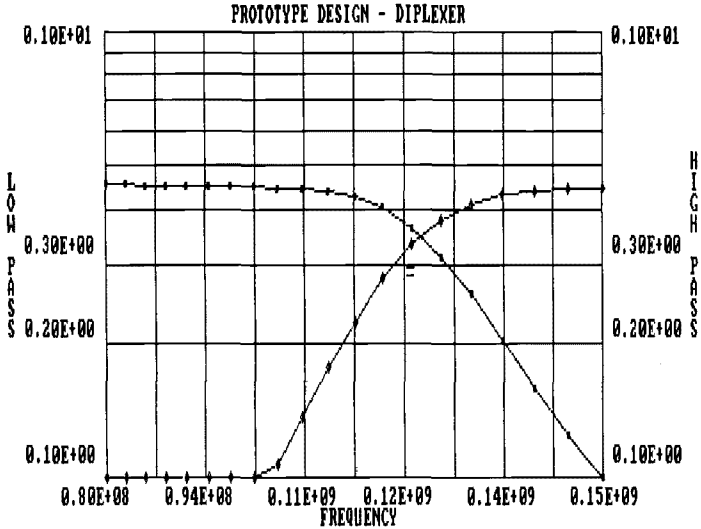

FIGURE 2(b)

LOW-PASS SECTION

FREQ=	8.0000E+07	AMPL=	4.62E-01	20LOG=	-6.7	PHASE=	-105.9
FREQ=	8.5000E+07	AMPL=	4.58E-01	20LOG=	-6.8	PHASE=	-113.4
FREQ=	9.0000E+07	AMPL=	4.55E-01	20LOG=	-6.8	PHASE=	-121.2
FREQ=	9.5000E+07	AMPL=	4.53E-01	20LOG=	-6.9	PHASE=	-129.4
FREQ=	1.0000E+08	AMPL=	4.52E-01	20LOG=	-6.9	PHASE=	-138.3
FREQ=	1.0500E+08	AMPL=	4.50E-01	20LOG=	-6.9	PHASE=	-148.3
FREQ=	1.1000E+08	AMPL=	4.46E-01	20LOG=	-7.0	PHASE=	-159.6
FREQ=	1.1500E+08	AMPL=	4.33E-01	20LOG=	-7.3	PHASE=	-172.6
FREQ=	1.2000E+08	AMPL=	4.06E-01	20LOG=	-7.8	PHASE=	172.8
FREQ=	1.2500E+08	AMPL=	3.59E-01	20LOG=	-8.9	PHASE=	157.5
FREQ=	1.3000E+08	AMPL=	2.99E-01	20LOG=	-10.5	PHASE=	143.2
FREQ=	1.3500E+08	AMPL=	2.36E-01	20LOG=	-12.5	PHASE=	131.3
FREQ=	1.4000E+08	AMPL=	1.82E-01	20LOG=	-14.8	PHASE=	122.6
FREQ=	1.4500E+08	AMPL=	1.40E-01	20LOG=	-17.1	PHASE=	117.0
FREQ=	1.5000E+08	AMPL=	1.08E-01	20LOG=	-19.3	PHASE=	114.2

HIGH-PASS SECTION

FREQ=	8.0000E+07	AMPL=	3.23E-02	20LOG=	-29.8	PHASE=	-134.9
FREQ=	8.5000E+07	AMPL=	3.73E-02	20LOG=	-28.6	PHASE=	-132.7
FREQ=	9.0000E+07	AMPL=	4.40E-02	20LOG=	-27.1	PHASE=	-128.6
FREQ=	9.5000E+07	AMPL=	5.45E-02	20LOG=	-25.3	PHASE=	-123.5
FREQ=	1.0000E+08	AMPL=	7.16E-02	20LOG=	-22.9	PHASE=	-119.3
FREQ=	1.0500E+08	AMPL=	9.88E-02	20LOG=	-20.1	PHASE=	-118.0
FREQ=	1.1000E+08	AMPL=	1.39E-01	20LOG=	-17.1	PHASE=	-120.7
FREQ=	1.1500E+08	AMPL=	1.94E-01	20LOG=	-14.2	PHASE=	-127.9
FREQ=	1.2000E+08	AMPL=	2.59E-01	20LOG=	-11.7	PHASE=	-139.1
FREQ=	1.2500E+08	AMPL=	3.24E-01	20LOG=	-9.8	PHASE=	-152.8
FREQ=	1.3000E+08	AMPL=	3.76E-01	20LOG=	-8.5	PHASE=	-167.3
FREQ=	1.3500E+08	AMPL=	4.09E-01	20LOG=	-7.8	PHASE=	179.2
FREQ=	1.4000E+08	AMPL=	4.27E-01	20LOG=	-7.4	PHASE=	167.6
FREQ=	1.4500E+08	AMPL=	4.36E-01	20LOG=	-7.2	PHASE=	157.8
FREQ=	1.5000E+08	AMPL=	4.40E-01	20LOG=	-7.1	PHASE=	149.6

FIGURE 4 - VALUES ADJUSTED TO NEAREST RETMA VALUES

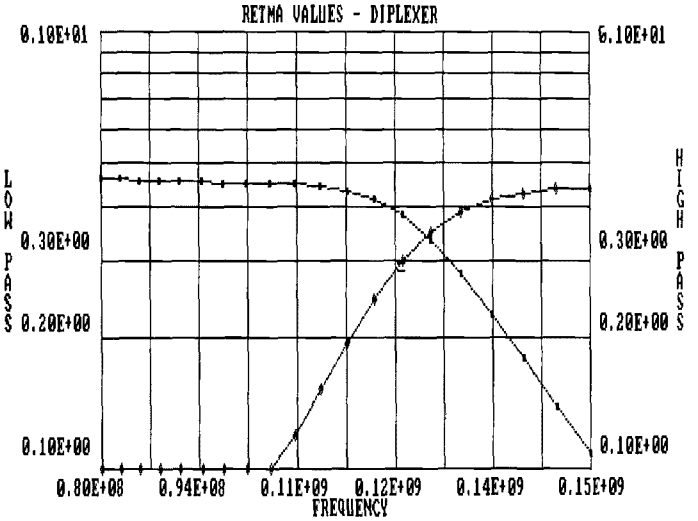
RETMA VALUES - DIPLEXER
0.10E+01
0.30E+00
0.20E+00
0.10E+00
LOW PASS
6.10E+01
0.30E+00
0.20E+00
0.10E+00
HIGH PASS
0.80E+08
0.94E+08
0.11E+09
0.12E+09
0.14E+09
0.15E+09
FREQUENCY

Figure 4(6)

SAW ACCELEROMETERS: INTEGRATION OF THICK AND THIN FILM TECHNOLOGIES

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INTRODUCTION

Surface Acoustic Wave (SAW) devices are now being used in many sensor applications[1-3] because of their inherent advantages (Figure 1). The ability to integrate the SAW delay lines with hybrid microelectronics to make compact, reliable units (Figure 2) and the requirement to obtain RF outputs directly proportional to the measurand (i.e., acceleration, pressure, vapor, etc.) have allowed this relatively new family of sensors to compete with other established sensor technologies such as capacitance and strain gauge type.

This paper describes how both thick and thin film processing technologies were combined to form a successful prototype SAW accelerometer intended for missile applications sensing ±50 Gs.

BASIC DESIGN AND OPERATION

The discussion on the basic design and operation of this accelerometer centers on its key sensing element, the SAW delay line. Since cost and size were not a major emphasis in this developmental program, a custom machined, two-tier, connectorized package (Figure 3) was designed to support and protect the SAW line and house the hybridized electronics.

Mechanical Design

Initially, two standard SAW materials were investigated; Y-Z lithium niobate and ST-X quartz. These materials were chosen for the following reasons:

1. Historically they have been the most popular substrates used for SAW devices. $LiNbO_3$ is used for its high piezoelectric coupling and SiO_2 is used for its thermal stability.
2. Material constants for these particular crystalline cuts are well known, thus allowing the SAW velocity change due to strain to be predicted.
3. These materials have better mechanical properties than other candidate materials, leading to better production yields and a more rugged accelerometer.

The mechanical configurations investigated were those which were readily derivable from these standard SAW materials and those providing maximum strain at the surface of the SAW substrate. Mechanical analysis of several configurations was performed and resulted in how the SAW substrate velocity changed as a function of applied stress, mechanical dimensions, material constants, etc. This analysis concluded that the cantilever beam approach required the least force to achieve a given strain and hence SAW velocity change (Figure 4). The force ($F_\perp$) applied to the cantilever beam is provided primarily by the acceleration field acting upon a seismic mass attached to the beam's end. In this cantilever beam configuration the mechanical calculations for strain and the material constants demonstrated that ST-X quartz has nearly twice the sensitivity of lithium niobate, thus making quartz the material selected

for the SAW accelerometer prototypes.

Electrical Design

The basic design used for the SAW accelerometer prototypes consisted of a single SAW oscillator (fo = 314 MHz) driving twin cantilevered SAW delay lines. One delay line is used as a reference and the other is stressed or "deformed" under acceleration by the seismic mass. The intent of this twin delay line configuration is to minimize any temperature effects between the two lines. The two outputs are fed to a phase detector to compare the relative phase shift due to a velocity change in the stressed substrate. The phase detector output is then amplified and used to produce both DC analog and RF outputs proportional to the applied acceleration force.

BASIC FABRICATION AND ASSEMBLY

The electronics circuitry for the accelerometer was fabricated as a thick film hybrid circuit on a 1" x 0.8"x .025" alumina substrate. The main electronics board contained a SAW oscillator, power divider, phase detector, amplifier section, and V-to-F circuit (Figure 5). The two delay lines and their tuning elements were mounted on a separate base plate and attached to the bottom of the package by screws (Figure 6).

PRELIMINARY TUNING

Prior to package assembly it was necessary to functionally adjust the reference SAW delay line to 90 degrees phase difference in relation to the deformable SAW delay line. This insured maximum sensitivity of the phase detector to any stress in the deformable cantilever. The package and baseplate fixtures were connected such that the outputs of the power divider were injected into both cantilevered SAW lines. The outputs of both the reference and deformable SAW lines were then fed back into the phase detector on the main electronics board. The DC amplifier output was then monitored and the reference cantilever was adjusted by means of locking screws on the seismic mass. When maximum amplifier output was obtained the reference cantilever screws were locked in place.

With the reference SAW line now held stationary, the deformable SAW line was manually deflected and the amplifier output checked. The result was approximately a one volt shift at full scale deflection.

The R-C circuitry on the V-to-F section was now adjusted to give a stationary output difference frequency of 550 KHz $\pm$ 25 KHz. This was necessary due to the fact that, because of individual SAW characteristics, component tolerances, etc., the stationary amplifier output varied.

TESTING RESULTS

Four prototype devices were built and tested for the following parameters:

1. Linearity
2. Sensitivity
3. Hysteresis
4. Effects of temperature
5. Transverse Sensitivity

The basic procedure for testing the SAW accelerometers was to mount them onto a centrifuge and calculate the acceleration by converting RPM into Gs. The acceleration was incremented in steps of 5 Gs and the DC output voltage monitored and recorded for each acceleration point.

Linearity and Sensitivity

The SAW accelerometers were tested for the linearity and sensitivity at ambient, hot, and cold temperatures. The results of the ambient temperature runs on two units can be seen in Graph #1 entitled "SAW-DC Voltage vs. Acceleration". From this graph it can be seen that the two units displayed a very linear relationship between acceleration and output voltage. The sensitivities of both units differed from around the zero acceleration point to the acceleration extremes. See Table below.

Acceleration	SAW 2	SAW 3
50 Gs	2.6mV/G	5.2mV/G
0 Gs	6.6mV/G	7.8mV/G
-50 Gs	7.8mV/G	9.5mV/G

It must be noted that the cantilevered structures were designed to maximize +G deflection and limit -G travel to save package space.

Hysteresis

The hysteresis of the SAW accelerometer was found by measuring the DC output voltage while incrementing the acceleration from zero to +50 Gs and decrementing back to zero. This procedure was repeated for negative acceleration. A typical SAW hysteresis curve can be seen in Graph #2 "SAW Accelerometer HYSTERESIS". From this graph it can be seen that there is a minimal amount of lag and the accelerometers deviated from their initial measured value by a maximum of 5 mV and 11 mV respectively.

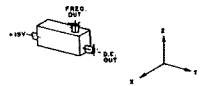
Effects of Temperature

The effects of temperature were measured by cooling or heating the SAW device and then placing the unit inside an insulated box and running the tests. Raising and lowering the temperature generally had the effect of raising and lowering the operating point. Raising and lowering the temperature also effected the sensitivity of the SAW units. Sensitivity increased to -9.46mV/G when cold (-25F) and decreased to -7.0mV/G when hot (150F). Sensitivity at ambient temperature is -7.89mV/G. This phenomenon is probably due more to semiconductor physics than the SAW temperature sensitivity. Saturation current through the phase detector diodes will increase with temperature and thereby reduce phase detection sensitivity. These effects can be compensated for with additional electronics.

NOTE: The operating point of the accelerometer at times shifted around irrespective of operating conditions. This explains why the hot curve is lower than the ambient curve in Graph #3 "SAW Accelerometer Temperature Effects". In general the operating point for this particular unit lowered with use.

Transverse Acceleration

Transverse acceleration is a critical in missile applications because acceleration occurs in more than one axis as the missile maneuvers. However, transverse acceleration was found to have very little if no affect on the DC output voltage. See Table below.



X direction is axis of desired motion

Y direction acceleration has no affect at all

Z direction acceleration has 0.2mV/G sensitivity

Summary of Testing Results

The SAW accelerometers exhibited a reasonably linear relationship between output voltage and acceleration. The units did display some offset and sensitivity drift with temperature variations. The offset voltage increased with a temperature increase and sensitivity increased as temperature decreased. Transverse acceleration is not a problem and hysteresis effects also don't appear to be a problem but more testing is needed to confirm this. The most common problem encountered in testing the units was that the offsets were at times unpredictable and often took a long time to stabilize.

In general, the SAW accelerometers worked well for prototypes. There were problems encountered in the testing that pointed to the associated electronics and mechanical mounting. Several improvements to overcome these problems will be addressed in the next phase of development.

CONCLUSION

This development program on SAW accelerometers proved very successful. The acceleration versus output voltage data was linear and reproducible to ±50 Gs. Size and cost reductions are being pursued in a follow-on developmental program which will provide a low profile, surface mountable package.

REFERENCES

[1] "A Surface Acoustic Wave Gas Detector", A. Bryant et.al., 1981 Ultrasonics Symposium Proceedings, pp 171-174.

[2] "Cantilever-Beamed SAW Accelerometers", P. L. Meunier and P. Hartemann, 1982 Ultrasonics Symposium Proceedings, pp 299-302.

[3] "Temperature Sensor Using SAW Delay Line", D. Hauden et.al., 1981 Ultrasonics Symposium Proceedings, pp 148-151.

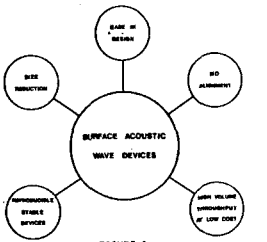


FIGURE 1
Reasons to Use SAW Devices

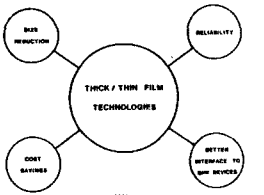


FIGURE 2
Reasons to Use Thick/Thin Technologies with SAW Devices

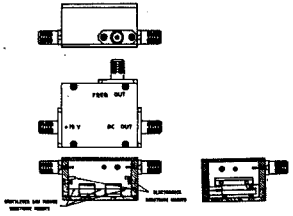


FIGURE 3
SAW Accelerometer
Package Assembly

FIGURE 4
Cantilever Beam

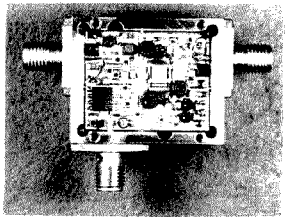


FIGURE 5
Electronics Substrate

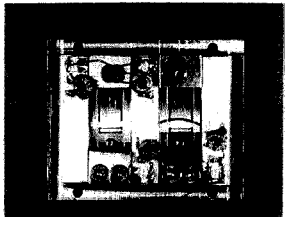
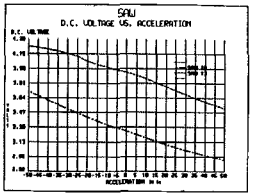
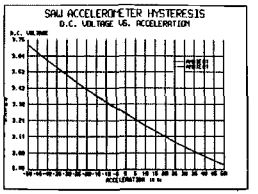


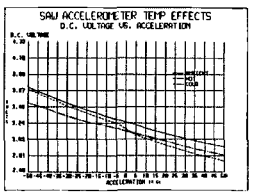
FIGURE 6
Cantilever SAW Substrate
with Tuning Components



GRAPH 1



GRAPH 2



GRAPH 3

IMPROVE SYNTHESIZED TRANSCEIVER PERFORMANCE AND RELIABILITY BY SIMPLE SCREENING OF THE VCO ACTIVE DEVICE

ABSTRACT:

This article describes the effect of 1/*f* noise from high frequency bipolar junction transistors on the performance of a synthesized transceiver; and it offers an explanation for the origin of the noise together with a simple screening technique to improve the transceiver performance and reliability.

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Introduction:

A basic element of frequency synthesized transceivers is the phase-lock loop circuit in which the output of a voltage-controlled oscillator (VCO) is constantly compared with the frequency of a reference crystal controlled oscillator. Synthesized transceiver performance is mostly based on the choice of design parameters for the phase-lock loop circuit. A compromise in loop bandwidth will optimize the desired switching speed with respect to the specified spurious output levels. The phase noise sources in the phase-lock loop [1, 2] are responsible for the spectral purity of the transceiver. The close-in phase noise will affect the residual FM hum and noise performance as well as the transceiver adjacent channel selectivity specifications.

To achieve good close-in phase noise, it is necessary to maximize the resonator's loaded Q and its available output power while choosing an active device with a low noise figure and a low 1/*f* noise contribution. This article describes the effect of 1/*f* noise from high frequency bipolar junction transistors on the performance of a synthesized transceiver; and it offers an explanation for the origin of the noise together with a simple screening technique to improve the transceiver performance and reliability.

Cause and Effect of 1/*f* Transistor Noise:

The major cause of 1/*f* noise in bipolar transistors has been traceable to surface properties. Surface contamination or defects can degrade 1/*f* noise performance and transistor reliability by creating early failures in the field.[3]

The 1/*f* transistor noise caused a degradation in the VCO phase noise in the synthesized transceiver; distinctly affecting the residual FM hum and noise and the

adjacent channel selectivity performance. The $1/f$ transistor noise was first verified by the -9dB per octave slope of the single-sideband phase noise spectral density, $L(fm)$ plot.[4] The high frequency bipolar transistor noise was then amplified in a low noise amplifier and recorded on a low frequency spectrum analyzer.

The transistors with excessive $1/f$ noise showed a relatively low DC beta and a large difference in the absolute value of this parameter at different collector currents. Thus, a simple characterization of the DC beta of the VCO active device can improve synthesized transceiver performance and reliability.

Transceiver Performance Background:

The transceiver includes a transmitter and a receiver section coupled to the frequency synthesizer which generates the appropriate injection signals to allow the transmission and reception of the carrier frequency.

The transmitter residual FM hum and noise specification is a measurement of the signal-to-noise quality of the transmitter within a specified bandwidth. Specifically, it denotes the ratio of residual frequency modulation to standard test modulation measured on a test receiver. In a narrowband system the standard test modulation is 60% of the 5 kHz maximum system deviation, and the test receiver bandwidth is in the audio voice pass-band range of 300 to 3000 Hz.

The synthesizer characteristics play a major role in determining the receiver selectivity specification; in particular, the close-in phase noise. Receiver selectivity is a measure of channel protection against undesirable signals close to the receiver carrier frequency. This is typically measured at the adjacent channel frequency, and it serves as a figure of merit for different types of receivers.

The transmitter sideband noise is also directly influenced by the phase noise at the output of the voltage controlled oscillator which serves as the injection frequency for the transmitter section.

Transceiver Degradation Due To $1/f$ Noise:

The residual FM hum and noise level of the VCO varied in excess of 20 dB from a maximum measurement of -36 dB. (ratio in dB of the test modulated audio to the residual noise audio level). The inconsistent VCO hum and noise levels were traced to the $1/f$ noise of the active device in the oscillator circuit.

The spectral response of the voltage controlled oscillator was measured using a double balance mixer as a phase detector in a narrow bandwidth loop to maintain phase quadrature with the reference source.[5] This setup was capable of measuring better than -140 dB/Hz from the reference source. A plot of the spectral density response for two different bipolar transistors from the same generic lot measured on the same VCO is shown in Figure 1.

The difference shown in the spectral density plot is due to the higher $1/f$ transistor noise. The characteristic -9 dB per octave slope is clearly shown on the top trace of the plot, while the spectral density slope for the good device (bottom trace) shows the -6 dB per octave normally associated with the white FM noise.

The adjacent channel receiver selectivity, 25 kHz from the carrier frequency, was also degraded by 5.5 dB for the measurements taken with the samples outlined on Figure 1. After tracing the transceiver degradations to the active device of the oscillator circuit, the high frequency bipolar transistor was fully characterized.

Bipolar Transistor Characterization:

The $1/f$ transistor noise was amplified and recorded on a low frequency spectrum analyzer. An audio amplifier was built with the high frequency bipolar transistor to amplify its own internal noise, and its output was passed through two additional stages of low-noise operational amplifiers. An overall gain of 100 dB was obtained from these amplification stages which served to drive the low frequency spectrum analyzer.

The noise spectral density for several transistors is shown in Figure 2. These pictures illustrate the different noise patterns observed.

The VCO residual FM hum and noise was measured for several transistors, then the spectral density was recorded on the low frequency spectrum analyzer, and finally the DC beta at the operating collector current (5mA) was measured for each device. A graph illustrating the correlation among these variables is shown in Figure 3.

The noise voltage at 1 kHz versus beta graph (Figure 3) shows a strong correlation of the high noise bipolar transistors responsible for the poor hum and noise levels to the low DC beta values recorded. In particular, transistor noise levels below $3nV\sqrt{Hz}$ at 1 kHz were found to correspond to VCO hum and noise levels lower than -52 dB.

However, since the residual FM hum and noise is measured in the audio voice pass-band range rather than at a specific frequency, a more accurate means of measurement was developed. This consisted of a noise test system whose output was a DC voltage level resulting from rectifying and integrating the $1/f$ noise in the specified audio bandwidth. A block diagram of the new noise test system is shown in Figure 4.

The amplified transistor noise was band limited from 300 to 3000 Hz with a 750 µsec preemphasis filter, processed through a full wave rectifier and integrated over a seven second period. The result of the integration was a DC voltage level proportional to the $1/f$ transistor noise. Figure 5 shows the relation of the rectified band limited noise voltage to the measured hum and noise levels. This graph also correlates an average DC noise voltage threshold limit of 0.5 Vdc to a VCO hum and noise acceptable level of -51 ± 1 dB.

Furthermore, Figure 6 shows the more accurate relationship of the rectified DC noise voltage to the hum and noise measurement and the oscillator transistor DC beta. This graph shows that the majority of the transistors with DC betas higher than 90 at 5 mA collector currents (VCE = 5V) had good VCO hum and noise performance. Further tests on a larger number of the same generic type transistors have shown a similar correlation (Figure 7).

Moreover, data at different collector currents was also taken, specifically at 5 mA and 10 µA. This data showed that the transistors with high noise levels demonstrated a large difference in these two collector currents. Refer to Figure 8.

Separate batches of transistors from different lots were specifically tested for noise, DC beta and the beta difference at different collector currents. In general, all transistors with betas higher than 90 showed low noise voltage levels and fairly close DC beta readings at the two collector currents mentioned. One batch of the high beta transistors (ßave = 130) showed high average noise voltage levels, but a large difference in DC betas at these two collector currents also was characteristic of this batch of transistors (beta difference was greater than 60).

1/f Noise Correlation To Surface Effects:

The major cause of 1/f noise in semiconductor devices is traceable to surface properties of the materials. The generation and recombination of carriers in the surface energy states and the density of surface states are important contributing factors. The 1/f noise has decreased with improved surface treatments in manufacturing, but even the interface between the silicon surface and the grown oxide passivation can create 1/f noise sources.[3]

Three distinct sources of low-frequency noise in bipolar junction transistors have been reported in the literature:[6]

1. A 1/f noise source associated with the surface of the emitter-base junction,
2. A 1/f noise source associated with the active base region of the transistor, and
3. Anomolous burst noise associated with the forward-biased emitter-base junction.

The noise spectral density of the transistors shown in Figure 2 correlates to these reported findings.

A good NPN high frequency transistor is designed with a narrow base width to reduce the transit time of the minority carriers, and with small emitter and collector areas to reduce junction capacitance.[7] A common fabrication technique uses interdigitated (emitter-base) geometries to increase the useful emitter edge length while keeping the overall emitter area to a minimum. This technique maximizes the perimeter-to-area ratio so that most of the emitter current will pass through the periphery, avoiding the large series resistance of the extremely thin base region.

Thus, the increased amount of current flow through the surface junction periphery tends to make the high frequency transistor more susceptible to surface defects. In contrast, low frequency (audio) transistors tend to have lower 1/f noise because their emitter geometries are designed to minimize the perimeter-to-area ratio so that more of the emitter current will avoid the periphery.

1/f Noise Correlation to DC Beta:

The basic operation of the NPN bipolar transistor consists of the injection of electrons from the emitter as minority carriers into the base region. Through the diffusion process they are collected at the collector region. The design objective for an efficient transistor is to match the number of electrons arriving at the collector to those being injected by the emitter. However, because of the electron-hole-pair (EHP) recombination at the base through the bulk and the surface, a 100 percent efficiency is never achieved. The holes required for the EHP recombination are supplied by the base current. In addition, the hole current that flows across the base to the emitter junction is also supplied by the base current.

The narrow base region width requirement minimizes the EHP recombination at the bulk, while recombination at the surface is best treated with careful and clean processing steps. Some of the Si-SiO_2 surface charge mechanisms reported are:[8]

1. Space charge within the oxide due to mobile contaminant ions (such as sodium),
2. Energy "traps" due to ionizing irradiation of the silicon sample,
3. Fast surface states which occur because of disruption of the periodicity of the lattice at the surface, and
4. Fixed surface state charge, Qss.

Since the DC beta (base to collector current amplification factor) is the ratio of collector

current to base current, the EHP recombination mechanism is a major contributor to this amplification factor. Consistently, for a given emitter current, if there is additional recombination due to surface effects, a larger number of electrons will recombine with the holes at the base and surface, decreasing the collector current and dropping the DC beta.

The surface effects and $1/f$ noise on high beta devices tend to be less noticeable because of the larger collector currents, but severe $1/f$ noise in high beta devices could still degrade the transceiver performance. For this reason, the difference in DC betas at separate collector currents became a second screening mechanism. A large beta roll-off at the low collector current of 10 μA, compared to the operating collector current of 5 mA, has been observed on devices with high $1/f$ noise, whereas normal devices have exhibited a minor beta roll-off (a difference of 10-20) due to the smaller number of electrons available for the EHP recombination.

In general, transistors with a high DC beta at low collector currents did not exhibit excessive $1/f$ noise.

Excessive $1/f$ Noise - A Reliability Predictor:

Correlation exists between high values of $1/f$ noise and poor reliability. It has been reported in reference 3 that artificial aging experiments have correlated excessive $1/f$ noise with the probability of early failure. The artificial aging experiments have noted that a large increase in $1/f$ noise occurs just prior to device failure, and units with low initial values of noise have demonstrated a longer life under these artificial conditions.

In a separate noise testing study for reliability screening[9], defective devices from tested samples showed abnormally high noise levels compared to the majority of good samples. The study concluded that defective samples can be identified and rejected using noise testing methodology based on $1/f$ noise.

In addition to the surface effect mechanisms covered, excessive $1/f$ noise may be the result of defective contacts, fractures or irregularities at the emitter-base junction which could also cause an early transistor failure. Early screening of the excessive $1/f$ noise devices will improve the reliability of the circuit and hence the system in which they will operate, in our case, the synthesized transceiver.

Conclusion:

Excessive $1/f$ noise in the active device of the VCO was shown to degrade the performance of the synthesized transceiver. Spectral purity, transmitter residual FM hum and noise, and receiver selectivity were degraded by the transistors with $1/f$ noise problems.

Noise testing on a large sample of high frequency bipolar transistors from different manufacturing lots showed a strong correlation for low noise transistors to high DC beta samples and especially at low collector currents.

Therefore, a simple screening of the VCO active device for high DC beta and a small difference in this parameter at the two specified collector currents could improve the synthesized transceiver performance and reliability.

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Figure 1 : Single Sideband Phase Noise 1Hz Bandwidth vs. Carrier Frequency Offset

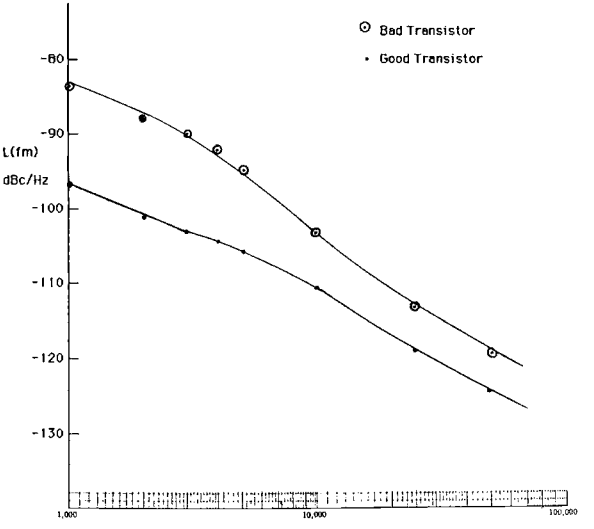


FIGURE 2

Noise spectral density of high frequency transistors

The spectrum analyzer setting

Bandwidth	300 Hz
Vertical Scale	dbv with +10 db offset
Horizontal Scale	1 KHz/Div
Noise Gain	100 db

Each photograph shows two traces; the bottom trace is the reference transistor, while the top trace is the device under test.

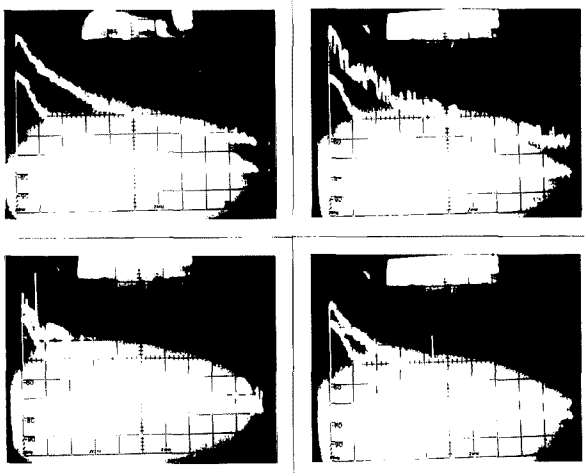


Figure 3 : Noise Voltage at 1kHz vs. DC Beta (Sample Size 83)

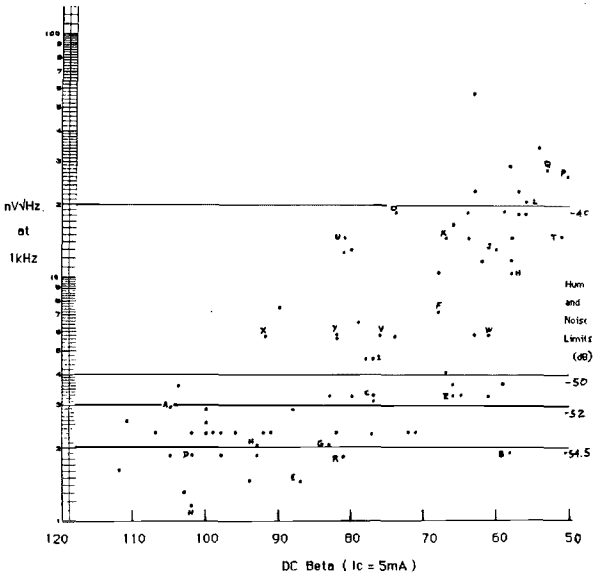


Figure 4 : Noise Test Fixture Block Diagram

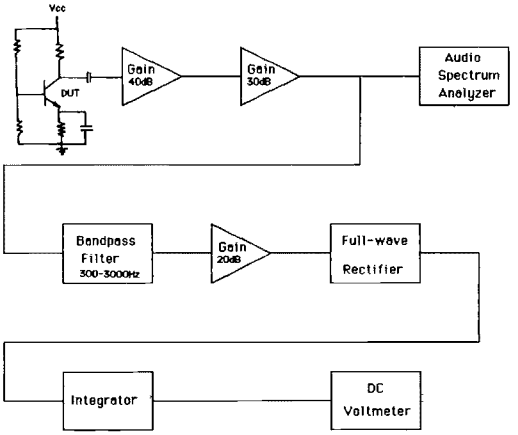


Figure 5 : Rectified DC Voltage vs. Hum and Noise

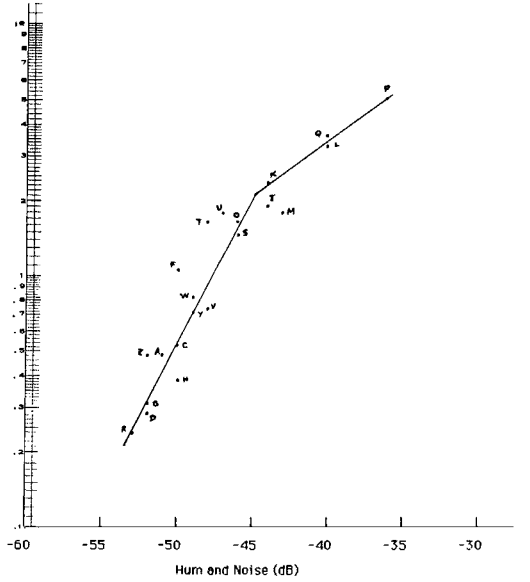


Figure 6 : Rectified DC Voltage vs. DC Beta (Sample Size 45)

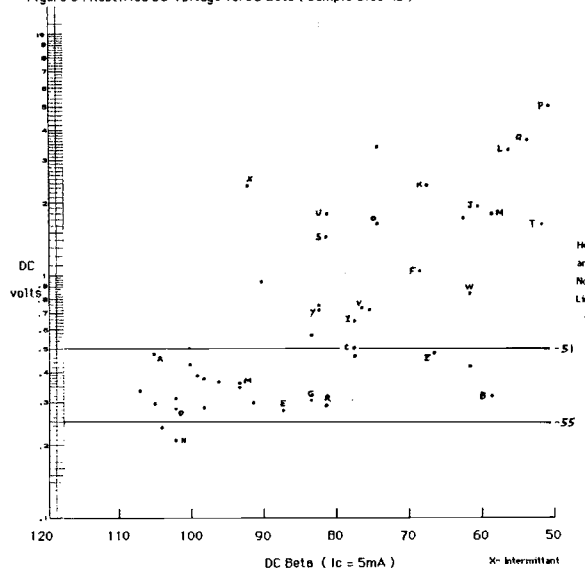


Figure 7 : Rectified DC Voltage vs. DC Beta (Sample Size 106)

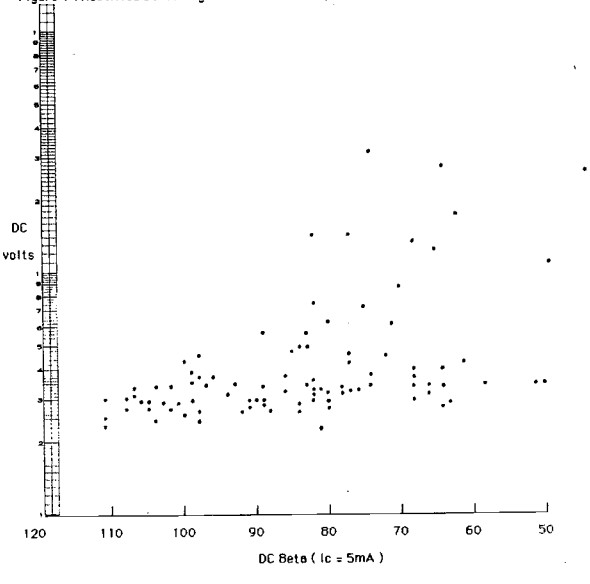
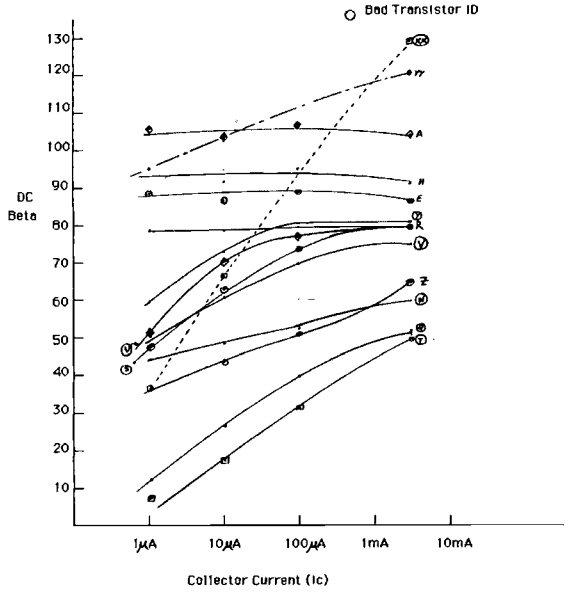


Figure 8 : DC Beta vs. Collector Current



A CAD DESIGN PROGRAM FOR ANALYSIS OF ELECTRO-THERMAL COUPLING IN HIGH POWER RF BIPOLAR TRANSISTORS

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ABSTRACT

A sophisticated thermal analysis program for CAD and CAE in the field of high frequency bipolar power transistors is presented. It is shown to agree with the experimental observations of phenomena associated with RF transistor operation, namely, electro-thermal interactions. Temperature, and current density distributions are analyzed and presented as a function of power density, RF and DC operation, total emitter ballasting, contour emitter ballasting, ambient temperature, and cell splitting. A figure of merit to describe current uniformity across the active area is introduced. The method of solution and modeling of transistor electro-thermal coupling is discussed.

INTRODUCTION

The push in solid state amplifier design has constantly been toward both higher frequency and power requirements. This only emphasizes the need for quantitative understanding of the coupling between the two major physical phenomena present in transistor operation, namely, electrical and thermal behavior. Both are intimately related to device performance that is crucial to the amplifier designer. These are reliability and efficiency issues, which although they appear to be at opposite ends of the performance spectrum at first thought, are indeed very much tied together.

Efficiency ultimately can always be related to current uniformity over the transistor cell. This itself is tied to both the temperature distribution over the cell and the vertical structure of the transistor, such as collector thickness, collector resistivity, base profile, etc. Horizontal factors such as finger spacing, cell spacing, and resistor ballasting also play a major role. Reliability is usually thought of in terms of maximum junction temperature because of its direct impact on mean time to failure. Other reliability issues include current distribution (ie. current densities which can not be verified directly experimentally), and catastrophic failure due to thermal runaway usually due to misuse of the device.

Other researchers have solved the temperature distribution problem for uniform and even arbitrary power distribution for idealized transistor-like structures. These solutions include both analytical and numerical models. The result generally is the temperature distribution for the entire device. These works are adequate in those regimes when the temperature and current distributions are not extreme, ie., when the temperature and current distributions are independent of each other. It is common knowledge that

current injection for the transistor as a whole is very much dependent on temperature, but this dependence is much more pronounced for the transistor locally. High current injection aggravates high temperatures, which in turn promote even higher current injection, which results in even higher temperatures. This process, known as current localization, can easily lead to thermal runaway. The normal RF transistor in fact operates under these aggravated conditions of high current densities and high temperatures, and the results of the works mentioned above cannot be used.

In this paper we report the simultaneous solution of this coupled problem (when it exists, ie., no thermal runaway). Our own work resulted in a digital computer program TEMP3D that is easy to use, requiring a minimum of inputs, and is built around an extremely robust algorithm.

MODEL DESCRIPTION

Because the thermal time constants involved are long compared to the exciting frequencies (in the RF range) we concern ourselves with the steady state case. TEMP3D solves for the surface temperature distribution in the active regions of the RF transistor. These regions may consist of a single cell or a multi-celled array. Each cell is composed of an array of emitter fingers. TEMP3D also provides the current distribution over these fingers. The results, both current and temperature, can either be tabulated or plotted.

Thermal Model - 3 Dimensional Heat Transfer Problem

The algorithm for the calculation of the temperature distribution is based on an analytical solution of the three dimensional problem for surface temperatures.

$$\nabla^2 T(x,y,z) = 0 \qquad (1)$$

The solution for the temperature at the surface T(x,y,0) takes on the following form:

$$T(x,y,0) = \int\int \Phi(x,y;x',y') P(x',y') \, dx'dy' \qquad (2)$$

where $\Phi(x,y,x',y')$ is the Green's function for (1). The analytical solution is derived with the assumption that the heat distribution P(x,y) developed at the surface is known. The temperature at the bottom of the chip is held constant and uniform. The chip is homogenous and uniform. The dependence of the thermal conductivity K of silicon is described by the expression

$$K = A_0 * T \wedge B \qquad [Watts/cm/K] \qquad (3)$$

where A_0, B are constants that depend on the bulk resistivity of the silicon substrate and T is the temperature in Kelvin.

Electrical Model - Transistor Action

The electrical behavior of the device is treated by breaking up each emitter finger in all cells into a number of identical transistors whose electrical parameters are derived from an appropriately scaled version of the entire device. These individual model transistors are coupled by means of base and emitter resistors to

make a single emitter finger (figure 1). Furthermore, these emitter fingers are coupled to one another via emitter ballasting resistors which may or may not be equal. The constraints for the electrical problem are that the total collector current and collector voltage are given, and the base-emitter voltage is the same for all finger transistors. The model for the nodal transistors is derived from a modified Gummel-Poon model which includes high current beta rolloff. The current injection of each elementary transistor is effected by the local temperature at that node. The current distribution calculation reflects either a DC or Class A RF solution, or high frequency Class C operation where the low frequency beta is scaled with the ft of the device.

Electro-Thermal Coupling

The solution to the total problem requires the simultaneous solution to both the thermal and electrical problems as described above so that each problem is consistent with the conditions imposed on it by the other. Namely, the electrical solution is to be consistent with the temperature distribution as dictated by the thermal problem. Similarly, the thermal solution is to be consistent with the power (current) distribution as calculated by the electrical problem.

The solution to the total problem being nonlinear in nature requires some kind of iterative scheme. The electrical problem being intrinsicly nonlinear ($I \sim \exp(V/Vt)$) is also solved by iteration. Only the thermal problem including the nonlinearity of the thermal conductivities is put into such a form that the solution is given by exact techniques, or rather an analytic form.

The algorithm for the solution of the total problem can be seen readily in figure 2. First, a uniform current distribution is assumed, and the corresponding temperature distribution is calculated. This thermal distribution provides the assignment of operating temperatures to the individual nodal transistors. For this thermal profile, the common emitter-base voltage for all fingers is the only parameter which uniquely defines the current at each nodal transistor. The appropriate value for this emitter-base voltage satisfies the condition that the total collector current is conserved.

Normally, the resulting nodal currents will not be consistent with the power distribution previously used to calculate temperatures. If this were the case, this would mean a self-consistent solution pair for both temperature and current has been obtained. However, a new temperature distribution needs to be calculated based on the latest solution to the electrical problem. From this resulting temperature distribution a new set of nodal currents can be calculated. This process is repeated until self consistency is reached.

The determination of the emitter-base voltage, however, is not so straight-forward. It is complicated by the fact that the nodal transistors are not coupled directly to one another. This is true only

on a finger level. The nodal transistors that belong to one finger are decoupled from the next by means of the external emitter finger ballasting resistors. In practice, this means that the same problem exists on the finger level that exists for the total device. Each emitter finger has its own unique potential that satisfies conservation of current in that finger.

The iteration procedure described above results in the electrical and thermal solution for the DC case. This solution can also be used for Class A RF applications where the RF power is small compared to the DC power dissipation. This analysis is also applicable to Class C operation by modifying the injection efficiency of the transistor. In this case the transistor current gain should be scaled down and determined by Ft and the operating frequency:

$$beta = beta0 / sqrt(1 + (beta0 * f / Ft)^2) \quad (4)$$

where beta0 is the DC current gain, f the frequency of operation, and Ft is the current gain bandwidth product.

Computational Considerations

Like any other numerical solution that approximates a continuum by discretization, the accuracy improves with the number of nodes. In the same manner, this increases the time required for calculation. Specific to our problem, the time necessary for the calculation of temperature increases with the square of the number of points. For the electrical problem which involves three nested loops (node current, finger current, and emitter-base voltage), the computational effort also increases rapidly with the number of nodes. By taking advantage of symmetry which most real devices employ the computational time required was observed to be reduced by a factor of 10.

Additional reduction in the cost of computation was achieved by the use of look up tables for eliminating redundant calculations. Special efforts were made in accelerating the convergence of the algorithm by using improved prediction methods.

The time required for a typical example (1 cell, 550 nodes, well ballasted, moderate power dissipation ~ 11 kW/cm2) was about 300 CPU seconds on a PRIME 750.

User Inputs/Parameters

The inputs for program use can be broken up into two categories: those that describe horizontal configuration, those that describe the device's vertical parameters, and those that describe operating and boundary conditions.

The horizontal parameters that determine device performance include:

- chip dimensions

- chip thickness

- cell configuration - to itself and to chip

- emitter configuration in the cell

- emitter ballasting distribution (Re)

  uniform or arbitrary on a finger basis

Vertical parameters which characterize a particular transistor process include

- epi thickness and resistivity

- Gummel-Poon parameters

- parasitic emitter resistance

- two dimensional injection effects
  extrinsic base resistance - rb'
  knee current

- ft

finally, transistor operating conditions are input. These include:

- bottom chip temperature

- total collector current

- collector voltage

- operating frequency

RESULTS

Benchmark Problem

For purposes of illustration a model to be used as a benchmark will now be considered. It represents a typical RF transistor with ft on the order of 5 GHz and saturated output capability of 1 W at 1 GHz. This structure as seen in figure 3 consists of 50 emitter fingers, 2 microns wide, spaced 4 microns apart. Each emitter finger has its own ballast resistor of 80 ohms, which makes for 1.6 ohms for the whole device. The total base area is 17 by 1.2 mils. Chip size is 25 by 18 mils, and 4.5 mils thick.

The benchmark operating conditions for purposes of comparison, are Ic = 100mA, Vce = 15 V, and Tmin = 60C. The typical printed output for the solution of this problem under these conditions can be seen in figure 4.

This data is organized into three parts. The first of these is a short summary that reports the minimum and maximum temperatures and nodal currents and the asscociated fingers. This is done for each cell in the structure. It should be noted that all currents unless noted are normalized to the current that would exist if the current were uniformly distributed across the device. Also seen is the heading "% AREA USED" which is a figure of merit that describes uniformity in current distribution across the cell.

The next section describes the temperature and current profiles along the fingers (y axis microns) that were selected

in the previous part for extrema in temperature and current.

The last part of the printout is a detailed summary on a finger by finger basis for each cell. Included are the temperatures and currents at both ends and center of each finger. Also included is the total finger current normalized and in mA as well as the ballast resistance associated with that finger.

As can be seen for this benchmark case the maximum temperature and current occur in the same finger, number 26. This maximum junction temperature of 114 C occurs in the same finger where the current is 13.5% greater than nominal. The minimum current and temperature occur at the corner of the cell in finger number 1. the temperature here is 87 C and the current is only 81% of nominal. As seen in the summary for all fingers, the variation in finger currents is only 10.7% while the variation in nodal current over the whole device is 28.5%. This uniformity in finger current is due to strong emitter ballasting, while there is no mechanism to force uniform current distribution along the finger.

The same data is effectively presented graphically in figures 5 and 6. temperature and nodal current are plotted as a function of finger positioned for cross-sections along the center of the cell and cell edge. It is evident that even for these benign operating conditions there is a noticeable variation in temperature and current from center to edge.

Figures 7 and 8 present similar data for temperature and current, except that the independent variable is position along the finger. Chosen for illustration are the hottest and coolest fingers at the center and end of the cell respectively.

In figure 9 total finger current in mA is plotted as a function of finger position. The sum of these finger currents must add up to the required 100 mA.

Data can also be presented in a quasi three dimensional format as seen in figure 10. The output from TEMP3D is compatible with two dimensional thermal analysis programs using finite element techniques that were also generated by the authors. Shown in figure 10 is temperature over the active region. The projection of the contour over the bottom plane gives the position and shape of the cell. The "x" and "y" dimensions are in mils. Isothermal representation of this same data is seen in figure 11. The difference between isotherms corresponds to 2 C.

Influence of Operating Point

It is well known that the high-current, low-voltage operating regime represents a less stressful condition than low-current, high-voltage operation, for constant power. The low-current, high-voltage condition yields higher junction temperatures and greater nonuniformity in current distribution. This increase in stress results from ineffectual emitter ballasting

at low currents. Another reason for this behavior is due to the degradation of beta with high current which makes base resistance ballasting significant. This is borne out by reference to figure 12. For all data points, the total DC dissipation was held to 1.5 W; the current was changed from 35 to 300 mA. Not only is a reduction in the maximum junction temperature observed, but the effective area used increases from 60 to 99% with increasing current. This effect is even more dramatic as the total dissipation increases.

Ambient Conditions

The role of the nonlinearities associated with the thermal conductivity of silicon and current transport can be seen in figure 13. In this case we have plotted the maximum junction temperature versus the bottom temperature of the chip. If the thermal conductivity of silicon had no dependence on temperature there still should not be a one for one increase in junction temperature as denoted by the line "linear model". This is because current injection itself depends strongly (expotentiallly) on temperature.

Emitter Ballasting (Re)

The dilemma in the use of emitter ballasting is that even though it provides for a more rugged device, it acts as a parasitic element electrically, which reduces transistor efficiency and gain. The RF transistor designer would like to minimize these undesirable effects and still guarantee reliable operation. Figure 14 presents the dependence of maximum junction temperature and "% Area Used", ie. current nonuniformity, on total emitter resistance. This is done for the benchmark model with identical ballasting resistors. It is seen that no significant change in transistor behavior occurs until Re drops below .4 ohms. After the total emitter resistance drops below the dynamic resistance of the emitter-base junction Vt/Ic ~ .33 ohms at 110 C the maximum junction temperature begins to rise quickly, and current becomes localized to the hot spot of the device. If ballasting were much further reduced, the benchmark model would experience thermal runaway even for these moderate operating conditions. This is evident from the fact, that for Re = .1 ohms the maximum junction temperature jumps to 136 C and the "% Area Used" drops to 48%. Figures 15 and 16 present the temprature and nodal current distributions for the case Re = .1 ohms. The localization of current and temperature in the center of the cell is readily observed.

Figure 17 shows the normalized finger currents as a function of finger positition with Re as a parameter. It can be seen that with the decrease in emitter ballasting the current tends to crowd in the center of the cell. As seen previously in figure 14 one can observe the striking jump in current localization in going from .2 to .1 ohms.

Contoured Ballasting

In view of the fact that it is desirable to ballast at lower levels from an circuit point of view, TEMP3D gives the Rf transistor designer the tool to change ballasting contours and obtain quantitative information on the effects of contouring on current and temperature distribution. As an example, the benchmark model for Re = .2 ohms was selected. The emitter finger ballast resistors were chosen as seen in figure 18. The emitter resistors were varied linearly in value from 6 to 10 ohms for fingers 1 to 10 respectively. fingers 11 to 25 were assigned resistor values that also varied linearly from 10 to 14 ohms respectively. The resistors belonging to positions 26 through 50 are symmetric about the center of the cell. the total emitter resistance for this contoured case was held to .2 ohms. This level is also shown for the uniform case where all 50 resistors have the value of 10 ohms.

The effect of this contour ballasting is presented in figure 19. The results for the uniform case yeilded a maximum junction temperature of 123 C and "% Area Used" of 70%. By going to this contoured scheme the junction temperature was reduced to 114 C. this is the same result as calculated for the 1.6 uniformly ballasted case. More significant, however, is the fact that the figure of merit for current uniformity increased to 85%.

This could still further be improved upon by refining the contour of the ballast resistors. The example shown represent a simple guess on our part based on the results from the uniform case.

Rf Behavior

It is also well known that the level for adequately ballasting RF transistors for Class C operation is much lower than for Class A. This is reflected in the fact that thermal resistance as measured under self-bias in Class C is lower than under pure DC conditions. What is inferred, is that the power distribution under strictly Rf conditions is more uniform than in Class A. We attribute this improvement in uniformity to degradation of gain with frequency. This degradation of gain is not only due to beta rolloff with frquency but is also a strong function of collector current amplitude. As the current amplitude increases, base widening effects become more pronounced. This phenomenon sharply limits the ability of the RF current to localize. The DC component of this current, which is responsible for heating, follows the Rf current distribution and tends to be more uniform in comparison to DC operation with the same power dissipation. Figure 20 illustrates how this phenomenon is handled in TEMP3D. Both curves correspond to the benchmark model with uniform emitter ballasting of .2 ohms. The difference between 1 GHz and DC operation is dramatic in

temperature (114 C vs 134 C), area used (99% vs 70%), as well as the finger current distribution as shown in figure 20.

Multi-Cell Structures

The ability of TEMP3D to handle multi-celled structures is shown in figure 21. A new transistor configuration based on the benchmark model was investigated. This new device is a four cell array having the same number of emitters and base area as the benchmark model. The spacing between cells was 2 mils in both directions. In all other respects the conditions and model parameters of these two devices were the same. As seen from the short summaries, the improvement in "% Area Used" (97% vs 90%) and maximum junction temperature (96 C vs 114 C) is significant. An interesting observation is that the fingers where maximum temperature and current occur is shifted from the center of each cell. This means that there still is thermal coupling between cells.

Device Miniaturization

The reasons for shrinking geometries of RF transistors are directly related to improving frequency performance. The reduction of cell area results in smaller collector-base capacitance. Tighter emitter structures lead to improved injection performance and reduction of the extrinsic base resistance. All these directly impact the maximum frequency of operation. The limitations here are related to two parameters primarily, chip thickness and power density.

Figure 22 illustrates the effects of scaling down the benchmark model: all horizontal dimensions were scaled down by a factor of two. In the new device all 50 emitters are 1 micron wide, the length of the cell is reduced to 8.5 mils, and the cell width is retained to be 1.2 mils. The results of the computer calculation are presented in figure 22. Both maximum temperature and the "% Area Used" dramatically change for the worse. The "% Area Used" goes from 89% to 64%, while the peak junction temperature jumps to 166 C versus 114 C.

Correlation with Experimental Results

The quantitative reliability of TEMP3D was verified using liquid crystal techniques. Liquid crystals were used because of their excellent spatial resolution (~ 2 micron). For the structures measured agreement with measured data was excellent (within 5 C).

CONCLUSIONS

A sophisticated thermal analysis program for CAD and CAE in the field of high frequency bipolar power transistors was developed. It has been shown to agree with the qualitative phenomenon associated with RF transistor operation, namely, electro-thermal interactions. Temperature, and current density distribution were analyzed and presented as a function of power density,

RF and DC operation, total emitter ballasting, contour emitter ballasting, ambient temperature, and cell splitting. A figure of merit to describe current uniformity across the active area was introduced. The method of solution and modeling of transistor electro-thermal coupling was discussed. The program is easy to use, converges rapidly, and presents data in a concise and convenient format.

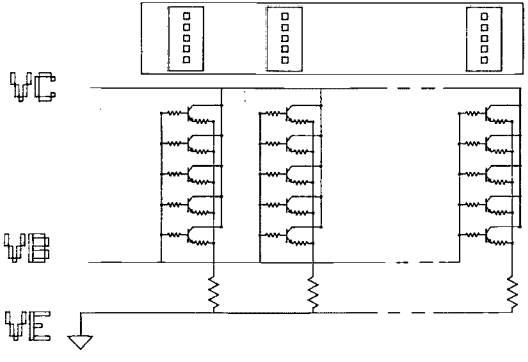


Figure 1. Electrical Schematic of Transistor (Electrical) Model

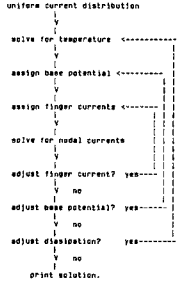


Figure 2. Schematic Representation of Algorithm for the entire solution, both current and temperature.

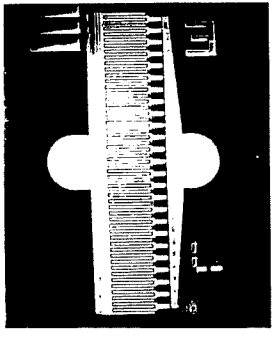


Figure 3. Electromicrograph of typical RF power bipolar transistor - base area 17 x 2.5 mils sq.

CELL NO.	MAXIMUM			MINIMUM			% AREA
	TEMP	FB	CURRENT	TEMP	FB	CURRENT	FB	USED
1 : 1	114.	98	1.335	98.	1	0.811	1	86.915

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 1	98			
		2.710	108.	0.848
		5.487	107	0.856
		8.278	110.	1.033
		11.029	110.	1.066
		13.809	114.	1.324
		16.571	114.	1.335
		19.342	114.	1.324
		22.113	112.	1.088
		24.884	108.	1.033
		27.655	107	0.956
		30.425	107.	0.848

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 6	1			
		2.710	97.	0.811
		5.487	95.	0.805
		8.278	93.	0.802
		11.029	91.	0.853
		13.809	94.	0.870
		16.571	94.	0.878
		19.342	94.	0.878
		22.113	91.	0.853
		24.884	89.	0.824
		27.655	85.	0.806
		30.425	97.	0.811

FB	TEMPERATURE			CURRENT			FOUR	Ic(max)	Re(sense)
1	97.	94.	97.	0.811	0.870	0.811	0.844	1.8878	80.0
2	91.	89.	93.	0.811	1.015	0.811	0.861	1.9818	80.0
3	94.	102.	93.	0.846	1.041	0.838	0.858	1.9458	80.0
4	94.	105.	94.	0.870	1.058	0.851	0.878	1.9401	80.0
5	98.	109.	98.	0.875	1.078	0.905	0.878	1.9565	80.0
6	97.	107.	97.	0.926	1.088	0.878	0.887	1.9733	80.0
7	98.	108.	98.	0.932	1.097	0.932	0.892	1.9847	80.0
8	98.	109.	98.	0.935	1.083	0.935	0.887	1.9954	80.0
9	98.	110.	98.	0.937	1.088	0.937	1.001	2.0025	80.0
10	100.	111.	100.	0.978	1.102	0.938	1.005	2.0082	80.0
11	100.	111.	100.	0.941	1.108	0.941	1.007	2.0102	80.0
12	100.	112.	100.	0.942	1.108	0.942	1.010	2.0122	80.0
13	101.	112.	101.	0.943	1.112	0.943	1.010	2.0144	80.0
14	101.	112.	101.	0.945	1.114	0.945	1.014	2.0175	80.0
15	101.	112.	101.	0.945	1.118	0.945	1.015	2.0189	80.0
16	101.	113.	101.	0.946	1.118	0.946	1.015	2.0205	80.0
17	102.	113.	102.	0.947	1.118	0.947	1.016	2.0217	80.0
18	102.	113.	102.	0.948	1.120	0.948	1.016	2.0232	80.0
19	102.	113.	102.	0.948	1.121	0.948	1.016	2.0237	80.0
20	102.	113.	102.	0.948	1.122	0.948	1.020	2.0280	80.0
21	102.	113.	102.	0.948	1.122	0.948	1.021	2.0310	80.0
22	102.	113.	102.	0.948	1.123	0.948	1.021	2.0314	80.0
23	102.	113.	102.	0.948	1.123	0.948	1.021	2.0324	80.0
24	102.	114.	102.	0.948	1.124	0.948	1.021	2.0326	80.0
25	102.	114.	102.	0.948	1.124	0.948	1.021	2.0330	80.0

Figure 4. Typical TEMP3D output for structure shown above. This benchmark model represents a device with 50 emitters, base area of 17 x 1.2 mils sq., Re = 1.6 ohms, chip thickness of 4.5 mils. Operating conditions are Vce = 15 V, Ic = 100 mA, and Tmin = 60 C.

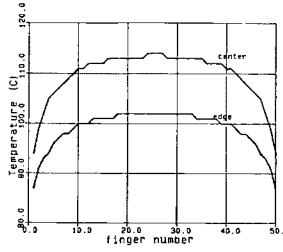


Figure 5.

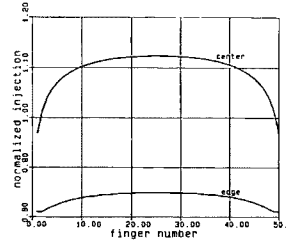


Figure 6.

Temperature and Current distributions along the cell length for the benchmark model under conditions described in Figure 4.

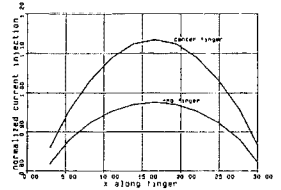


Figure 7.

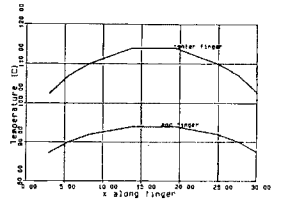


Figure 8.

Figures 7, 8. Temperature and Current distributions along finger length for the benchmark model (Figure 4.)

Figure 9. Finger Current injected at each finger for the benchmark model.

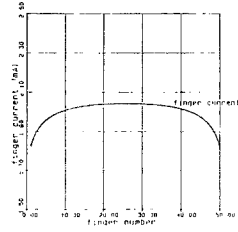


Figure 9.

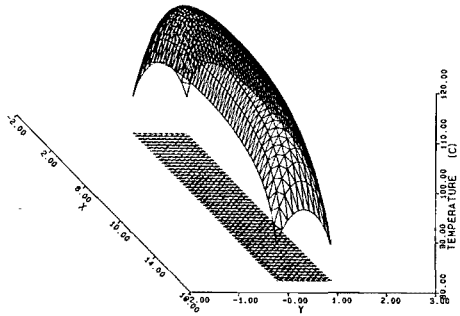


Figure 10. Three Dimensional Representaion of Surface Temperature for the benchmark model (Figure 4.). Tmax = 114 C, Tmin = 87 C.

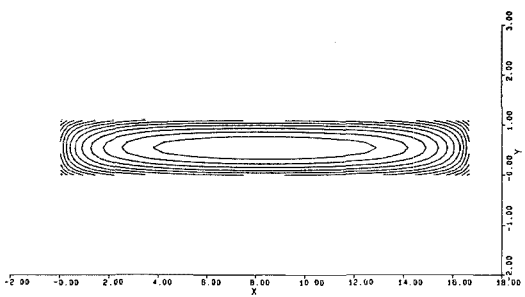


Figure 11. Isothermal Representation of Surface Temperatures shown in Figure 10. Tmax = 114 C, Tmin = 87 C. 2 C/isotherm.

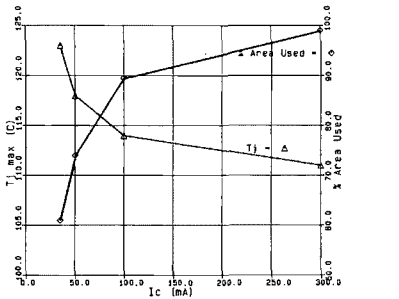


Figure 12. Effects of tradeoff in current vs. voltage for constant power dissipation for the benchmark model (Figure 4.).

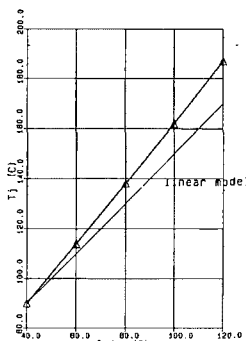


Figure 13. Effect of ambient temperature on maximum junction temperature Tj for the benchmark model (Figure 4.).

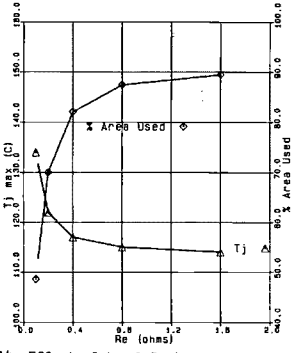


Figure 14. Effect of total Re in the case of uniform ballasting on Tj, maximum junction temperature (see Figure 4. benchmark model).

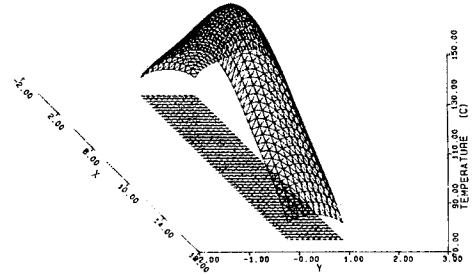


Figure 15.

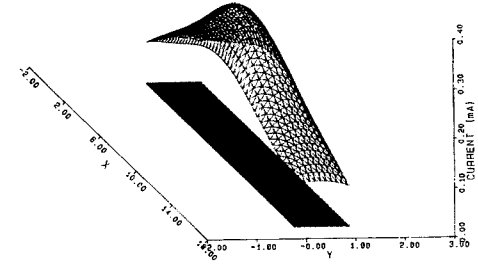


Figure 16.

Temperature and Current Distributions for the benchmark under standard conditions with uniform ballasting and total Re = .1 ohms.

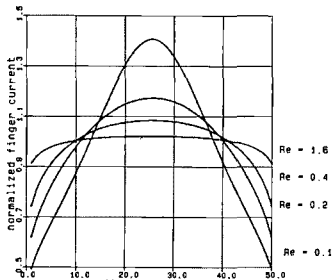


Figure 17. Effect of total Re in the case of uniform ballasting on finger current (ie., current injection along cell length) for the benchmark model.

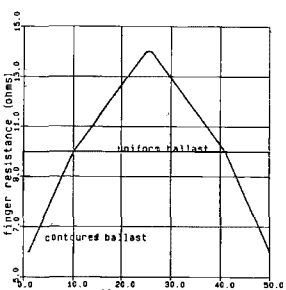


Figure 18. Finger ballast as a function of position for the cases of uniform and contoured ballasting.

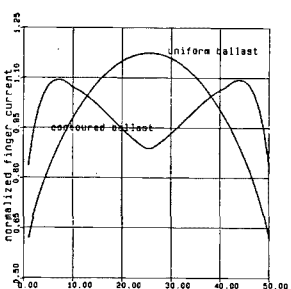


Figure 19. Resulting current injection along cell length for the cases of uniform and contoured ballasting (Figure 18).

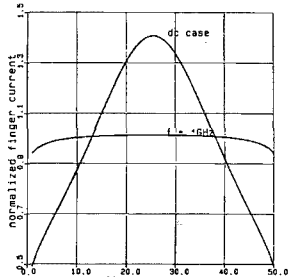
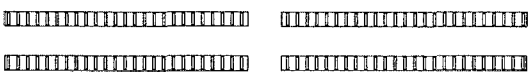


Figure 20. Comparison of Class C and Class A operation for the case Re = 0.1 ohms.

CELL NO.	MAXIMUM				MINIMUM				% AREA
	TEMP.	F#	CURRENT	F#	TEMP.	F#	CURRENT	F#	USED
1 : 1	98.	15	1.081	15	81.	1	0.878	2	97.220
1 : 2	98.	15	1.081	15	81.	1	0.878	1	97.220
2 : 1	98.	11	1.081	11	81.	25	0.878	25	97.220
2 : 2	98.	11	1.081	11	81.	25	0.878	25	97.220



CELL NO.	MAXIMUM				MINIMUM				% AREA
	TEMP.	F#	CURRENT	F#	TEMP.	F#	CURRENT	F#	USED
1 : 1	114.	28	1.135	28	87.	50	0.831	50	89.513

Figure 21. Illustration of cell splitting and multi-cell handling by TEMPJ Total base area, and emitter areas are conserved. Cell spacing in top model is 1.0 mils edge to edge.

CELL NO.	MAXIMUM				MINIMUM				% AREA
	TEMP	F#	CURRENT	F#	TEMP	F#	CURRENT	F#	USED
1 : 1	108.	28	1.364	28	101.	50	0.865	50	83.758

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 1	28			
		2.718	132.	0.891
		5.487	143.	0.986
		8.256	152.	1.062
		11.029	158.	1.218
		13.800	164.	1.326
		16.571	166.	1.364
		19.342	164.	1.326
		22.113	159.	1.218
		24.884	152.	1.062
		27.655	143.	0.986
		30.425	132.	0.891

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 1	50			
		2.718	101.	0.878
		5.487	106.	0.781
		8.256	106.	0.826
		11.029	112.	0.876
		13.800	113.	0.906
		16.571	114.	0.917
		19.342	113.	0.906
		22.113	112.	0.876
		24.884	109.	0.826
		27.655	106.	0.781
		30.425	101.	0.878

CELL NO.	MAXIMUM				MINIMUM				% AREA
	TEMP	F#	CURRENT	F#	TEMP	F#	CURRENT	F#	USED
1 : 1	114.	28	1.135	28	87.	50	0.811	50	89.513

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 1	28			
		2.718	102.	0.848
		5.487	107.	0.858
		8.256	110.	1.033
		11.029	112.	1.080
		13.800	114.	1.124
		16.571	114.	1.135
		19.342	114.	1.124
		22.113	112.	1.080
		24.884	110.	1.033
		27.655	107.	0.858
		30.425	102.	0.848

CELL NO.	FINGER NO.	Y	TEMP	CURRENT
1 : 1	50			
		2.718	87.	0.811
		5.487	90.	0.889
		8.256	92.	0.924
		11.029	93.	0.953
		13.800	94.	0.970
		16.571	94.	0.976
		19.342	94.	0.970
		22.113	93.	0.953
		24.884	92.	0.924
		27.655	90.	0.889
		30.425	87.	0.811

Figure 22. Illustration of device scaling. All horizontal dimensions of cell on the left have been reduced by a factor of 2. Benchmark model is seen on the right.

Microwave Integrated Receiver for the Morelos Mexican Satellite System

by
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ABSTRACT

This article describes the characteristics and design procedure of a microwave integrated front-end for the Morelos Mexican Satellite System. The receiver works at Ku band and provides a 0.9-1.4 GHz signal to the modem. The main application of this receiver is educational television reception. However, the system can be used for thin route telephone and data transmission applications.

INTRODUCTION

The Morelos Satellite is a hybrid system for both C and Ku Band[1]. It is expected to be fully operational at the beginning of 1986. The satellite system is composed of two satellites, Morelos I located at 113.5°, and Morelos II located at 116.5° West. The two satellites are versions of the HS376, the most purchased commercial communications satellite in the world. Morelos is the first Hughes Aircraft satellite to use a planar array for reception of the four Ku band channels, each one with 108 MHz bandwidth, covering the country with a minimum effective isotropic radiated power (KuEIRP) of 44 dBw. The transmit and receive beams for C band and the transmit beams in Ku band are provided by a 6-foot wide shared aperture grid antenna with two polarization selective surfaces. The front surface detects horizontally polarized signals and the rear detects vertically polarized signals. Two separate microwave feeds are used for both polarizations. The C band structure of the satellite consists of 12 vertically polarized narrowband channels with 36 MHz bandwidth each and six horizontally polarized with 72 MHz bandwidth. The front-end described in this article is designed for the Ku frequency band of the Morelos System. Figures 1 and 2 show the physical structure of Morelos and its EIRP "footprint" respectively.

II. LINK CALCULATIONS

In order to define the technical specs of the Ku band front-end, a computer program that provides the main parameters of the link was developed. This program is particularly adapted to the characteristics of the Morelos Satellite system and gives important information about the receiver's performance under several input conditions. Fig. 3 shows a flow-diagram of the computer program. The output data are given graphically and can be adjusted for different input data according to the designer needs.

Figures 4 and 5 are provided by the program and show the behabior of carrier to noise ratio (C/N) with respect to two basic parameters, the low noise amplifier noise figure F_{LNA} and the low noise amplifier gain G_{LNA} for different antenna gains. Fig. 6 shows the relation between C/N and S/N for a typical TVRO receiver (Microdyne 1100 TVR)[2].

It can be seen from fig.4 that for F_{LNA} = 3 dB, C/N is around 19 dB. According to *Fig.6 this value fo C/N would give a S/N of more than 50 dB* which would imply a good TV reception; however, if the sensitivity of the system given by Equation 1 is taken into consideration for the case of the Morelos System with a KuEIRP of 44 dB, it is observed that for F_{LNA} = 3 dB there is a minimum acceptable operational margin (OM) of around 3 dB. The operational margin is given by Equation 2 as:

$$s(dBm) = (\text{Noise Floor} = -174\ dBm) + F_{LNA} + 10\ \log_{10} BW \qquad 1)$$

$$OM(dBm) = I_{LNA} - S, \qquad 2)$$

where BW is the satellite channel bandwidth, which is 500 MHz for Morelos (11.7 - 12.2 GHz), and I_{LNA} is the signal level at the LNA's input and is given as:

$$I_{LNA}(dBm) = EIRP + \text{Free Space Loss} + G_{ANT}, \qquad 3)$$

where G_{ANT} *is the earth station* antenna gain.

For F_{LNA} = 3 dBm and BW = 500 MHz, we obtain S = -84.02 dBm and for EIRP = 44 dBW free space loss of -205.18 dB and GANT = 50 dB; I_{LNA} = -81.18 dBm. This will result in an OM according to Equation 2 of around 3 dB.

Taking into account the results of the above described example it can be observed that if a F_{LNA} = 6 dB is chosen OM would be around zero; e.g., the input signal is immersed in noise. This situation is not desirable at all. In order to increase the operational margin OM, I_{LNA} should increase. It can be seen from Eq. 3 that EIRP and G_{ANT} should in turn be increased. However, increasing EIRP is not feasible because it is fixed from the satellite specs, and G_{ANT} is difficult to increase beyond 50 dB, at least for Ku band commercial antennas. The most practical possibility to improve OM is to reduce F_{LNA} to the minimum and try to push G_{ANT} beyond 50 dB with the minimum possible losses in the antenna feed system.

Fig. 5 shows the direct influence of G_{LNA} on the C/N value. Available Ku band commercial antennas with 40-50 dB gain are considered for this figure. It can be observed that for F_{LNA} = 2 dB the LNA's gain could be around 35 dB to obtain adequate values of C/N. This implies that increasing the gain beyond 35 dB at the 11.7-12.2 GHz frequency band

does not provide any further improvement.

From the link analysis we can define the design requisites of the receiver for Morelos in the Ku band: Maximum $F_{LNA} < 3$ dB; desirable $G_{ANT} \geq 50$ dB and $G_{LNA} \geq 30$ dB.

SYSTEM INTEGRATION

Fig. 7 shows the basic structure of the Ku band receiver for the Morelos Satellite system. We are using an integration approach that combines monolithic microwave integrated circuit (MMIC) subsystems (basically LNA blocks) manufactured by NEC with other hybrid microwave circuits assembled in our laboratory. The technical specs for the LNA-MMIC are[3]: Bandwidth - 11.7-12.2 GHz, F_{LNA} = (MC5806A) - 2.2 dB F_{LNA} (MC5806B) - 3.0 dB G_{LNA} = 17 dB. Considering these specs and the design requisites defined before, it can be seen that if two LNA modules are connected in cascade we will achieve the design objectives: $G_{LNA} \geq 30$ dB and $F_{LNA} \leq 3$ dB. Careful packaging and assembling of the MMIC modules is an important factor to obtain a successful design. Improper assemblies would result in a loss of gain per module of around 2 or 3 dB and instabilities in noise figure.

The picture shown in figure 8 corresponds to the subassembly of the Ku band integrated receiver. Local oscillator, mixer and intermediate frequency amplifier are respectively MC5808, MC5807 and MC5805 NEC hybrid modules. The band pass filter and other interstage modules are designed in our laboratory.

CONCLUSIONS

The Ku band front-end described in this article will be tested directly on the Morelos System when the two satellites are fully operational around the first trimester of 1986. Final testing of the modules will provide information about the conveniences of using MMIC instead of conventional hybrid modules from the economic and efficiency points of view. The program developed for the link analysis of Morelos has been very useful in defining the receiver's specs and it is expected to improve it to cover more subtle aspects of the parameters of the link.

ACKNOWLEDGEMENTS. We thank Ricardo Chavez, Benjamin Ramirez and Isabel Alcaraz for their valuable participation in the final manuscript.

REFERENCES

1) Comparative Analysis of C and Ku Frequencies for the Mexican Satellite Communications Domestic System (In spanish) Hughes Document Ref 43 (82) 001132/F2017, March, 1982, Hughes Aircraft Co.

2) Microdyne 110 TVR Receiver Data Sheet, Microdyne Corp., Ocala Florida 1983.

3) MMIC data sheet, MC 5806A, MC 5806B, Nippon Electric Corp. 1984.

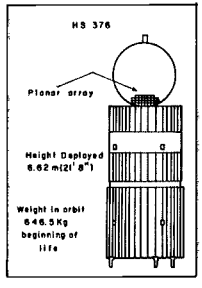


FIG.1) BASIC STRUCTURE OF MORELOS I, II

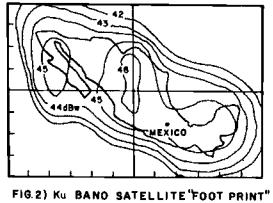


FIG.2) Ku BAND SATELLITE "FOOT PRINT"

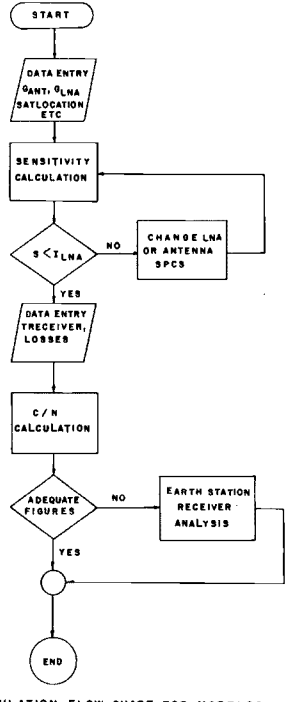


FIG.3) LINK CALCULATION FLOW CHART FOR MORELOS

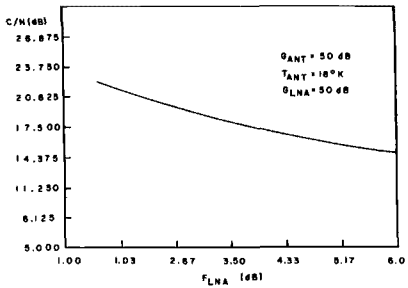


FIG. 4) C/N VS. F_{LNA} FOR A Ku BAND RECEIVER

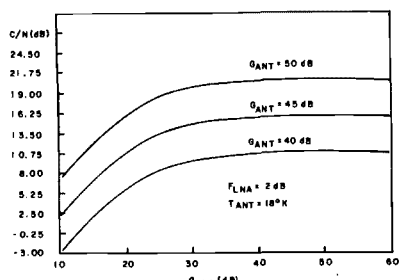


FIG. 5) C/N V.S. G_{LNA} FOR A Ku BAND RECEIVER

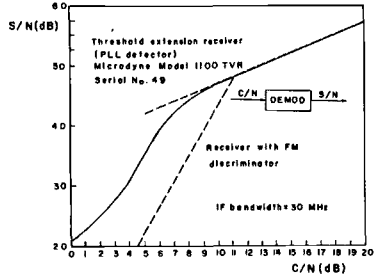


FIG. 8) OUTPUT S/N AS A FUNCTION OF FM DETECTOR INPUT C/N

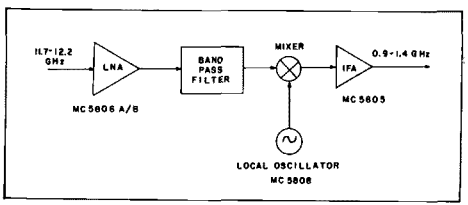


FIG.7) BASIC STRUCTURE OF THE Ku BAND RECEIVER

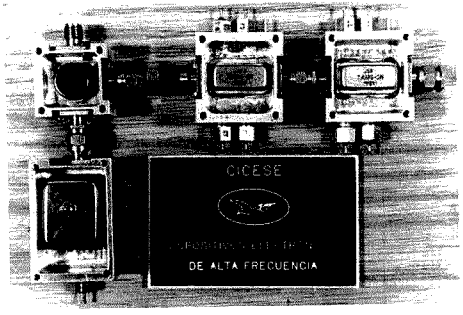


FIG.8) SINGLE CONVERSION MODULE FOR THE Ku BAND RECEIVER

HIGH EFFICIENCY POWER AMPLIFICATION WITH OPTIMALLY LOADED HARMONIC WAVESHAPING

by
William McCalpin

High efficiency power amplification is achievable by utilizing harmonic waveshaping techniques to control the collector voltage and current waveforms. By appropriately manipulating these waveforms, the collector-voltage current product is minimized; thus, the power dissipated in the device is reduced. The goal of the waveshaping is to approximate a switching type device which has at least one abrupt step in either voltage or current in order to reduce the time in which both are present. This can be accomplished by pulsing the input to produce a square current waveform and employing the device as a saturated current source with a load network that will create a first approximation of a half-sinusoid voltage.

To elucidate the realization process of the RF amplifier made, five main points are presented: the need for Class F operation, a description of Class F amplification, a Fourier analysis of the waveforms required, the practical realization of the amplifier and the data and analysis from operation and testing.

Power amplification is separated into several modes of operation having various maximum theoretical efficiencies and output powers. In practical terms, operation in all of these classes is in suboptimum conditions due to losses, bandwidth and drive level requirements, and saturation limits of the active device. For our application, an amplifier output level of 50 watts at a single frequency of 425 MHz is used, so it is expected that the practical data should come close to the theoretical limits of the class of operation.

For this particular frequency and output level, Class F was chosen because high efficiency was required and there exists inherent problems with high efficiency operation in other classes at this carrier frequency. Class A linear amplification was avoided because an optimum efficiency of only 50% at maximum power output is possible. This limit exists because the device and the load receive the same amount of power from the supply. The most common form of Class B amplification is a transformer coupled push-pull configuration with a maximum theoretical efficiency of 78.5%. Class C has a maximum efficiency between 85 and 90% depending on the angle of conduction; however, at UHF frequencies it has relatively low efficiency. Class D utilizes the notion of a switch in order to reduce device dissipated power which brings the theoretical efficiency to 100%. However, in order to reasonably simulate the switching action, an active device of 25 to 30 times the fundamental frequency is required. The fundamental frequency of our amplifier was set at 425 MHz which puts the f_T too high for a UHF device to reasonably simulate a switch.

Class F models the device as a saturated current source and utilizes a load network that resonates at harmonic frequencies as well as the fundamental. Class F efficiency is limited in that fully switched waveforms are not possible because the power dissipating in each switching transition cannot be reduced simutaneously. [1] In addition, the waveshaping in Class F requires an

f_T of only 10 times the fundamental frequency which is more within the limitations of an active UHF device. "Second Harmonic Peaking" is a variation that uses a second harmonic resonator to include the second harmonic component in the collector voltage making a first approximation of a half-sinusoid. The device produces a square collector from a pulsed input. The collector waveforms and a circuit containing the second harmonic resonator are given in Figure 1 below.

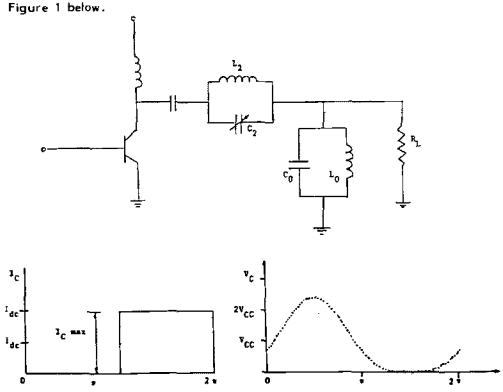


Figure 1

Circuit and waveforms from Fourier Analysis, See Raab, F.H. "Analysis of Second-Harmonic-Peaking Power Amplifier", May 1982, pp 2-3.

The second harmonic resonator in Figure 1 (represented by L_2/C_2) presents a load to the second harmonic which is included in the collector voltage waveform. The fundamental resonator shunted to ground acts as a low-pass filter to the second harmonic removing it from the output, thus the load only dissipates power at the fundamental frequency.

A Fourier analysis of the collector waveforms, given by F.H. Raab[2], clarifies the increase in efficiency due to the harmonic loading. With the second harmonic resonator, the collector voltage waveform is represented by

$$v_C(\theta) = V_{CC} + V_{OM}\sin\theta + V_{2M}\cos 2\theta.$$

Because the second harmonic sine wave is centered in the middle of the voltage waveform it cannot flatten the collector voltage and is therefore not included. Maximum flatness is achieved when the second derivative is zero which implies that the switching transition has become abrupt. The first two derivatives of the collector voltage are given below.

$$\partial v_C(\theta)/\partial\theta = V_{OM}\cos\theta - 2V_{2M}\sin 2\theta$$

$$\partial^2 v_C(\theta)/\partial\theta^2 = -V_{OM}\sin\theta - 4V_{2M}\cos 2\theta$$

By setting the second derivative equal to zero and theta equal to three pi over two it is observed that

$$0 = -(-V_{OM}) - 4V_{2M}(-1)$$

or

$$V_{2M} = -V_{OM}/4.$$

If the minimum collector voltage is to be zero, and if V_{2M} is negative one fourth V_{OM} when theta is three pi over two, then

$$0 = V_{C,min} = V_{CC} - V_{OM} - V_{2M}$$

or

$$V_{OM} = (4/3)\, V_{CC},$$

and

$$V_{C,max} = V_{CC} + V_{OM} - V_{2M}$$

or

$$V_{C,max} = (8/3)\, V_{CC}.$$

The power output is therefore

$$P_O = V^2_{OM} / 2R = (8/9)\, V_{CC}^2 / R$$

Since the device produces a square collector current, the values of the DC input current and the peak collector current can be evaluated from the collector voltage.

$$I_{OM} = V_{OM} / R = (4/3)\, V_{CC} / R$$

Because the collector current is a squarewave

$$I_{OM} = (2/PI)\, I_{C,max}$$

or

$$I_{C,max} = (2\ PI / 3)\, V_{CC} / R,$$

and if the DC input is half the maximum collector current, then

$$I_{DC} = (\ PI / 3\ )\, V_{CC} / R.$$

The input power is the product of the supply voltage and current and is therefore

$$P_i = V_{CC} * I_{DC} = (\ PI / 3\ )\, V_{CC}^2 / R.$$

With this information the performance of the power amplifier can now be determined. The collector efficiency of the P.A. is the ratio of the output power to the supply power input or

$$\text{eff.} = P_O / P_i = (\ (8/9)\, V_{CC}^2 / R) / (PI / 3)\, V_{CC}^2 / R$$
$$= (.849) * 100\% = 84.9\%$$

The normalized power output capability is defined as the ratio of the power to the product of the peak collector voltage and the peak collector current or

$$P_{max} = P_O / V_{C,\,max} * I_{C,\,max}$$
$$= (8/9) V_{CC}^2 / R) / (\ (8/9) V_{CC} * (2\ PI / 3)\ V_{CC} / R)$$
$$= (\ 1/2\ PI\ ) = 0.159.$$

For comparison the normalized power output for a Class C amplifier operating at 85% efficiency is calculated to be equal to 0.112. Thus, a high theoretical efficiency and normalized power output is attainable by manipulating the second harmonic component in a Class F amplifier configuration.

A pulse amplifier using the theoretical analysis described above was constructed that operated at 425 MHz with a peak power output of 50 watts. The circuit construction used is given below in Figure 2. The transmission lines shown serve two purposes, one is to match the low output impedance of the

device collector to the standard 50 ohm output, and the other is to present the second harmonic loading required to produce the desired waveforms at the device collector for Class F operation.

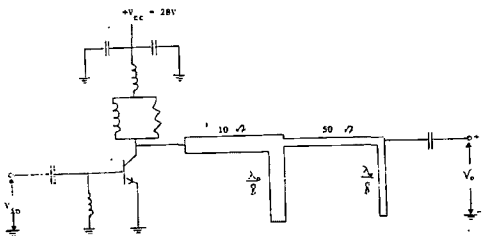


FIGURE 2

The first step in matching the collector impedance of the device used to the circuit output is determinimg the impedance looking back at the device from the transmission lines. A model of the device used in the circuit design is given below.

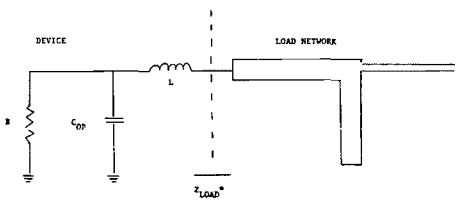


FIGURE 3

Where:

$L = .8$ nH

$C_{OB} = 39$ pF (measured at 1/2 $V_{CC} = 14V$

$R = (V_{CC} - V_{sat})^2 / 2 P_o$, $V_{sat} = 3V$

$= (25)^2 / 2 * 50$ watts $= 6.25$ ohms

$Z_L = 4.45 \angle -.163$

$Z_L = 4.39 - j.721$ at 425 MHz

In order to calculate the circuit elements necessary to match the device collector impedance to 50 ohms and manipulate the second harmonic loading, a computerized circuit optimization program was used. Withe the stubs modeled as shunt capacitors, (at the fundamental frequency) the optimized dimensions for the microstrip lines were calculated. The result values are shown in Figure 4.

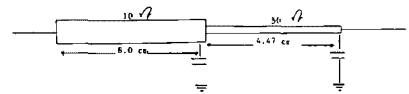


FIGURE 4

The optimized capacitance values were then used in a microstrip stub program which iterates the process of calculating an accurate value of E_{eff} from the dielectric thickness and the E_{rel} of the Teflon fiberglass material. From this, the dimensions of the stubs and the speed of the wave in the line were determined. The two stubs are lambda over eight in length at the fundamental frequency or lambda over four in length at the second harmonic Points A and

B on Figure 5 are open circuited which translate through a lambda over four stub transformation to present a second harmonic short to ground, thus providing the low-pass filter shown in Figure 1. Moving back towards the device collector from the circuit output, the second harmonid shorts at points A' and B' translate through the lambda over four lines to a high impedance which presents a second harmonic load at the collector.

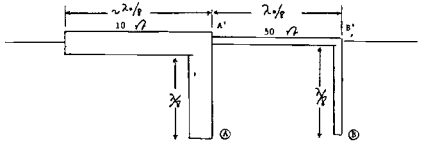


FIGURE 5

The remainder of the circuit elements in Figure 2 are positioned to provide DC supply to the device collector while maintaining stability in the circuit. The series capacitors on the input and output are 510pf chip capacitors for DC blocks. The inductor-resistor branches are ferrite core wire would inductors with a 15 ohm resistor to provide a supply path while presenting an open circuit to the RF power. The left-hand capacitor on the supply branch is a 1500 MF charge storage capacitor to preserve the squareness of the current pulse at the collector by preventing pulse slump and poor rise time. The right-hand capacitor is a .1 MF parallel plate bypass capacitor to bring RF ground to that node to prevent any RF power from entering the power supply or meters.

Along with the circuit in Figure 2, a circuit with exactly lambda over eight transmission lines, and a circuit with the optimized line lengths but using tuning capacitors instead of the stubs were constructed and tested for comparison. The three configurations are shown in Figure 6.

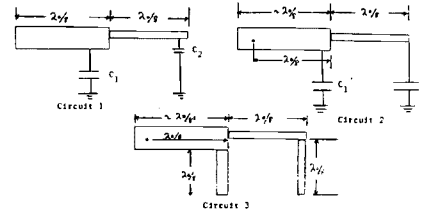


FIGURE 6

The data below shows the device collector efficiency, overall efficiency, and overall gain of the three amplifier configurations, where:

$$\text{Collector efficiency} = P_O / V_{CC} * I_{D.C.}$$

$$\text{Overall efficiency} = P_O - P_i / V_{CC} * I_{D.C.}$$

$$\text{Overall gain} = 10 \log_{10} P_O / P_i$$

Circuit 1: lambda over eight transmission lines with tuning capacitors of C_1 = 33.4 pF and C_2 = 18.1 pF.

P_{in} = 15 W , P_{out} = 73 W, V_{CC} = 28 V , I_C = 4.3 A

Collector eff. = 60.6%

Overall eff. = 48.2%

Overall gain = 6.9 dB

Circuit 2: optimally matched transmission lines with tuning capacitors of C_1 = 24.0 pF and C_2 = 8.45 pF.

P_{in} = 8 W, P_{out} = 54 W , V_{CC} = 28 V , I_C = 2.7 A

Collector eff. = 71.4%

Overall eff. = 60.8%

Overall gain = 8.3 dB

Circuits 3: optimally matched transmission lines with lambda over eight stubs.

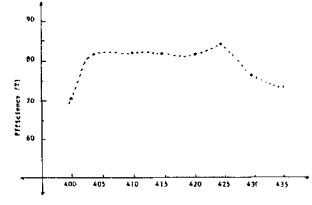
P_{in} = 7.7 W , P_{out} = 51 W , V_{CC} = 27.9 V , I_C = 2.2 A

Collector eff. = 83.1%

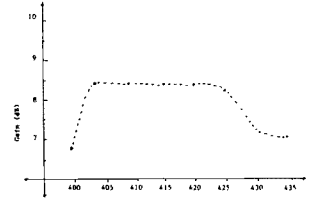
Overall eff. = 70.5%

Overall gain = 8.2 dB

The above data was optimized and measured after careful tuning. The increase in efficiency is believed to be primarily due to an improvement in impedance matching along with a drop in the supply current necessary to maintain the specified output level. As shown in Figure 7 below, the highest efficiency was attained in a tight notch at 425 MHz. This notch is caused by a small dip in the supply current, however, a relatively high level of efficiency was maintained over a 20 MHz bandwidth. Because a trade-off exists between gain and efficiency due to the fact that the collector waveforms can be overdriven to produce sharper edges, the data in Figures 7 and 8 was tuned for optimal efficiency and gain simultaneously to more accurately portray the frequency response shown below[3]



Frequency (MHz)
Figure 7



Frequency (MHz)
Figure 8

A spectrum analyzer was used to probe along the series transmission lines to determine the harmonic component at different locations. Figures 9 and 10 show the harmonic response for the optimally matched transmission lines with and without the stubs respectively. (The stubs replaced by tuning capacitors).

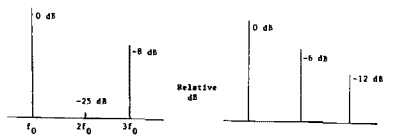


FIGURE 9
Measured at Point C' in Circuits of Figure 6

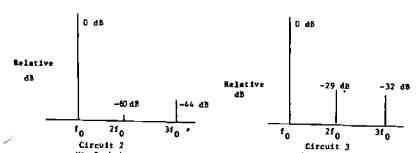


FIGURE 10
Measured at Amplifier Output

As shown in the data above, there is more second harmonic component in the circuit with the stubs acting as a second harmonic load, yet the second harmonic component is removed from both when probed at the output. Since the efficiency increased from Circuit 2 to Circuit 3, it can be concluded that this rise in efficiency is due to the waveshaping caused by the harmonic load. It is also possible that a better impedance match resulted from using the stubs; however, the junctions of the stubs with the lines can only at best be approximated in a practical sense and is therefore difficult to determine for certain.

Thus, it has been demonstrated that high efficiency and power output are available in practical terms at a UHF radio frequency of 425 MHz. At this carrier frequency, a collector efficiency of 83.1% with a gain of 8.3 dB was achieved using the second harmonic waveshaping techniques and impedance matching described above.

FOOTNOTES

[1]Frederick H. Raab, Ph.D., "Fundamental Limitations in Class-E and Class-F Power Amplifiers, " Green Mountain Radio Research Co., Copyright 1982.

[2]Complete Fourier Analysis by Frederick H. Raab, Ph. D., "Analysis of Second-Harmonic-Peaking Power Amplifier", Green Mountain Radio Research Co., Copyright, 1982.

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MODULATION TECHNIQUES FOR BIOTELEMETRY

by
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Biotelemetry can be defined as a means of wireless transmission of physiological data. Transmission can be via radio, infrared or ultrasound. The frequencies of interest range from DC for temperature telemetry to several thousand Hertz for muscle voltage monitoring.

In aerospace biotelemetry, the telemeter is carried in the aircraft or spacecraft and need not be extremely lightweight. This is not the case, however, when ambulatory people or animals must be monitored. Ambulatory biotelemetry has necessitated the development of a number of interesting battery saving techniques.

Probably the first ambulatory biotelemeter was developed by Norman Holter. It was about the size of a five gallon water can and had to be carried on a pack board. This was followed in 1952 by a compact telemeter using Raytheon subminiature tubes (1).

The advent of the transistor led to renewed interest in ambulatory biotelemetry in the late fifties and early sixties (2-6). These early telemeters usually employed self excited oscillators operating in the 100 MHz FM broadcast band (Fig 1). This circuit utilized the patient as a transmitting antenna.

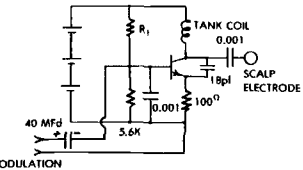

Fig. 1. A 100 MHz self excited oscillator. The transistor is a 2N835. Modulation sensitivity is adjusted by selecting the biasing resistor (R1). The batteries are miniature 1.35 volt mercury cells.

Although transistor manufacturers don't like to mention the fact, the junctions in bipolar transistors are actually voltage controlled tuning diodes. Telemeter designers soon learned to utilize this property as a method of frequency modulation. A base to emitter signal of only about a millivolt was found to produce adequate deviation at 100 MHz. This meant that the amplifier for telemetering a 50 microvolt EEG (brain voltage) signal need have a gain of only 20.

A major problem with these direct FM transmitters was motion artifact due to detuning of the transmitter when the person being telemetered moved his hand near the tank coil. The problem was solved by using an FM-FM system with a frequency modulated audio subcarrier. This technique is still used in most EKG (heart rate) telemeters.

Hand capacitance detuning is a problem only when low frequency signals such as heart voltage or brain voltages are to be telemetered. In the case of higher frequency signals such as muscle voltage, the movement artifact can be removed by high pass filtering. We have used this technique in a simple multiplex telemeter for muscle voltage and muscle tension (7). Direct FM was used for the muscle voltage and a high frequency subcarrier was used to transmit data from the muscle tension strain gage.

Much of the early interest in biotelemetry was for EEG (brain voltage) studies. A typical application was the location of a seizure focus by implanting multiple electrodes within the patient's brain. A continuous multichannel recording was made day and night until the patient had a seizure. The focus was then located by observing which electrodes detected the strongest signal. The epilepsy could then be treated by destroying a small portion of the brain at the seizure focus. This was usually done by heating the brain with a radio frequency probe. Cases of this type are now usually treated with drugs rather than surgery.

In the beginning, multiple channel recording was done with a separate transmitter for each channel. This was soon found to be impractical. The IRIG format of multiple FM subcarriers was then used to some extent (Fig. 2). However, it had a fairly heavy battery drain because a separate subcarrier oscillator was required for each channel. Continuous operation of the transmitter and all subcarrier oscillators was required.

It soon became evident that the best way to conserve

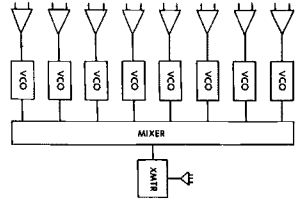

Fig. 2. The IRIG format of multiple subcarriers was used in some early telemeters. Its major disadvantage was excessive battery drain.

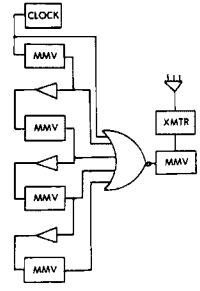

Fig. 3. Pulse position modulation can be generated by a train of pulse width modulated one-shots. This circuit uses SN5188 one-shots. They are modulated by SN524A amplifiers.

battery power was to pulse the carrier on and off. As early as 1961 Kamp and Storm Van Leeuwen (8) used a combination of pulse width modulation and pulse repetition rate modulation in a two channel system. Although a third channel could have been added

by employing pulse amplitude modulation they recognized that this would have been undesirable because of amplitude variations due to signal fading.

A typical hard wired electroencephalograph machine has eight or more channels. Researchers have always wanted to telemeter that number of signals with low battery drain. In order to do this, various pulse coding schemes have been tried. The simplest and most commonly used is pulse position modulation. In this system, the spacing between any adjacent pair of pulses represents the height of an amplitude sample for a particular channel. The data samples for the various channels are transmitted sequentially. At the end of the pulse train there is either a synchronizing pulse or a synchronizing space. A new pulse train representing the next set of amplitude samples is then transmitted.

One of the earliest pulse position modulation telemeters used a chain of pulse width modulated one shots separated by buffers (9) (Fig. 3). The buffers introduced a short delay between adjacent one-shot pulses so that a pulse train was generated when the one-shot outputs were combined in a NOR gate. This pulse train triggered a one microsecond one-shot which in turn keyed the transmitter. Each pulse train was initiated by a clock pulse. There was a synchronizing space at the end of each pulse train.

The received pulses were fed serially into a shift register with parallel outputs for the four data channels. At the start of each received pulse train a reset one-shot was triggered. Its time constant was chosen so that it would time out during the sychronizing space at which time it reset the shift register. Other investigators (10) have used a synchronizing pulse rather than a synchronizing space. This, however, required special circuitry to distinguish between the synchronizing pulse and the data pulses.

We subsequently built a six channel telemeter using the same basic multiplexing one-shot chain (11). This technique worked well but did not make the best use of available battery power.

In order to prolong battery life, we decided to eliminate the one-shots and substitute a ramp generator and a voltage comparator. These circuits were common to all of the nine data channels (12). The data channels were sequentially connected to the comparator by CD4016 CMOS switches (S1-S9) (Fig. 4).

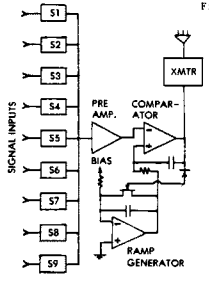

Fig. 4. A simplified block diagram of a nine channel pulse position modulation telemeter. The signal input switches are CD4016's. A MMT3823 J FET is used to dump the capacitor in the ramp generator after each data sample. Pulse spacing is determined by the reference level set on the comparator by the input signal sample.

Actually eighteen switches were used because each input was push

pull. Sequencing of the switches was done by a CD4017 shift register. The selected signal channel was amplified by the common pre-amplifier and used to establish a reference level on the voltage comparator. If the signal level was high, the reference level was high and it took the ramp generator longer to run up to this reference level. When the reference level was reached, the comparator dumped the ramp generator integrating capacitor via a J FET. It also pulsed the transmitter on and shifted the shift register to enable the next input channel. After all nine channels had been sampled there was a synchronizing space. A clock then reset the shift register.

This circuit eliminated the need for separate pre-amplifiers and separate pulse width modulators for each channel. The elimination of separate preamplifiers was due to the low noise characteristics of CMOS switches. This property of CMOS is not well known. Let us suppose that we are switching with a single MOS FET other than CMOS. The gate must be pulsed high to close the switch. Since the line we are switching is high impedance (200K ohms) a portion of the control pulse will be coupled via the gate to channel capacitance into the signal line. Now, let us assume that we are using a CMOS switch. This consists of a P channel MOS FET in parallel with an N channel MOS FET. Since these two MOS FETS require opposite polarity control pulses the portions of the control pulses that are capacitively coupled into the signal line effectively cancel. This circuit worked well for recording from depth electrodes implanted within the brain since the brain signal level was a couple of hundred microvolts peak to peak. For scalp electrode recording an individual preamplifier for each channel was required.

The NASA people have built an eight channel 0.1 percent accuracy pulse code modulation telemeter (13). The data signals were first converted into pulse width modulation by a ramp generator. These pulses gated a 10 MHz oscillator. The 10 MHz pulses within these gated pulse trains were counted by a 10 stage counter. Output from the counter went to a parallel in, serial out shift register which in turn keyed the transmitter.

All of the foregoing telemetery systems were for AC signals. Drift is a major problem when DC signals such as temperature are telemetered. Fryer (14) has used a free running multivibrator as a subcarrier oscillator. One of the two time constant determining resistances was the temperature sensing thermistor. The other was a reference resistor which established the zero reference level. The telemetered temperature was proportional to the ratio of these two resistances.

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WIDE-BAND HIGH-DYNAMIC-RANGE FRONT-END CIRCUITRY FOR AM RADIO

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ABSTRACT

This paper presents the bipolar integrated input-amplifier and frequency-conversion circuitry of an AM upconversion front end for car-radio receivers. Thanks to the upconversion concept and the excellent performance of the wide-band high-dynamic range front end, tuned preselection filters can be omitted, thereby eliminating the need for adjustments and reducing production costs considerably. Tuning is easily accomplished by varying only the oscillator frequency.

The dynamic range of the front end exceeds 120 dB. Field strengths up to about 20 and 200 mV/m can be handled without noticeable second- and third-order intermodulation, respectively.

INTRODUCTION

Conventional AM receivers for long-wave and medium-wave reception use intermediate frequencies somewhere between 450 and 490 kHz. Such receivers need a preselection filter to reject the image and other spurious channels. This filter has to be tuned along with the local oscillator. Band switches and several adjustments are required to ensure adequate tracking.

Well-aligned receivers with mechanically tuned variable capacitors or coils can provide excellent performance, but are expensive. The use of varactors for tuning as an alternative offers the possibility of digital synthesizer tuning. However, their nonlinearity reduces the useful dynamic range of the preselection filter. Besides, band switches and adjustments are still needed.

This paper presents the front-end circuitry of an upconversion receiver for car-radio with a block diagram as shown in Figure 1. The complete receiver has been integrated in a conventional bipolar process (f_{Tnpn} = 400 MHz). Channel selectivity has been realized by a low-cost 10.7 MHz quartz filter. The upconversion concept evades the need for tuned preselection. A low-pass filter at the mixer input effectively rejects image and local-oscillator-related spurious responses. However, a proper noise match to the whip antenna has to be realized in a wide-band low-distortion amplifier, since a fixed low-pass filter in front of this amplifier would seriously impair noise performance [1]. The gain of this amplifier has to be kept low because very large input signals have to be handled linearly. As a consequence, the noise and intermodulation performance of the frequency-conversion circuits (mixer and local oscillator) are also very important.

The first section of this paper discusses a capacitive-feedback wide-band input amplifier with an optimally biased bipolar input stage. The dynamic range of this amplifier has been extended by means of an automatic gain switch, which is activated when very large field strengths are present somewhere in the spectrum.

The second section deals with the frequency conversion circuits. A double-balanced switching mixer, a negative-resistance "one-pin" LC oscillator and a buffer stage maximize the dynamic range. In order to accurately fix the oscillator output amplitude even with large parameter variations, while maintaining an acceptable noise performance, a novel type of AGC has been employed.

INPUT AMPLIFIER AND AGC SWITCH

amplifier configuration

The low-frequency equivalent circuit of a car-radio whip antenna, including the cable to the receiver input is shown in Figure 2. The open antenna voltage is given by

$$V_a = h_{eff} E_a,$$

where E_a is the electric field strength and h_{eff} is the effective height. For a whip antenna, h_{eff} equals half its physical length l_a

*Also with: Sagantec B.V., Croy 5a, 5653 LC EINDHOVEN
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$$h_{eff} = \tfrac{1}{2} l_a .$$

In conventional receivers, the source capacitance $C_a + C_c$ forms an inherent part of the preselection filter. Its reactive part is thus tuned out, thereby significantly simplifying the realization of good noise and intermodulation performance. It can be shown [1] that a filter that covers the whole band to be received and that includes the source impedance would unacceptably degrade noise performance. Therefore a wide-band amplifier has to be used.

A frequency-independent response to the electric field, and consequently to the open antenna voltage, is obtained in a capacitive-feedback amplifier according to Figure 3. The gain of this amplifier is approximately given by

$$\frac{V_o}{V_a} = -\frac{C_a}{C_f} .$$

Note that the cable capacitance ideally does not influence the gain. The impedance level of the low-pass filter behind the preamplifier is chosen as high as 470 Ω to keep the output current low. Insertion loss has been kept small by using an asymmetrical filter terminated in the high input impedance of the voltage-to-current converter of the mixer.

AMPLIFIER IMPLEMENTATION

Figure 4 shows the circuit diagram of the wide-band input amplifier. The signal path is formed by the NPN transistor Q_A, Q_B and Q_C. The noise of the circuit is determined predominantly by the first two stages. Assuming that the bias current of the second stage is much larger than that of the first stage, the spectra of the equivalent input noise sources of the amplifier can be approximated as

$$S(v_n) = 4kT\{r_{bA} + r_{bB} + r_{eA}/2\}, \; S(i_n) = 2qI_B .$$

Referring to Figure 5, the spectrum of v_{eq} *in series with the* antenna voltage v_a can be written as

$$S(v_{eq}) = \left\{\frac{(C_a + C_c + C_f)^2}{C_a^2}\right\} S(v_n) + \frac{1}{\omega^2 C_a^2} S(i_n).$$

The equivalent noise voltage (v_{eq}) in a 2.5 kHz bandwidth and for $r_{bA} + r_{bB} = 100\ \Omega$ is depicted in Figure 6 for various values of the input-stage bias current. A tradeoff is observed between high- and low-frequency noise performance. An acceptable compromise is obtained at a bias current of 50 μA. The equivalent noise voltage *chan equals 0.8 μV at 1 MHz and 1.5 μV at 150 kHz measured in a* 2.5 kHz bandwidth

In order to achieve a high loop gain, the second-stage load is made very high by means of active bootstrapping ($Q_1 - Q_4$). The loop gain has a dominant pole determined by the impedance level at node B. The impedance is formed by a capacitance with a value of about 10 pF. With a feedback capacitance $C_f = 22$ pF, a gain of about 0.6 and a bandwidth of 60 MHz is obtained. In order to minimize intermodulation due to high-frequency input signals a smaller bandwidth is highly desirable; however, this should not be realized at the expense of a smaller slew rate. The only appropriate technique to reduce the bandwidth without deteriorating, as a result of slew-rate limitations, the intermodulation performance is the use of phantom zeros [2]. A network consisting of two coils and a resistor in series with the amplifier input provides such zeros. It has been designed such that the amplifier noise performance is scarcely degraded and the frequency response is 3 dB down at 7 MHz.

The output stage is biased at a collector current of 6 mA and can deliver a peak-to-peak voltage of 4 V to the low-pass filter. In low-end applications a fixed feedback capacitor of 22 pF can be used. In that case an antenna voltage of about 2 V, corresponding to a field strength of 4 V/m can be handled. The total equivalent noise (including mixer contributions) can then have a value of 1.6 μV (B = 2.5 kHz). The dynamic range exceeds 120 dB. Second- and third-order intermodulation products become noticeable (i.e. are equal to the noise floor) at input-signal levels of 15 and 100 mV, respectively. These measurement results bring the second- and third-order intermodulation-free dynamic range (IMFDR) to 80 and 97 dB, respectively.

Automatic gain switch

In order to further increase the dynamic range of the input amplifier, the gain is switched automatically to a lower value as soon as a certain input level is exceeded. Figure 7 shows the basic implementation, where the position of the switch has been chosen such that it has no detrimental effect on noise and intermodulation performance. An external JFET is used as a switch. It is driven by a logic signal obtained by appropriate detection and comparison with a reference level of the amplifier output signal. The comparator hysteresis is chosen 3 dB more than the required gain variation so as to obtain a safe margin, where the gain remains low before the switch is deactivated, thereby avoiding bouncing.

In order to detect the signal level sufficiently accurately, a full-wave rectifier is employed. Comparison with the reference level is performed by two cascaded comparators, the first of which has the required hysteresis. The second comparator is added to avoid a possible source of instability in the switch operation. With C_{f1} = 10 pF and C_{f2} = 30 pF, field strengths of 2 V/m and 8 V/m, respectively, can be handled linearly. The noise floor in a 1.5 kHz bandwidth lies at 1 and 2 µV at 1 MHz, respectively. Second- and third-order IMFDR are at 77 and 90 dB when the switch is deactivated and at 86 and 97 dB when it is activated.

MIXER, BUFFER AND LOCAL OSCILLATOR

Since the preamplifier has to handle large signals at a restricted supply voltage (V_{Bmin} = 7.5 V), the gain is limited to a rather low value. The same holds for the conversion gain of the mixer. The large dynamic range desired and the low gain values involved make the noise and distortion originating from the frequency conversion action more important than in conventional receivers. When infinite betas and a zero switching time are assumed, the current transfer i_o/i_{in} of a double-balanced mixer (Figure 8) does not contribute to noise and distortion. In the case of finite betas, the distortion is generated by current-induced beta variations and the noise is determined by the base-current shot noise, exclusively. Finite switching times introduce additional mixer distortion, since the signal current is transferred in a nonlinear way from input to output during the switch transitions. Finite switching times also lead to other noise contributions besides the base-current shot noise.

Without a doubt, the best mixer performance is obtained when it is driven by a high-slope local-oscillator signal. Ideally, the "finite-slope" noise contributed by the conversion process is then completely determined by the local-oscillator noise. In the frequency-conversion circuitry described here, this situation has been accomplished to a reasonable extent. The mixer switching time is less than 5 ns.

In order to obtain adequate noise performance in the local oscillator an LC oscillator is preferred over a relaxation oscillator. Pulling effects are avoided by employing a limiting differential-pair stage that drives the mixer. Though this limiting action may increase the white noise floor of the local-oscillator signal, the carrier-to-noise ratio of the output signal is still sufficiently high so as not to degrade the receiver noise performance significantly.

The amplitude of the oscillator sine-wave should be fixed well enough to guarantee that the differential-pair buffer stage acts as a current switch. Some form of automatic level control in the oscillator is required to make the amplitude virtually independent of impedance variations in the resonance circuit.

A basic method for the realization of a suitable negative-resistance "one-pin" oscillator is shown in Figure 9. This circuit, however, does not include the proper means for amplitude stabilization. It is useful for appreciating the stabilization technique used in the oscillator to be presented here to distinguish three different modes of operation.

In the first mode, the incremental loop gain $g_m R_p$ is just slightly higher than unity. When the oscillator amplitude in that case is smoothly limited by the third-order nonlinearity of the differential-pair transconductance, the circuit behaves as a Van der Pol oscillator. In this mode of operation, small variations, either in the resonance-circuit impedance or in the bias current,

may easily result in turn-off or in an increase in amplitude and a much stronger limiting action.

In the second mode of operation the stronger limiting action is put to good use, and the differential pair acts as a current switch. As long as the output voltage of the circuit is so small that no saturation occurs, the output amplitude depends linearly on the tail current and on the resistance in the resonance circuit. Though less than in the previous situation, the output amplitude is still rather sensitive to parameter spread, and the appropriate level for the buffer is hard to guarantee.

In the third mode of operation, the tail current and the resistance of the resonance circuit are so large, and the collector-to-base voltage so small that either Q1 or Q2 saturates. During the peaks of the output voltage, the resonance circuit is short-circuited and the noise performance cannot be expected to be much better than in a regenerative oscillator.

The oscillator can be forced to operate either in the first or second mode by using well-known AGC techniques. These techniques, however, require a form of detection together with some low-pass filtering in order to control the magnitude of the tail current. The method presented here is intended to force the oscillator to operate in the second mode by using a novel AGC technique. The operation principle is illustrated in Figure 10. The tail current of the differential pair is modulated with the oscillator signal. In the waveform supplied to the resonance circuit the first-harmonic content is thus reduced, all the more so as the output amplitude increases, as depicted in Figure 11.

The differential pair providing the tail current is biased such that Q4 initially conducts and Q5 does not. After the oscillations are started, the amplitude at the base of Q4 will get a value such that this transistor will be driven out of conduction during the peaks of the oscillator signal. The amplitude will thus be fixed at a value closely corresponding to the DC bias voltage between the bases of the tail-current differential pair.

A complete circuit diagram of the oscillator-buffer combination is shown in Figure 12. The tuning range amply exceeds the required range of 10.85 - 12.32 MHz, so that no adjustments are needed for guaranteed acquisition of the frequency-synthesizer phase-lock loop.

The output sine-wave amplitude is fixed at a value of about 0.5 V, large enough to obtain a proper switching action of the buffer stage. A wide range of tank-circuit impedances can be used. Impedances as low as 1 kΩ still do not stop oscillations. With a resonance circuit with a Q of 50, the carrier-to-noise ratio at 9 kHz from the carrier is about 70 dB in a 5 kHz bandwidth. Since the adjacent-channel rejection in the IF filter is much smaller than 70 dB, the oscillator noise does not impair receiver selectivity.

The signal input of the mixer is driven from a differential-pair voltage-to-current converter using simple emitter degradation. As only low-frequency operation (up to 1600 kHz) is involved, the nonlinearity of this circuit can be solely attributed to the exponential relationship between V_{BE} and I_C. A straightforward calculation of the third-order intermodulation then shows that it hardly contributes to the intermodulation generated in the preamplifier when it is biased at a tail current of 10 mA and with 150 Ω degeneration resistors.

The noise contribution of the mixer as a whole (including the V-I converter) can be largely attributed to the V-I converter. As a consequence of the switching operation, not only is the noise of the input frequency band and the image frequency band converted to the IF frequency, but also the noise in the bands related to the odd oscillator harmonics. The low-pass filter effectively short circuits the equivalent noise current source of the V-I converter at frequencies higher than the cut-off frequency. So, only the base-band contribution is determined by both the equivalent input sources. A calculation of the various contributions leads to an equivalent input spectrum in series with the preamplifier output $S(v_{no}) = 4kT3700$. This source transforms into an equivalent source in series with the antenna voltage:

$$S(v_{eq,a}) = (\frac{C_f}{C_a})^2 \, S(v_{no}).$$

This noise source is significant in the case of low preamplifier gain (activated switch). In the high-gain situation (deactivated switch) the preamplifier noise dominates.

CONCLUSIONS

This paper presented an integrated front end for a long-wave and medium-wave AM car-radio receiver. The circuits are realized in a conventional bipolar process (f_T = 400 MHz). Thanks to the upconversion concept and the high dynamic range of the various circuits, the system needs no adjustments, thereby significantly reducing production costs. The second- and third-order IMFDR amount to 86 and 97 dB, respectively, in high field-strength situations, where an automatic gain switch in the preamplifier is activated. The maximum field strength that can be handled is 8 V/m.

ACKNOWLEDGEMENT

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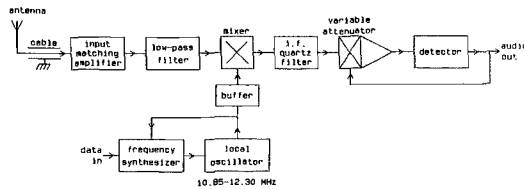

Fig. 1 Block diagram of an upconversion receiver.

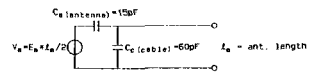

Fig. 2 Circuit representation of whip antenna and cable.

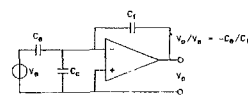

Fig. 3 Input-amplifier configuration with capacitive feedback.

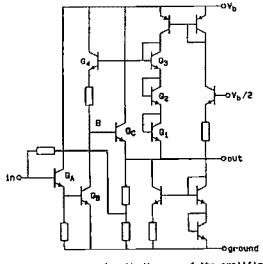

Fig. 4. Complete circuit diagram of the amplifier.

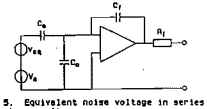

Fig. 5. Equivalent noise voltage in series with the antenna voltage.

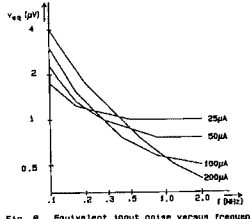

Fig. 6. Equivalent input noise versus frequency with bias current of the first stage as parameter.

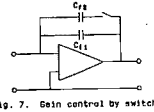

Fig. 7. Gain control by switching the feedback-capacitor values.

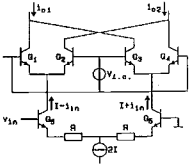

Fig. 8. Double-balanced switching mixer. V_{lo} is the local-oscillator signal.

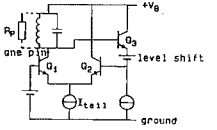

Fig. 9. Basic negative-resistance oscillator.

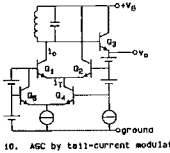

Fig. 10. AGC by tail-current modulation.

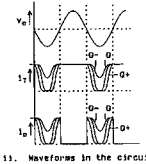

Fig. 11. Waveforms in the circuit of Fig. 10.

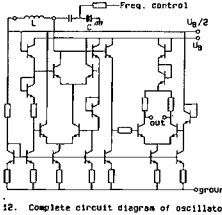

Fig. 12. Complete circuit diagram of oscillator-buffer.

DESIGN OF COAXIAL HIGH-PASS FILTERS HAVING VARIOUS TRANSFER PROPERTIES

by Dick Wainwright
Chief Scientist, Cir-Q-Tel, Inc.

Abstract: As explained in a companion paper 1/ "Design of Combline and Interdigitated Bandpass Filters" (usually with narrow band wide tuning range) the cost of construction depends heavily on the physical form assumed by the precision ground plane housing and the physical form and fit of the component parts/elements.

Various types of filters of highpass formulation are given. Pseudo-elliptic and all-pole Butterworth, Chebishev and other realizations such as Gaussian, etc. are described. The series capacitive elements may be formed as Teflon-insulated coaxial capacitors, the shunt elements of which may be composed of a simple helix or straight (coaxial) inductor for the all-pole designs or by a series inductor-capacitor combination for the Elliptic or Pseudo-elliptic high pass. n-odd values are in general preferred, which simplifies construction. Other classes of filters: Zobel, Levy A-Z, (Ref.6) Butterworth, Gaussian and Bessel all-pole (n-odd) are of similar consruction; however, the Bessel, various Gaussian realizations, Transitional, and the Inverse Chebishev Elliptic are, in general, unsymmetrical; thus they are somewhat more difficult to build.

Figures 2A and 2B are schematic diagrams highlighting the series 'C' capacitors of the devices described comprising the centrally located coaxial capacitors, the $C_{1+2}\cdots C_{n-2}$. These C_{odd} capacitors may be broken up into an array of two capacitors each in series to provide for the filter-internal 'C' series, the schematics for which are as shown in Figures 2B and 3B. This construction technique provides for accessible attachment of shunt elements 'L' or 'L-C'. Of course, these elements may be stepped as to diameter (see Fig. 4A and B) and plugged into each other, resulting in a lesser number of pieces in the construction, but somewhat more complicated in terms of component tolerance realization and assembly; in which case, the capacitors C_s are not present.

In general, n-odd equally terminated filters ($R_S=R_L=Z_o$ maximum power transfer terminations) have been assumed, i.e., n-odd: 3, 5, 7...n-odd.

The shunt elements connect at convenient accessible locations as shown in the various pictorial cutaway figures: 4, 5 and 6.

1/ "Design of Combline and Interdigitated Bandpass Filters"

These Figures 4, 5 and 6 all include schematic of (actual) the complete high pass filter (type of shunt element(s) optional for Chebishev all-pole or Pseudo-Elliptic high pass filter); note capacitors C_s, 1-3, C_s, 3-5, etc. (See Note, Figure 5.)

Note: In suspended substrate (SSS) or strip/microstrip designs the dual of the networks shown may conveniently be used.

Patent protection has been applied for on these device designs.

The determination of element values follows standard design procedure which is described in the references. See example pages 8, 9 and 10.

REFERENCES FOR FURTHER READING

Ref. 1: "Microwave Engineers' Handbook", Artech House, Inc., Horizon House-Microwave, Inc., Theodore S. Saad, Editor. Co-editors: R.C. Hansen, C.J. Wheeler, Library of Congress Card No. 76-168891

Ref. 2: Frederick E. Terman, "Radio Engineers Handbook", McGraw Hill Book Co., Inc., New York. 1943; First Edition

Ref. 3: Anatol Zverev, "Handbook of Filter Synthesis", John Wiley & Sons, New York, Library of Congress Card No. 67-17352

Ref. 4: D.J. McLean, "COCCl Insertion Loss Design of Electric Filters", Technical Report No. 2, 1956, Stanford Electrical Laboratories, Stanford University. Prepared under ONR Contract No. 225(4), NR 373 360

Ref. 5: L. Young, G.L. Matthaei, E.M.T. Jones, "Microwave Filters, Impedance-Matching Networks and Coupling Structures", McGraw Hill Book Co., Library of Congress Catalog No. 64-7937

Fig. 6: R. Levy, Generalized rational function approximation in finite intervals using Zolatarev functions, IEEE Trans. Microwave Theory Tech Vol. MTT-18, Dec. 1970 pp. 1052-1064

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Ronald B. Alexander, Esq., Board Chairman; Douglas H. Alexander, President; Hilda A. Wainwright, Vice President & Corporate Treasurer; Ann McCauley, Exec. Sec., Norman Selinger, Sales Manager; Joan King and Jay Kociol for proofreading and helpful hints; Dorothy DeWitt, my secretary for her hard work, patience and understanding, and to all of the fine people at Griffith & Coe Advertising, Inc. of Hagerstown, Maryland for their expert artwork.

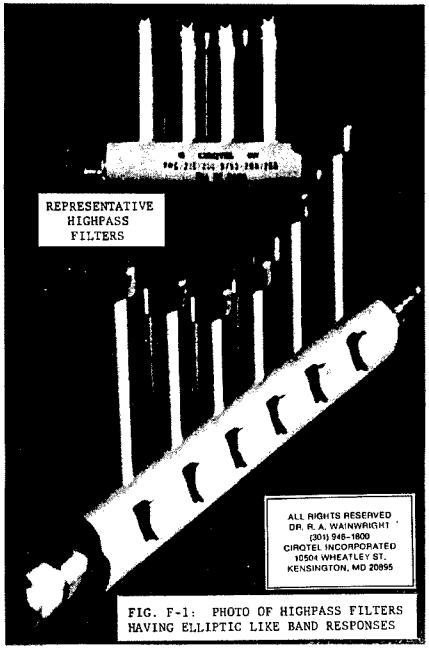

FIG. F-1: PHOTO OF HIGHPASS FILTERS HAVING ELLIPTIC LIKE BAND RESPONSES

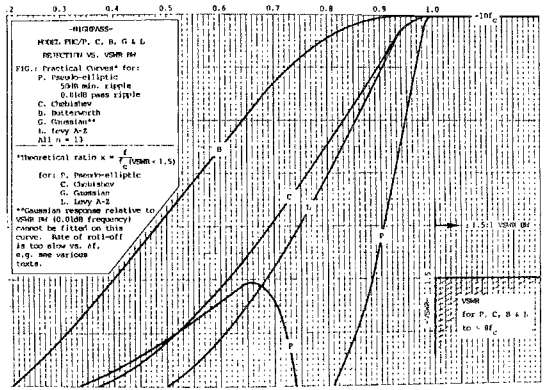

FIG. F-2: PRACTICAL CURVES FOR REPRESENTATIVE HIGHPASS FILTERS

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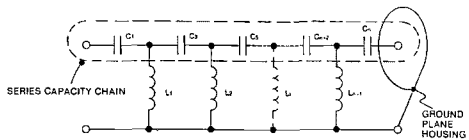

FIG. 2A1 TYPICAL SCHEMATIC, n odd, ALL-POLE HIGH PASS FILTER

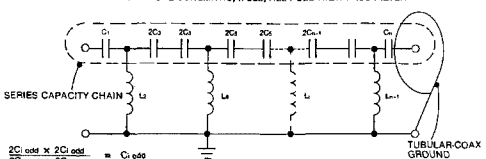

FIG. 2A2 SCHEMATIC DIAGRAM, IDEALIZED FOR SPLIT 'C' SERIES CTR.

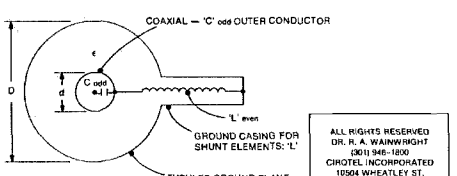

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FIG. 2A3 END VIEW OF FIG. 2A2.

NOTE: THE TUBULAR GROUND-PLANE ENCASING THE SERIES CAPACITY CHAIN $C_1, C_3, C_5 \ldots$ C odd IDEALLY PROVIDES FOR A $Zo = Rg = R_L$ CONFIGURATION (CO-AXIAL) TO PROVIDE FOR A WIDE-BAND MATCH TO FREQUENCIES ($f > 2$ fc to f mode) WELL ABOVE THE CUTOFF FREQUENCY. f mode is that frequency above which a tube of diameter D no longer supports a TEM wave.

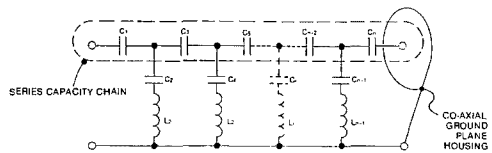


FIG. 2B1 TYPICAL SCHEMATIC, n odd, ELLIPTIC-LIKE LOW PASS FILTER

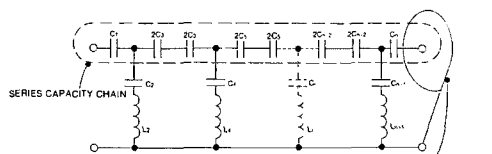
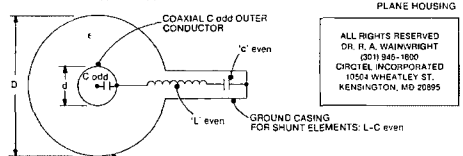


FIG. 2B2 IDEALIZED SCHEMATIC DIAGRAM OF ELLIPTIC-LIKE HIGHPASS FILTER, SHOWING SPLIT CENTRAL 'C' SERIES.



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TUBULAR GROUND PLANE, CASING FOR 'C' odd CAPACITORS

FIG. 2B3: END VIEW OF FIG. 2B2

NOTE: THE TUBULAR GROUND-PLANE ENCASING THE SERIES CAPACITY CHAIN $C_1, C_3, C_5 \ldots$ C odd IDEALLY PROVIDES FOR A $Zo = Rg = R_L$ CONFIGURATION (CO-AXIAL) TO PROVIDE FOR A WIDE-BAND MATCH TO FREQUENCIES ($f > 2$ fc to f mode) WELL ABOVE THE CUTOFF FREQUENCY. f mode is that frequency above which a tube of diameter D no longer supports a TEM wave

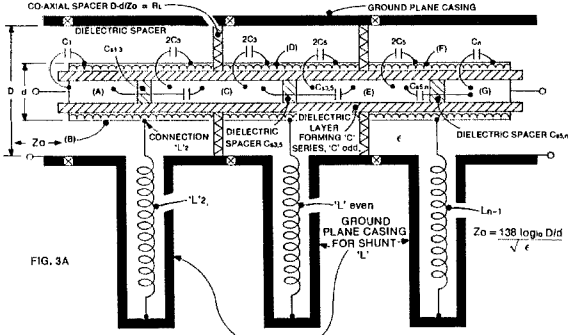

FIG. 3A

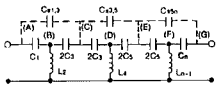

FIG. 3B, n = 7, ALL POLE, COAXIAL HIGH PASS FILTER — ACTUAL SCHEMATIC DIAGRAM.

FIGURE 3 A, B: PICTORIAL CUTAWAY VIEW SHOWING RELATIONSHIP OF ALL PARTS & SCHEMATIC DIAGRAM.

ALL POLE — (CONSTANT 'K' CONFIGURATION) REFERENCE FIGS. 2A2 AND 2A3

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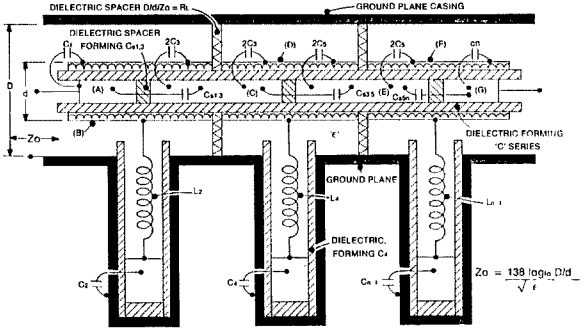

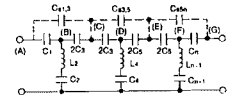

FIG. 4B: 7 POLE, 3 ZERO, COAXIAL HIGHPASS FILTER, SCHEMATIC

FIGURE 4 A, B: PICTORIAL CUTAWAY VIEW SHOWING RELATIONSHIP OF ALL PARTS AND SCHEMATIC DIAGRAM REF FIGS. 2B1 AND 2B2

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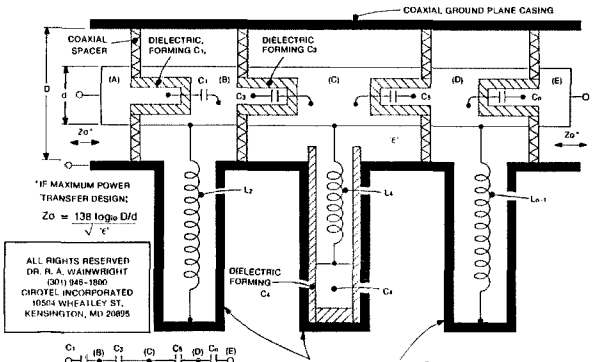

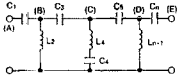

FIGURE 5A,B PICTORIAL CUTAWAY VIEW SHOWING RELATIONSHIP OF ALL PARTS AND SCHEMATIC DIAGRAM.

FIG. 5B, n = 7, 7 pole-1 ZERO COAXIAL HIGH PASS FILTER SCHEMATIC

(PATENT APPLIED FOR)

EXAMPLE:

DESIGN A HIGH PASS FILTER TO THE FOLLOWING SPECIFICATIONS

1. PASSBAND: 0.9 ≥ 4 GHz; LOSS ≤ 0.5 dB
2. Zo = 50 ohms, passband VSWR ≤ 1.5-1
3. REJECT ≤ 500 MHz: ≥ 35 dB
4. CONNECTORS: N(F) IN; N(M) OUT

FROM REFERENCES; ALLOWING DESIGN MARGIN, SET fc AT 800 MHz THEN:

$$\frac{fc}{fr\ (>35dB)} \sim \frac{800}{500} = 1.6, \text{ indicating } n = 8,$$

USE n = 9 FOR SYMMETRICAL DESIGN (n-odd)

THEN COMPUTE ELEMENTS: (0.01 dB ripple)

$C_1 = 4.885$ pf $L_2 = 6.97$ n H
$C_3 = 2.205$ pf $L_4 = 5.808$ n H
$C_5 = 2.088$ pf

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SEE SCHEMATIC BELOW (FIG. E-1)

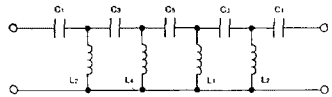

FIG. E-1; SCHEMATIC

RESULTING IN:

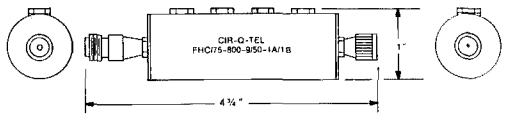

FIG. E-2 OUTLINE DRAWING HIGHPASS FILTER

WEIGHT: < 5 OZ.

THE RESPONSE CURVES: AMPLITUDE AND RETURN LOSS FROM 10 MHz - 10 GHz IS GIVEN IN FIG. E-2 A AND B
LOSS: < 0.5dB FROM 0.850-4.7 GHz
VSWR: < 1.5:1 FROM 0.810-4.6 GHz
REJECTION: > 35dB at ≤ 535 MHz

FIG. E-2A
AMPLITUDE RESPONSE OF EXAMPLE DESIGN FIG. E-1 (MEASURED)

FIGURES E-2B
RETURN LOSS RESPONSE (MEASURED)

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HIGH POWER FILTERS

Specsmanship & Design Considerations

By Dick Wainwright, Chief Scientist
Cir-Q-Tel, Inc.

Abstract:

Blivetry*: power; feasibility; Q: selectivity; gradients; hot spots; energy storage; contaminants; ionization; breakdown; peak-average; C.W.; A.M.; % modulation; F.M.; etc.; volt-amps; connectors; size; weight; heat generation, flow & sinking; ionization; impacting; altitude; humidity; salt spray; insulation; shock; vibration; harmonic content; rejection; source & load; EMI; form factor; skin depth-plating; dissipation factor; dielectric strength; topology; susceptibility; losses; volts; amps; volt-amps; Q; MTBF; manufacturers ratings & reality; heat; heat flow; - - all are but a smattering of the flow of words/thoughts that haunt every sensible designer of high power devices. (Notice: certain key words were repeated to emphasize their importance.)

*Blivetry: The art of defying the basic laws of physics by forcing two or more objects to fit into the same space - analogous to fitting ten pounds of parts into a one pound container.

Customers, bless them, generally think of filters as bandaids - one often hears the uninformed say, "Anyone can design filters - the textbooks are full of tables of element values". That is true, but volts and amps and concomitant happenings make a difference. "The ratings", not the values, are of fundamental importance in power handling devices, design and application. A little experience usually results in a lot of smoke testing.

An intimate knowledge and an awareness bordering on paranoia, plus considerable experience are fundamental requisites.

The writer has on innumerable occasions lost the "first go-around" on a project bid on the basis of: price, size, weight and exceptions prudently taken, in some instances, because the user did not know or furnish such very important information as:

a. Harmonic content of transmitter power output relative to fundamental power
b. Possible incompatibility of specified connectors with specified power and load conditions
c. The amount of surface area available for heat conduction/radiation and/or availability of cooling air. Assuming that cooling air is available, the rate of air flow, pressure, as well as the temperature of the cooling air, must be known.

d. Heavy shock and vibration specifications were specified along all three major axes when in fact the application, under power, was indoors and fixed.

e. Specifications indicating unrealistically low values of device VSWR (e.g. 1.1:1) when in fact the filter would in practice be operating continuously into loads of never less than 2:1 and often in excess of 3:1 VSWR. (In some cases an infinite VSWR of any phase) Specified selectivity, i.e., ratio of "f" low-reject/"f" high pass ($f_{p(high)}$ was given as very nearly 1:1; and it is not unusual to find specifications indicating selectivity ratio values of 1.01:1, 1.02:1, etc. When using a number of filters to cover a broad range of frequencies it is usually best to uniformly distribute the power pass band and reject to pass ratios to avoid undue stress on any of the filters: see Example (1).

f. Other mitigating relationships that, taken as whole, result in unrealistic designs.

Taking it from the top, a-f:

a. Harmonic content of transmitter output:

Typical solid state transmitters, of recent vintage, can be expected to yield harmonic power levels of (push-pull final through combiner to 50 ohms unbalanced): Table 1

TABLE 1

Harmonic Order		Level dBc	Harmonic watts/KW (fundamental)
2nd	:	-18	15.8
3rd	:	-12	63.1
4th	:	-21	7.9
5th	:	-18	15.8
6th	:	-22	6.3
7th	:	-21	7.9
8 - 13	:	Avg. -22	37.8) Avg.: 6.3W/harmonic

Total Harmonic Power: 154.6 watts/KW fundamental power

As an aside, note at this juncture that the customer may wish to use a ferrite isolator at the transmitter output to obtain a well-matched transmitter output, but, through oversight, may neglect the fact that most isolators are frequency sensitive, resulting (possibly) in excessive heating by harmonics, resulting in isolator burn-out and/or additional harmonic generation caused by the ferrite being operated near the Curie temperature of the materials, etc.

(b) Connectors power rating insufficient for application. Most connector manufacturers haven't the foggiest idea of how much power/apparent power their connectors will safely handle. Current ratings, not voltage ratings, are generally the problem drivers. Z_o is of little consequence in systems working with very high VSWR values - of course they are directly related.

Given the fact that most filters are "reflective devices" i.e. produce attenuation by reflection of power rather than being absorptive, absorptive filters are generally much more expensive and generally considerably larger than reflective devices. However, in many UHF and above, frequency range applications the use of harmonic absorptive filters may make a lot of sense.

(c) How much surface area should one allow for the cooling of high power filters, and, if cooling air is available, what is its pressure and rate of flow?

First one may make the assumptions:

1. The maximum power vs. connector type is in the order of 2/3 of the cable attached, derated appropriately.
2. Normally a high power filter ("hot" surface temperature) is designed such that the hot surface temperature of the filter does not exceed ambient C° + 50°C with a heat sinking plate average temperature of no more than ambient air C° + 10°C= +95°C max. Cooling air, if available, should not exceed an effective temperature of +80°C; hence, air speed may be an important consideration as the air approaches the filter hot spots.

In many cases substantial size fins may be required but fins are not very effective in cramped air flow spaces - convection air currents must be free to circulate if convection cooling represents a substantial portion of the cooling means, and surrounding heat conducting surfaces may need to have rough surface to "wipe" the heat out of the circulating air.

(d) Heavy shock and vibration specifications along all three major axes, i.e., G forces applied to coaxial filters should be studied carefully and if at all possible, the strong G forces should be confined to the smaller dimensions of the coaxial structure. Minimal forces of no more than 5G, preferably, and no more than 10G max. (11 m/sec. std. shock specifications) on the length should be applied to coaxial high power filters of substantial size, plus consideration as to the adequacy of mounting hardware and supporting structures is essential.

(e) Selectivity, time delay, energy storage & electrical (absorptive) losses/heat generation go hand in hand.

Q: The ratio of:

$$\frac{\text{Energy Stored per Cycle}}{\text{Energy Dissipated per Cycle}}$$ of the applied energy

is a critical consideration in the design of all filters in general, and is of great importance in high power filters. For a given loss, the required ratio of Q unloaded/Q loaded is different for every filter design. It is not uncommon for certain designs to require inductor Q unloaded values in excess of 500-1000 or more and for capacitors 3500-8000 or more to barely eke out a responsive design, where rejection bandwidths to low loss band edge ratios are quite small, say much less than 1.2:1 for 40-60 dB rejection; almost impossible values

of 2000 or more for coil Q and over 10,000-15,000 capacitor Q may be required, but unobtainable because of space, moding and/or frequency limitations.

The Q of coils increases roughly as the square root of frequency, hence generally high frequency filters yield lower losses, given the same selectivity and available space.

For a given loss (see Table 2) the unloaded Q required increases substantially with passband ripple (VSWR), complexity, n and type of filter. (Elliptic, all-pole Chebishev, Butterworth, etc.).

TABLE 2

Selectivity f60dB/f3dB	Nominal VSWR	Filter Design	Representative Qul. for a Given Loss (approx.)	Energy Storage
1.25	1.2	Elliptic (0.01 dB Ripple)	1000	20
1.5	1.35	Chebishev (all-pole) ripple=0.1 dB	650	15
1.7	1.2	Chebishev (all-pole) ripple=0.01 dB	460	12
-	-	Chebishev (all-pole) ripple=0.001 dB	290	-
2.1	1.2	Butterworth	200	10
4.2	-	Bessel		-

Table 2 indicates representative values - not absolutes.

As an example, a 0.01 dB Chebishev (all-pole) filter required approximately $\frac{460}{200}$ -1$\sim$84% more Q than a Butterworth filter for a given loss and the Elliptic filter given has twice the energy storage indicating that voltages and currents are roughly 40% more than in a Butterworth filter.

(f) Other factors of consequence:

(1) Phase linearity vs. f.

(2) Matching of phase: A $\pm$ 5° phase matching specifications may nearly double the price relative to a non-matching phase unit because of the component tolerance problem alignment accuracy and the need to "fix" parts to preclude minute variations in operating environment.

(3) Humidity: High humidity conditions, especially with condensation presents substantial problems.

(4) Altitude: Derating or pressurization with dry nitrogen or sulfur hexafluoride may be forced as a solution. Of course, pressurization eliminates humidity problems.

(5) etc.

The author wishes to thank the following people who were very helpful in the preparation of this paper as well as for the permission of the management of Cir-Q-Tel to publish these data and information:
Ronald B. Alexander, Esq., Board Chairman, Douglas H. Alexander, President; Hilda A. Wainwright, Vice President & Corporate Treasurer; Ann McCauley, Executive Secretary/Office Manager; Norman Selinger, Sales Manager; Joan King & Jay Kociol for proofreading and helpful hints; Dorothy DeWitt, my secretary, for her hard work, patience and understanding, and to all of the fine people at Griffith & Coe Advertising, Inc. of Hagerstown, Maryland for their expert artwork.

Addenda to: High Power Filters, Specsmanship
and Design Considerations -
by: R.A. Wainwright

Suppose one wishes to provide filters covering the 100-1000 MHz frequency range that will in turn yield greater than 40 dB attenuation at the second and higher order harmonics; let Nf be the number of contiguous band filters.

First, determine the number of octaves included in this band: 100-1000 MHz (an octave is a 2:1 frequency ratio).

Then:

(1) 100-200 MHz - 1st octave

(2) 200-400 MHz - 2nd octave

(3) 400-800 MHz - 3rd octave

(4) 800-1600 MHz - 4th octave (up to 1000 MHz is all the coverage that is required however,

or

On: octave number is an integer: On 2^{Nf}. If one is to evenly distribute the filters such that: Note all logarithms are to base 10.

[1] $Ki = \frac{fc\ (VSWR)\ high}{fc\ operate(VSWR)\ low}$ is about the same for all filters, then given: $KNf = \frac{1000}{100} = 10$

then for each filter Ki

[2] $K(Nf) = 10 = Ki^{Nf}(1)$ etc.; $Nf = 4$ (filters minimum)

Then: $\frac{\log 10}{Nf} = \log Ki$

and

Ki=(antilog 10)/4 =1.77827941

(see Fig. E-1)

If 5 filters were to be used, which number will be determined upon evaluation of filters chosen for this task, then, (see Fig. E-2)

if Nf=5

Then

Ki=(antilog 10)/5 =1.584893192

Assuming 4 or 5 filters, then develop Table 1

Table 1

VSWR Passband of Filters 1-4 or 1-5

Ki		1	2	3	4	5
1.78	Nf=4	100-178	178-316	316-562	562-1000	-
1.56	Nf=5	100-158	158-250	250-395	395-628	628-1000

From Fig. E-4 for N(f)=4 or 5 given Ki=1.78 and Ki=1.58 respectively, assuming an elliptic-like response device is compatible with other electrical parameters, ratings, etc.; Then:

The ratio of the lowest 2nd harmonic frequency (2fL) to highest passband (VSWR) frequency (fcH) for Nf=4 and 5 are

as given in Table 2

Table 2

	Filter 1 (2fL/fcH)	Filter 2 (2fL/fcH)	Filter 3 (2fL/fcH)	Filter 4 (2fL/fcH)	Filter 5 (2fL/fcH)
Nf=4	200/178= 1.123	1.123	1.123	1.123	1.123
Nf=5	200/158= 1.26	1.26	1.26	1.26	1.26

From Fig. E-2, [(2fL/fcH) -1]=0.123 absissa (frequency scale) and: rejection + return loss= 60 dB ordinate. If return loss is selected as 20 dB VSWR approx. 1.25:1) then 40 dB rejection + 20 dB return loss = 60 dB at 0.123 and 0.26 respectively (absissa value on Fig. E-4).

For Nf=4: at 0.123 (abissa) and 60 dB: rejection + return loss (ordinate) one finds n=11 (elliptic) filter. (see mark "°")

For Nf=5: at 0.26 (absissa) and 60 dB on ordinate. (see mark "x"), n=9 (elliptic) filters, (Fig. E-2).

If on the other hand one wishes to use an all-pole 0.01 dB ripple Chebishev, (of practical construction) ladder network series coil, and shunt capacitors, with no finite frequency traps

Then: for n=19 the ratio: fcH/2fL=1.36 for 40dBc attenuation, (note: Chebishev filters having more than 19 elements, n = 19

are not generally considered practical) it becomes apparent that additional 10-1000 MHz band segmentation may be necessary, (see Fig. E-3 and Table 3.

If: fcH/2fL = 1.36 then solving for Nf (minimum), fL(1)=100 MHz, then 1.36 fcH =2fL =200 MHz

Then fcH(1)=200/1.36=147 MHz

Proof: $1.47^6 = 10 = 10.09029837$

Please be aware that the Tables and graphs given herein Do Not List Theoretical Values.

Figures E-1, E-2 etc. are self explanatory. For all-pole (equi-ripple passband and monotonic reject band) Chebishev filters the reject band attenuation (dB) given by

[Eqn. 5]

$$dB\ @fx = 10 \log\left\{\left[1 + \log^{-1}\frac{\alpha r(dB)}{10}\right]\cosh^2\left[n \cosh^{-1}\left(\frac{fx}{fcH}\right)\right]\right\} fx > fcH$$

where: [fx(dB] is the frequency of x(dB) of rejection α r is the specified pass band ripple (dB)

fcH is the theoretical passband upper end, i.e. equi-ripple band edge. Table 3 gives the (practical) values of the rejection and frequency parameters for 0.01 dB ripple (α r) in the pass band for various practical n odd values. Practical filter intrinsic-matched conditions, VSWR values between 1.25 & 1.4:1 will in general be obtained depending on practical component tolerances. Table 3 lists (practical) ratios of f(xdB)/fcH

for all-pole Cheblshev filters. Where α_r =0.01 dB (passband ripple)

Table 3

Table of Practical Values of f(dB)/f_c(high) for x dB Rejection for 0.01 dB ripple, practical, VSWR: 1.25:1 Chebishev all-pole ladder

n	20dB	30dB	40dB	50dB	60dB	70dB	80dB	90dB
7	1.8	2.15	2.75	3.4	4.2	5	-	
9	1.52	1.80	2.15	2.5	3.0	3.5	4.0	
11	1.42	1.73	1.85	2.1	2.42	2.75	3.1	
13	1.32	1.50	1.70	1.90	2.15	2.38	2.65	
15	1.23	1.37	1.55	1.72	1.94	2.15	2.36	2.60
17	1.15	1.28	1.44	1.60	1.77	1.95	2.14	2.30
19	1.12	1.21	1.36	1.52	1.64	1.78	1.90	2.06

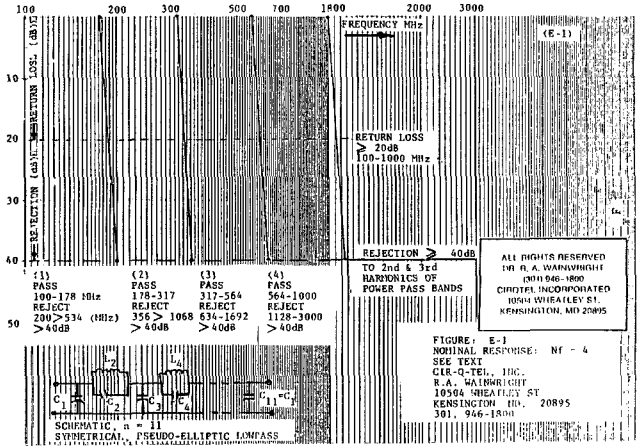
FIG. E-3 might well be a graphical specification for a set of 6 filters spanning the 100-1000 MHz power passband where Ki=1.47 and 40dB is obtained as harmonic rejection. Additional figures show Typical-All-Pole-Lowpass Filters.

Table 4*

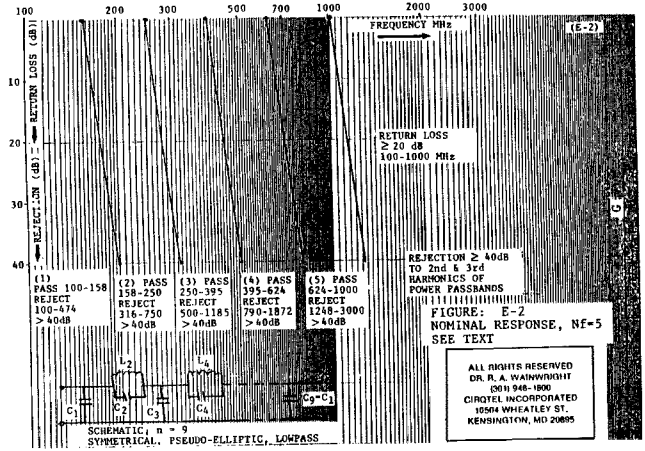
Passband VSWR/ripple (dB)

VSWR	2	1.8	1.5	1.4	1.36	1.3	1.24	1.2	1.1	1.05
ripple	0.51	0.37	0.18	0.12	0.10	0.07	0.05	0.035	0.01	0.0026

* Ref: Cir-Q-Tel, Inc. catalog (since 1962) page 35, Table 28



(E)


100
200
300
500
700
1000
2000
3000
FREQUENCY MHz
(E-2)
RETURN LOSS (dB)
REJECTION (dB)
10
20
30
40
RETURN LOSS
≥ 20 dB
100-1000 MHz
REJECTION ≥ 40dB
TO 2nd & 3rd
HARMONICS OF
POWER PASSBANDS
(1) PASS 100-158 REJECT 100-474 >40dB
(2) PASS 158-250 REJECT 316-750 >40dB
(3) PASS 250-395 REJECT 500-1185 >40dB
(4) PASS 395-624 REJECT 790-1872 >40dB
(5) PASS 624-1000 REJECT 1248-3000 >40dB
FIGURE: E-2
NOMINAL RESPONSE, Nf=5
SEE TEXT
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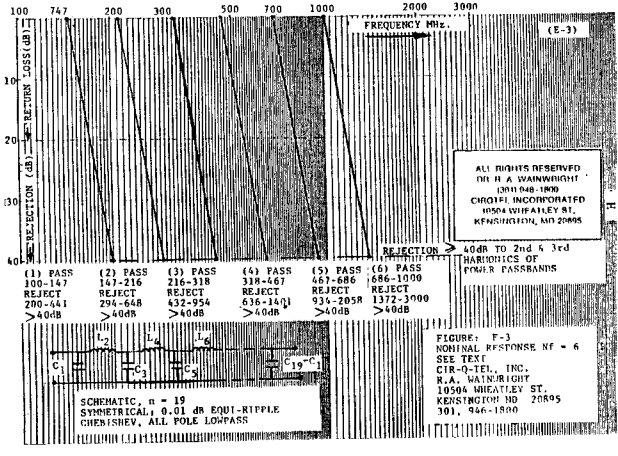
(301) 946-1800
CIROTEL INCORPORATED
10504 WHEATLEY ST.
KENSINGTON, MD 20895
SCHEMATIC, n = 9
SYMMETRICAL, PSEUDO-ELLIPTIC, LOWPASS


100
747
200
300
500
700
1000
2000
3000
FREQUENCY MHz.
(E-3)
RETURN LOSS (dB)
REJECTION (dB)
10
20
30
40
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DR. R. A. WAINWRIGHT
(301) 946-1800
CIROTEL INCORPORATED
10504 WHEATLEY ST.
KENSINGTON, MD 20895
REJECTION → 40dB TO 2nd & 3rd HARMONICS OF POWER PASSBANDS
(1) PASS 100-147 REJECT 270-441 >40dB
(2) PASS 147-216 REJECT 294-648 >40dB
(3) PASS 216-318 REJECT 432-954 >40dB
(4) PASS 318-467 REJECT 636-1401 >40dB
(5) PASS 467-686 REJECT 934-2058 >40dB
(6) PASS 686-1000 REJECT 1372-3000 >40dB
FIGURE: E-3
NOMINAL RESPONSE Nf = 6
SEE TEXT
CIR-Q-TEL, INC.
R.A. WAINWRIGHT
10504 WHEATLEY ST.
KENSINGTON MD 20895
301, 946-1800
SCHEMATIC, n = 19
SYMMETRICAL, 0.01 dB EQUI-RIPPLE
CHEBISHEV, ALL POLE LOWPASS

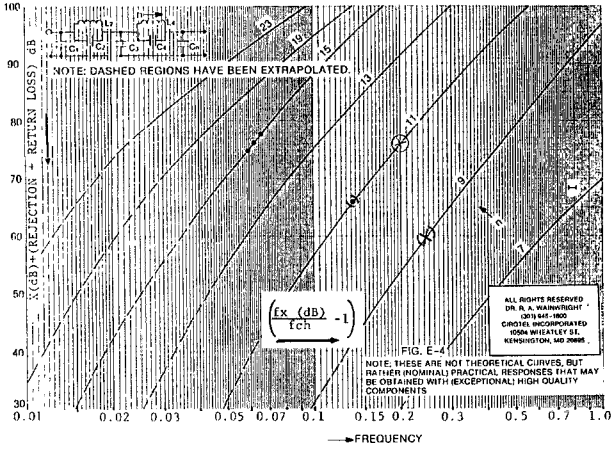
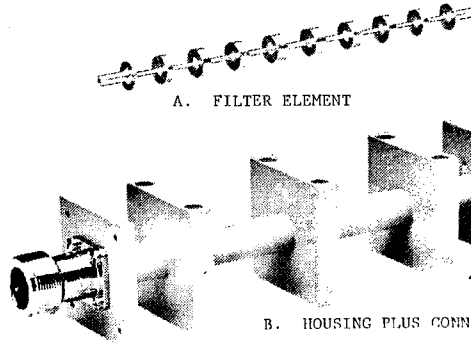


FIG. E-4



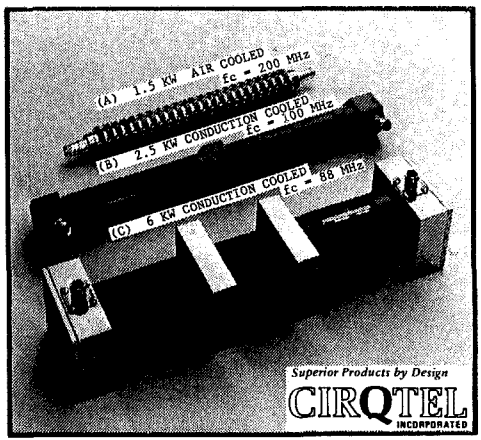
A. FILTER ELEMENT

B. HOUSING PLUS CONNECTOR,

FIG. E-5

LEVY A-Z, n=19 -2KW C.W. 2:1 LOAD-HIGH POWER LOW PASS FILTER; fc = 1.65 GHz
PASSBAND LOSS: 0.1dB TYPICAL

CIRQTEL INCORPORATED



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QUASI-LOWPASS FILTER

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Similar highpass filters from < 1 MHz - 2 GHz.

Why the Levy A-Z?

1. Virtually unlimited variation of all poles...Bessels-Chebishev, sometimes referred to as "BCL", but more appropriately "the Levy A-Z" Wheelpox using Achieser & Bolotarev's arithmetic).
2. Handles much more power (in almost every case) than Chebishev types + steeper responses with a lesser number of elements. This means lower loss and higher power in a smaller package (e.g., 0.07dB max. loss over f_c/VSWR2 1M in 15-pole. f_c-1850 MHz, 1.5KW filter). (An equivalent Chebishev went up in smoke.)
3. Lowpass filters are seldom required to respond to DC. Our highpass filters to infinity. By trading off around passband ripple for selectivity, and a wide range of filter f_c, we get:
   - added spurious (unrequiring) response-free bandwidth.
   - easily realizable multi-section, passband-limited (or sliver), lowpass or highpass, unusually configured filters; hence, inherently low-cost filters having time-proven subsidiarity in hostile environments.
   - an inherent construction that is far more rigid and reliable than older models of the same externally configured (Chebishev) types and, for that matter, most of the box-like suspended substrate filter configurations.

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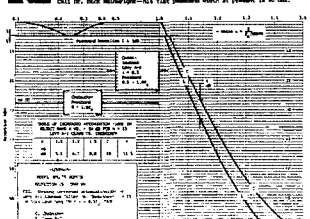

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<1.25:1 VSWR
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3.5-5 GHz >30dB rejection
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AN I F LIMITING AMPLIFIER DESIGN ON "K" SOFT BOARD

by

Steve Chambers
Section Head
Discrete and Module Engineering
ACRIAN, INC.

Discriminators have long been used in receiver design for the reception of FM, PM and FSK signals (Frequency Modulation, Pulse Modulation and Frequency Shift Keying). Unfortunately, discriminators are susceptable to instantaneous amplitude pertavation of the modulated carrier. Therefore, because detected noise may be misconstrued as meaningful data, it is necessary to limit the peak amplitude swing to the carrier. For this purpose, Acrian has designed a limiting I F amplifier.

The limiting amplifier design that will be described in this article will limit the peak amplitude swings of the carrier. At the same time, it will establish the receiver's dynamic range, the signal to noise ratio, and other important parameters of the receiver.

Table I describes the key performance requirements of the limiting amplifier. These key performance requirements are the signal to noise ratio, signal power, noise power, intermodulation distortion, noise pedestal flatness, and frequency range. Note that the signal to noise ratio is -60 dBc with an input of -50 dBm. The signal power output is +10 dBm with a -50 to +10 dBm signal input. The noise power, with a -97 KTN noise power input, must also have a +10dBm output. The intermodulation distortion requirement is -19 dBc. The noise pedestal flatness across the frequency range of 1 GHz + 50 MHz is +5 dB. The noise power requirement of this limiting amplifier design serves to quiet the receiver when no signal is present.

KEY PERFORMANCE REQUIREMENTS

* SNR; -50dBM - INPUT = -60DBC
* SIGNAL POWER, - -50 TO +8DBM INPUT = +10DBM
* NOISE POWER, - -97 KTN NOISE INPUT = +10 DBM
* I M D = -19 DBM
* NOISE PEDESTAL FLATNESS = 5 DB @ 50 MHZ
* FREQUENCY = 1000 ± 50 MHZ

THE NOISE POWER WAS REQUIRED TO QUIET THE RECEIVER WHEN NO SIGNAL WAS PRESENT.

TABLE I

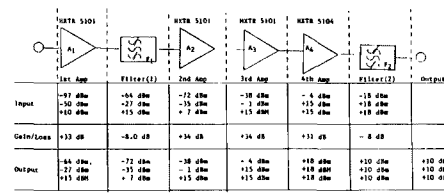
Block Diagram I and Table II shows the allocation of performance by stage. There are four amplifier stages and two filters. The amplifiers each contribute approximately +34 dB gain for a total of 130 dB gain. The gain level of 130 dB is required to amplify the -97 KTN noise energy of the input up to a +10 dBm output. Stage A1 is biased somewhat differently than the other three amplifiers to establish the noise figure of the total amplifier. Filters F1 and F2 both have an insertion loss of -8 dB due to the installation of 3 dB pads at both input and output. Amplifiers A1, A2 and A3 all use HXTR-5101 transistors, while the output amplifier A4 uses HXTR-5104 transistors for a higher saturated output level. Amplifier A1, while establishing the noise figure of the amplifier, also has the widest range of input level (from -97 KTN to a +10 dBm input). Its output saturates at +15 dBm of output power due to the use of the HXTR-5101 transistor.

The block diagram shows that as we get further down the amplification path, each of the amplifier stages is going into hard saturation. This causes a problem in the first layout.

As previously stated, the amplifier A1 establishes the signal to noise ratio (SNR) of the total amplifier. Filter F1 sets the noise bandwidth. Amplifiers A1 thru A4 combine for a total of 130 dBm gain. Filter F2 shapes the signal bandwidth, and Amplifier A4 is in a limiting mode for all input signals.

One of the problems of this design is that all the amplifiers are in hard saturation with the +10 dBm input to the first stage. Amplifier A3 is in a hard saturation at the -51 dBm input level. Ideally, amplifier A4 should be the only amplifier in saturation. This causes several types of problems. When an amplifier stage has an overdriven base emitter junction, the bias becomes negative and the second harmonics increase to a level equal to that of the fundamental signal. This overdriven condition causes this stage to become a good multiplier. It also causes what is known as the McDonald Effect. The McDonald Effect occurs when the emitter-base junction is overdriven by an input signal over an extended period of time. Hot carriers build up in this junction. With hot carriers in the junction, the HFE or Beta of the device goes to 0, limiting the gain of the device.

ALLOCATION OF PERFORMANCE BY STAGE



HXTR - 5101 is in hard saturation at +15 dBm output
HXTR - 5104 is in hard saturation at +21 dBm output

BLOCK DIAGRAM I

ALLOCATION

- AMPLIFIER A_1 ESTABLISHES THE SNR
- FILTER F_1 SETS THE NOISE BAND WIDTH
- AMPLIFIERS A_1 -A_4 COMBINE FOR 130 DB OF GAIN.
- FILTER F_2 SHAPES THE SIGNAL BAND WIDTH
- AMPLIFIER A_4 IS IN A LIMITING MODE AT ALL INPUT LEVELS.

PROBLEM

- ALL AMPLIFIER IN HARD SATURATION AT THE +10 DBM INPUT
- AMPLIFIER A_3 IS IN HARD SATURATION AT THE -50 DBM INPUT

TABLE II

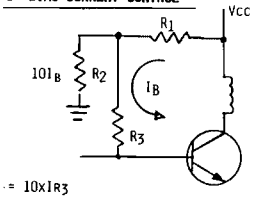
There are solutions to these design problems. First, it is imperative that we establish a device Beta parameter for the vendor. Second, control of the bias current must be established. Passive limiting must also be added. Figure I shows the current divider ratio of base current to shunt current which is established at a 10:1 ratio. The shunt current is actually 10 times that of the base current. Under these conditions, the effect of the base voltage going negative is eliminated.

Figure II shows the adding of a Schottky barrier diode in a passive limiting application. These diodes clip the input signal, to all stages except for the last output stage, at a .4 Volt peak to peak swing. This can only be done with an FSK, PM or FM type signal and cannot be employed on an AM signal. The overall schematic of amplifiers A1 through A3, shown in Figure II, shows how each of the bases uses a Schottky barrier diode to add the passive limiting. Only one device now remains in an active limiting mode.

In order to design the matching network for amplifier A4, it is necessary to establish some large signal S parameters for the device. Table III shows the published small signal S parameters and the measured large signal S parameters at the appropriate VCE and collector current. In order to establish the optimum S parameters for designing the matching circuitry that works for the output stage, it is necessary to set up a special S parameter measurement test station. This test station employs a signal generator, circulators, an input and reflective power meter, a triple stub tuner, and a special 50 Ohm to 50 Ohm circuit with the transistor soldered in. Another triple stub tuner is used on the output, a spectrum analyzer (HP8410) is needed to check for second harmonic, and an output power meter will be required to obtain optimum output power.

After optimum performance is achieved at each individual frequency, the triple stub tuners are terminated at 50 Ohms and the transistor is removed from the circuit. The network analyzer is used to launch in and measure the output complex conjugate and the input complex conjugate of the device. Figure IV shows such a test setup.

o BIAS CURRENT CONTROL



$I_{R2} = 10xI_{R3}$

FIGURE I

o PASSIVE LIMITING

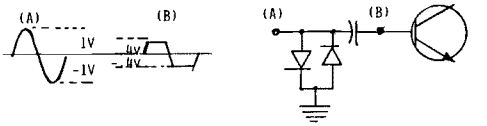


FIGURE II

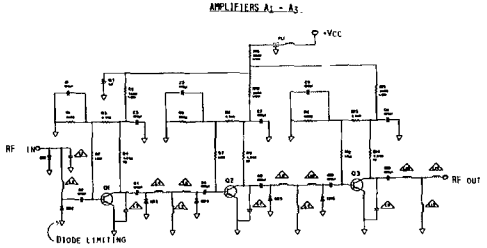


FIGURE III

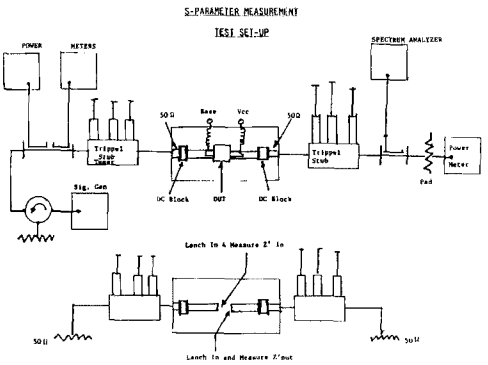


FIGURE IV

Block Diagram II shows the final line up of the devices using the passive diode limiting at each of the stages (except for the last device in A4). As indicated in the block diagram, the output saturated level of all the amplifiers is +9 dBm, well below the hard saturated output level. Only amplifier A4, with its good matching network for large signal parameters, is in saturation. This gives us a flat +10 dBm across the band of interest.

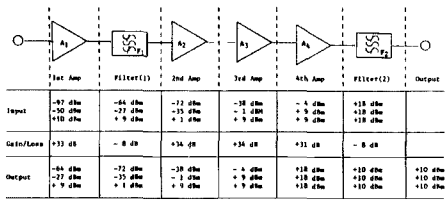
CIRCUIT CARD ASSEMBLY MATERIAL

When it was decided that high "K" Duroid material would be used for the construction of this amplifier, strong concerns were voiced by the production and manufacturing engineers. But there are both pros and cons of using the old standard of Kovar/Ceramic materials. On the positive side, Kovar/Ceramic works and we have procedures that are already in place to manufacture using this material. The thermal expansion of the Alumina/Kovar to the chips mounted on top is approximately the same. It is extremely stable down to -55 C, and we hold etching tolerances to 3 mils + 1mil.

On the negative side, using the Ceramic/COR system, extra drawings are required for the ceramic printed circuit board. Kovar is very heavy and costly to machine and plate. The Kovar carrier must be ultra flat, you must use thin film techniques for etching, and it requires a hot plate. In addition, the alumina substrate requires the use of laser drilling for the printed circuit holes.

While using the Duroid 610.5 material has some manufacturing handicaps (the fabricated boards must be bought outside, new internal manufacturing procedures must be devised, and there is a danger of pad lifting from excessive rework), the advantages are significant. The use of the Duroid material requires no ceramic drawings, Kovar carriers or flatness. The material is flexible and can be batched, stepped and repeated using MC equipment. Most of all, during breadboard testing it has passed temperature cycling on the breadboards from 0 through 85 C with components attached to the boards and using the alumina backing. No dielectric fractures have occured.

DIODE LIMITING PERFORMANCE BY STAGE



BLOCK DIAGRAM II

THE ACTIVE LIMITING STAGE

- THE LAST STAGE OF AMP A_Q IS THE TRUE ACTIVE LIMITER.
- MUST USE LARGE SIGNAL "S" PARAMETERS TO DESIGN THE INPUT AND OUTPUT MATCHING NETWORK.
- HP SMALL SIGNAL S-PARAMETERS

  VCE = 18V, IC = 110MA

S11	S21	S12	S22
.64 ∠179	3.7 ∠ 69	.08 ∠32	.32 ∠ -90

- MEASURED LARGE SIGNAL S-PARAMETERS

  VCE = 10V IC = 35MA

S11	S21	S12	S22
.70 ∠169	1.5 ∠ 78	.10 ∠ 64	.21 ∠-105

TABLE III

CONCLUSION

When designing an IP limiting amplifier that requires 130 dB gain, passive limiting is critical at each individual stage except for the last output stage. The last stage, which is actually doing the active limiting, must have large signal S parameter data taken in order to establish good input and output matching networks. Passive diode clipping or limiting can only be used with FSK, FM or PM type modulation, and cannot be used for AM. High "K" Duroid material makes an excellent material for this type of circuitry.

DESIGN OF COMBLINE and INTERDIGITAL BANDPASS FILTERS

by Dick Wainwright
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Abstract: The economic design of parallel coupled bandpass filters, e.g. interdigitated and combline having rod (finger-like), helical coil and annular ring inductive elements with necessary tuning capacitors Ct, in precision machined rectangular box-like (ground plane) containers can be an expensive proposition, especially given the fact that the average purchase order quantity for such devices is in the order of 10-15 units. Hence, in general, the savings resulting from volume manufacturing processes are not available.

Standardization is in many organizations a sometime thing. The cost of precision machining for small volume orders even with CNC machining substantially drives the cost of manufacturing, the making of cavities-holes, drilling and tapping is expensive in any shop, by almost any means.

The component value(s) realization of various filters having Pseudo(Quasi) 1/ Elliptic, (Inverse Chebishev), all-pole Chebishev, Butterworth, Gaussian, Bessel and other response shapes to satisfy a given set of specifications is not terribly difficult. One can, with a digital computer, design rather complex devices in seconds - the precision machining and assembly processes may take hours. If one must "design in" self equalization 1/and/or near band edge traps by means of non-adjacent resonator coupling, etc., the machine assembly/adjustment times may expand astronomically and will usually require very astute technicians for their adjustment.

This paper suggests designs* that have been realized in round, hollow, right circular cylindrical ground-plane housings that have been manufactured in substantial quantities, that yield superior time and frequency responses. Cavities-holes are expensive, unless one buys them ready-made, as is the case with the seemingly infinite variety of commercially available tubing: round, rectangular or of almost any shape, size, wall thickness, material, etc. that are easily made by casting, drawing or extruding and perhaps by other means.

The round-tube ground plane housing is easily punched, drilled, tapped, plated, painted, etc., and it provides degrees of freedom for a wide variety of resonator shapes: posts, helically coiled of many shapes, annular ring-like (uniform transmission line, semi-microstrip-line) (Fig.1),

*Patent(s) Applied For

1/J. D. Rhodes, "Theory of Electrical Filters" Chapter 7, John Wiley & Sons ISBN: 0 471 71806 8

which may be simply arrayed in comb-line, interdigital, or, because of the round element mounting (ground) plane one may angularly rotate (Fig. 2D) the elements up to ± 180° (Θ plane) or tilt them (Ψ plane)-(yaw-Z axis) or rotate annular inductors in the ± φ plane. One may also simply add fixed or adjustable decoupling elements and/or design for very wide tuning ranges, e.g., narrow band designed for up to 7% dB BW, or more, that may be simply adjusted over 2:1, 3:1, or, 5:1 tuning ranges. Many such devices have been designed and constructed. In the case of helical coils, pitch and winding sense may also be a design variable.

By proper design of coupling structures and general parts layout, one may obtain nearly constant percentage/MHz bandwidth over very wide tuning ranges in the 1 MHz 18 GHz range of frequencies.

The possibilities literally boggle one's imagination!

All devices electronic contain nothing more than: coils (L), capacitors (C), ± resistance (± R) or the equivalents or mixes thereof, and their necessary connections by means of conduction or induction (field coupled), which are necessarily limited to L, C or R or a mix thereof as elements/equivalent elements, in passive circuitry.

Figures 1 and 2 are self-explanatory. Figure 1 shows some of the possible inductive element, physical configurations that may be used in round-tubular ground plane housings. Figure 2 shows some possible array configurations of the inductive elements that may be used in a round-tubular ground planes. Figure 3 gives details on an 8 resonator, interdigitated, annular ring inductive element bandpass filter that tunes the range 300>600 MHz, having a nominal 3 dB BW of: 1.3% @ 300 MHz, 2.5% @ 450 MHz and 3.3% @ 600 MHz, roughly linearly increasing % 3 dB BW vs. fo, as was required in the specifications.

Table 1 lists general passband responses for this device. Figure 3C and D are plots of the general passband response. Figure 3D is the plotted response obtained while sweeping the passband and from 125 MHz to 4.9 GHz. Over 80 dB of rejection was obtained for this filter on an HP N.A. 8505 sweeping to 1.3 GHz. However, the plots given were taken on an HP scaler N.A. having a noise floor of roughly -50 dBc. Figs. 3D and 3G are the filter responses with wide band sweep, as indicated. Figs. 3E and 3H are plots of the group delay responses.

TABLE 1

fo MHz	∝ fo dB	3 dB BW	±10° (MHz) LIN∅ BW	±5° (MHz) LIN∅ BW	±2.5° (MHz) LIN∅ BW	1.5:1 (MHz) VSWR BW
300	8.1*	4	4.4	3.5	2.7	2.7
600	5.4*	20	27.2	17.9	11.8	11.8

* All tests were on unplated devices of aluminum construction. Data measured on an HP 8505 vector N.A. for Table 1.

Figure 4 gives general details on a 10 resonator combline tunable bandpass filter tuning from 3 $\gtrless$ 8 GHz (the electrical performance data on the devices shown in Figures 5C through F are incomplete in that the N.A. noise floor is shown at about -60 dBc. This unit should yield an ultimate rejection of well over -100 dBc).

The tunable combline filter shown in Figure 4 has essentially a 2.5%, 3 dB BW over its entire > 3:1 tuning range: 3 > 8 GHz. No noticeable spurious returns (above approximately -60 dBc) are apparent to nearly 13.4 GHz over the entire tuning range.

If one were so inclined, one might say that this device in an evanescent mode device at the lower tuned frequencies where:

$$\frac{\text{F (min) mode}}{\text{Fo (min) tuned}} = \frac{13.4 \text{ GHz}}{2.7 \text{ GHz}} \sim 5:1$$

and a combline at the upper reaches of its tuning range where: $F \text{ mode}/f_o = \frac{13.4}{8.15} < 2:1$

Remembering, of course, that the response above 13.4 GHz is waveguide moding, and not an element caused spur response.

Figure 5 gives the general details on the rotation coupled (WS^2 /$\Theta,\Psi,\phi,$ p,) bandpass filter, in this case a 4 pole, 2 zero tunable device tuned to 92.3 MHz, spacing, sense, and judicious use of partial electric walls and an adjustable coupling capacitor between two of the elements yields exceptional time and frequency domain properties in a relatively small package weighing 4.2 ounces.

Figure 5C: Linear frequency, 2 cycle semi-log plot of: amplitude, return loss and group delay. The group delay is exceptionally flat to the 7 dB, B.W. and then rolls off monotonically, a general characteristic of linear phase filters that also have excellent time domain properties.

The additional data table: (Figure 5C) shows tabulations for the non-linear $\pm$ 1° and $\pm$ 0.5° bandwidths; the interesting features are, however, the exceptionally deep notches: 110-112 dBc, and the pulse response, which was traced from an oscilloscope photograph; the apparent time sidelobe (note: looks more like it may have been caused by a load mismatch since it is devoid of normal zero-axes crossings which are typical of the "ringing effect") is on the order of -33 dBc, which incidentally is the return loss minima value measured at fo. See Return Loss Plot (Figure 5C)

Conclusions: The physical realization of parallel coupled-tubular-like, combline, interdigital filters and the use of angularly variable coupling means Θ, Ψ and ϕ angle rotated elements for controlled coupling/decoupling have been described for a variety of inductive element

configurations that are easily incorporated into moderately narrow band tunable bandpass filters. Because tunability was of prime consideration in these designs, wide bandwidth > 5% BW 3dB was not considered. However, much wider bandwidths are practical with many of these structures, depending on (a) type of resonator, and (b) orientation of inductive elements, spacing, θ, Ψ, and ϕ angle relationships, etc.

Coupling or decoupling may be obtained by spacing, rotation or by the use of decoupling iris, or other means, in the form of probes, crossing wires or posts which may in turn be rotated as a design variable: Figures 5.

As an added feature, one may incorporate (a) partial walls (septums) which may be rotated as to position to provide controlled decoupling (partial electric or magnetic walls) or one may use direct or tapped L or C coupling to further enhance the range of possibilities for various response shapes in the frequency and/or time domain.

A generalized design procedure has not been presented here since the arithmetic is rather cumbersome and to some extent proprietary; also, patent protection has been sought on the general design of all of these devices.

(conclusions continued on page 8)

(conclusions continued)

References:
(1) J. D. Rhodes, "Theory of Electrical Filters" Chap. 7, John Wiley & Sons ISBN: 0 471 71806 8

(2) Patent application filed with patent attorneys Kirschstein, Kirschstein, Ottinger & Israel, New York, NY: R. A. Wainwright, Inventor

(3) G. L. Mattaei, L. Young, E. M. T. Jones, "Microwave Filters, Impedance-Matching Networks and Coupling Structures" Chapters 5-8, McGraw Hill Book Co. Copyright 1964, Library of Congress Catalog Card No. 64-7937

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Ronald B. Alexander, Esq., Board Chairman; Douglas H. Alexander, President; Hilda A. Wainwright, Vice President & Corporate Treasurer; Ann McCauley, Exec. Sec., Norman Selinger, Sales Manager; Joan King and Jay Kociol for proofreading and helpful hints; Dorothy DeWitt, my secretary for her hard work, patience and understanding, and to all of the fine people at Griffith & Coe Advertising, Inc. of Hagerstown, Maryland for their expert artwork.

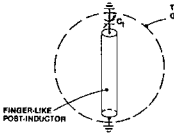

FIG. 1A

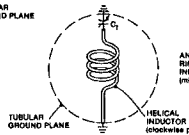

FIG. 1B1

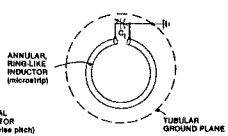

FIG. 1C

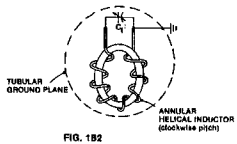

FIG. 1B2

FIG. 1 SOME OF THE POSSIBLE INDUCTIVE ELEMENT PHYSICAL CONFIGURATIONS THAT MAY BE USED IN A ROUND-TUBULAR GROUND PLANE HOUSING.

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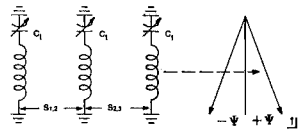

FIG. 2A1: HELICAL COMBLINE
NOTE: Pitch and Sense is also a considered variable as well as Helix Diameter and S: Spacing

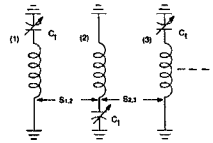

FIG. 2A2: HELICAL, INTERDIGITATED
(See Note: FIG. 2A1)

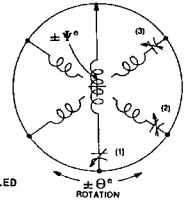

FIG. 2A3
HELICAL, ROTATION COUPLED

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SOME POSSIBLE TYPES OF INDUCTIVE ELEMENT ARRAYS THAT MAY BE USED IN A ROUND TUBULAR GROUND PLANE: Θ and Ψ ROTATION FOR FIGS. 2A & 2B AND Θ, Ψ AND ϕ FOR ANNULAR RING, TOROIDAL HELIX RING: REF. 2B2: TO THESE MAY BE ADDED VARIOUS COUPLING STRUCTURES FOR ADDITIVE/SUBTRACTIVE INTERFERENCE 1] Angle Ψ applies to all Figure 2 drawings.

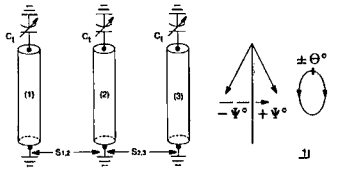

FIG. 2B1: POST/FINGER COMBLINE

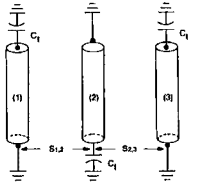

FIG. 2B2: POST/FINGER, INTERDIGITATED

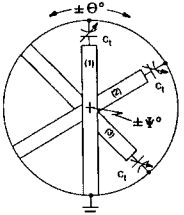

FIG. 2B3: POST-ROTATION COUPLED

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SOME POSSIBLE TYPES OF INDUCTIVE ELEMENT ARRAYS THAT MAY BE USED IN A ROUND TUBULAR GROUND PLANE: Θ and Ψ ROTATION FOR FIGS. 2A & 2B AND Θ, Ψ AND ϕ FOR ANNULAR RING, TOROIDAL HELIX RING: REF. 2B2: TO THESE MAY BE ADDED VARIOUS COUPLING STRUCTURES FOR ADDITIVE/SUBTRACTIVE INTERFERENCE 1/ Angle Ψ applies to all Figure 2 drawings.

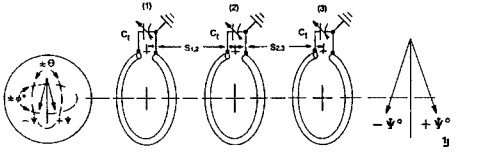

FIG. 2C1: ANNULAR RING, COMBLINE

NOTE: Rings have an added degree of freedom in $\pm\phi°$ rotation angle

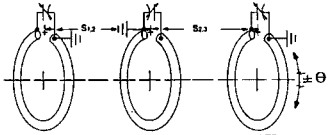

FIG. 2C2: ANNULAR RING - INTERDIGITATED

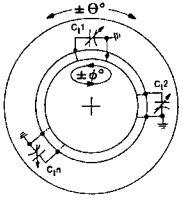

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FIG. 2C3: ANNULAR RING, ROTATION COUPLED

NOTE: The Helical Ring Toroidal Inductor Array is left to the imagination of the reader, Ref. FIG. 1B2

SOME POSSIBLE TYPES OF INDUCTIVE ELEMENT ARRAYS THAT MAY BE USED IN A ROUND TUBULAR GROUND PLANE: Θ and Ψ ROTATION FOR FIGS. 2A & 2B AND Θ, Ψ AND ϕ FOR ANNULAR RING, TOROIDAL HELIX RING: REF. 2B2: TO THESE MAY BE ADDED VARIOUS COUPLING STRUCTURES FOR ADDITIVE/SUBTRACTIVE INTERFERENCE 1/ Angle Ψ applies to all Figure 2 drawings.

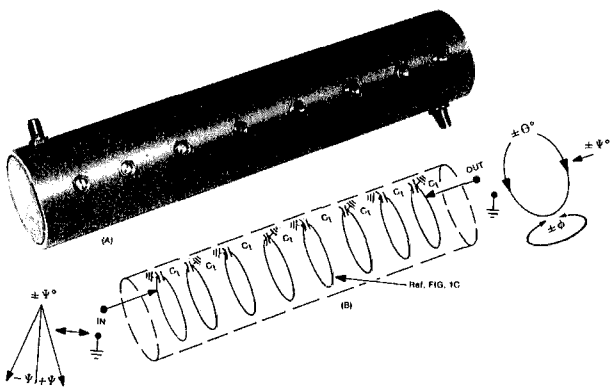

FIG. 3 A: PHOTO; B: SCHEMATIC FOR
8 RESONATOR, INTERDIGITATED ANNULAR
RING, TUNABLE BANDPASS FILTER;

RANGE = 300 > 600 MHz.

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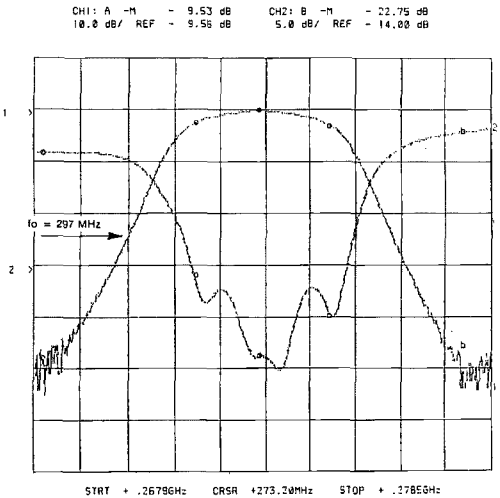

NARROW SWEEP BAND
FIG. 3C

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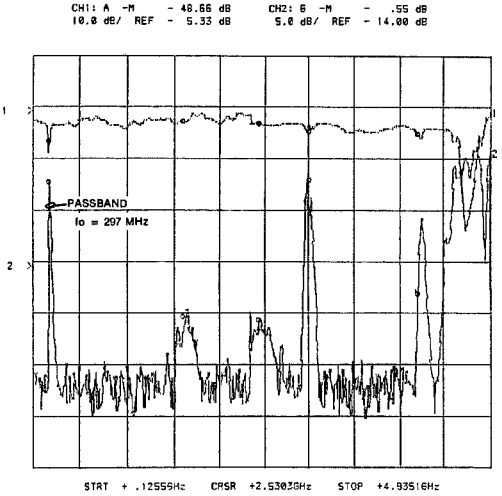

WIDE BAND SWEEP TO 14.9 GHz

FIG. 3D

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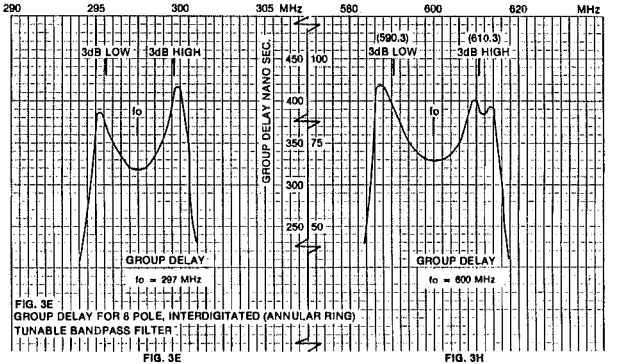

FIG. 3E
GROUP DELAY FOR 8 POLE, INTERDIGITATED (ANNULAR RING)
TUNABLE BANDPASS FILTER

FIG. 3E FIG. 3H

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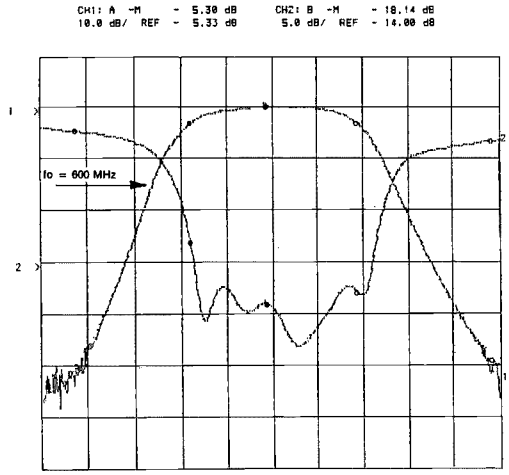

NARROW BAND SWEEP
FIG. 3F

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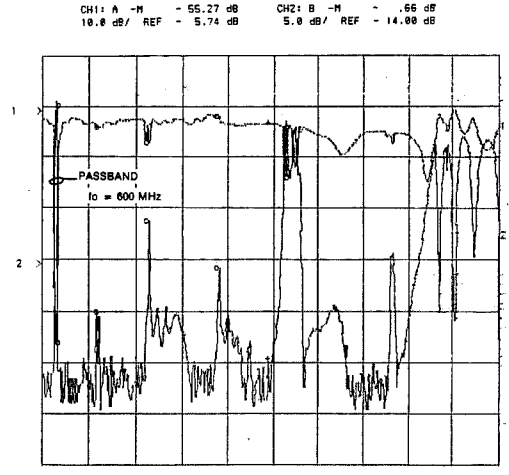

WIDE BAND SWEEP TO 14.9 GHz
FIG. 3G

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FIG. 4A

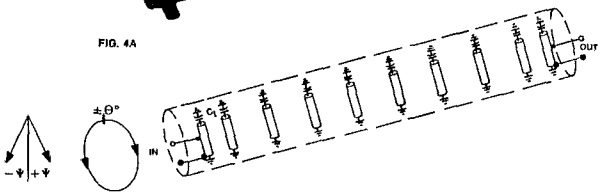

FIG. 4B

FIG. 4: A = PHOTO, B = SCHEMATIC FOR 10 RESONATOR COMBLINE (POST) BANDPASS FILTER RANGE: 3 > 8 GHz, 3dB BW : 2.5%

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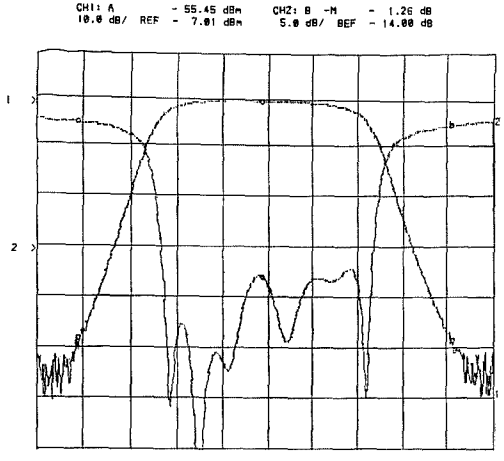

PASSBAND SWEEP, fo = 2.7 GHz

FIG. 4C

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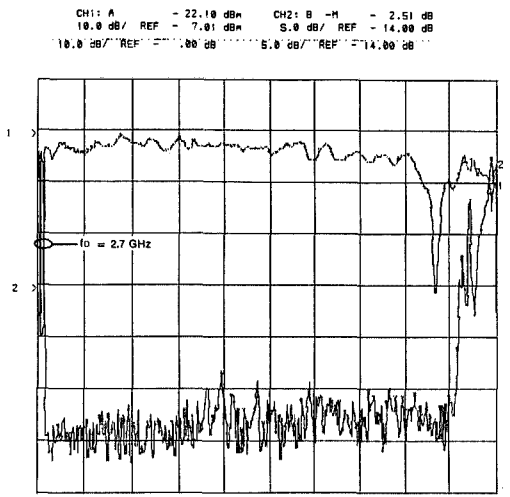

WIDE BAND SWEEP TO 14.9 GHz

FIG. 4D

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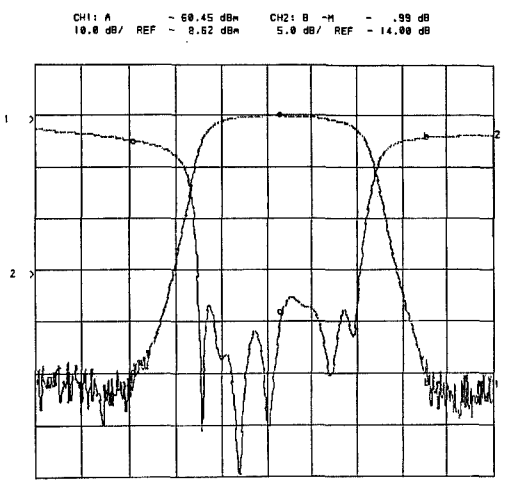

PASSBAND SWEEP fo = 8.15 GHz

FIG. 4E

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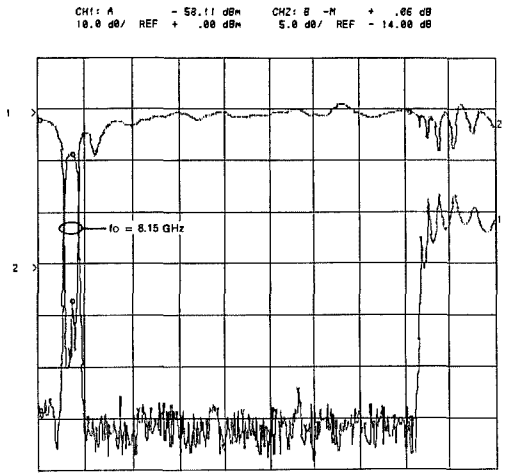

WIDE BAND SWEEP TO 14.9 GHz

FIG. 4F

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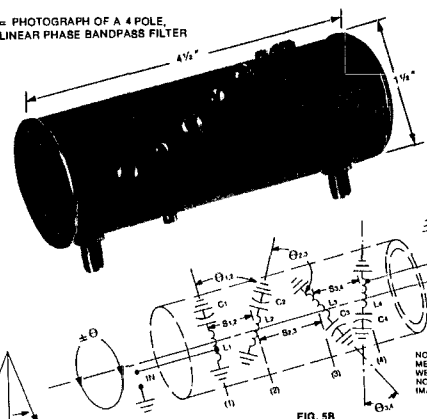
FIG. 5A = PHOTOGRAPH OF A 4 POLE, 2 ZERO LINEAR PHASE BANDPASS FILTER



$K_{1,2,3}$ COMPLEX COUPLING COEFFICIENT FROM RESONATORS (1) TO (2) TO (3) TO (4) MAY BE MODIFIED BY THE MUTUAL COUPLING FROM RESONATOR (1)-(3) AND THE INTRODUCTION OF COUPLING ENHANCEMENT AND/OR DECOUPLING ELEMENTS ETC.

NOT SHOWN ARE COUPLING ENHANCEMENT/DECOUPLING ELEMENTS WHICH WERE USED TO TRIM ATTENUATION NOTCHES AND PROVIDE NEARLY MAXIMALLY FLAT TIME DELAY, SEE FIG. 5C.

FIG. 5B

FIG. 5B SCHEMATIC CONCEPT OF A 4-(W-S[1] / Θ, Ψ, ϕ, P) TUNABLE BANDPASS FILTER
S = SPACING; S_{ij}: WINDING SENSE (HELICAL COILS): $S_{1,2}$, $S_{2,3}$: (CW, CCW)
$\pm\Theta_{i,i+1}$: ROTATION ANGLE BETWEEN ADJACENT INDUCTORS
$\pm\Psi_{i,i+1}$: YAW ANGLE FROM NORMAL MAJOR z AXIS OF ADJACENT ELEMENTS
$\pm\phi_{i,i+1}$: TWIST ANGLE (ANNULAR INDUCTORS) BETWEEN ADJACENT ELEMENTS
P: PITCH OF WINDINGS

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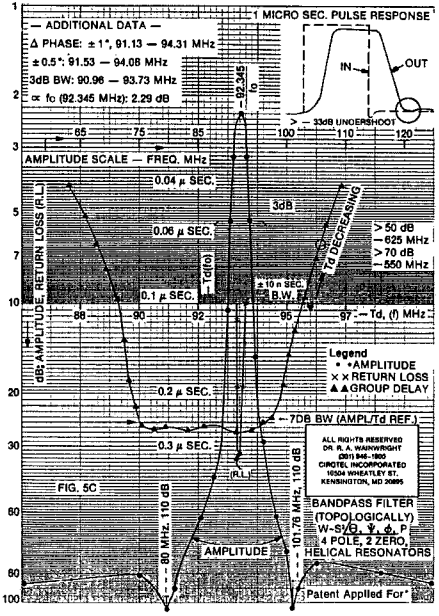
PATENT APPLIED FOR


— ADDITIONAL DATA —
Δ PHASE: ±1°, 91.13 — 94.31 MHz
±0.5°: 91.53 — 94.08 MHz
3dB BW: 90.96 — 93.73 MHz
∝ fo (92.345 MHz): 2.29 dB
1 MICRO SEC. PULSE RESPONSE
IN
OUT
33dB UNDERSHOOT
92.345 fo
AMPLITUDE SCALE — FREQ. MHz
AMPLITUDE RETURN LOSS (R.L.)
0.04 μ SEC.
0.06 μ SEC.
0.1 μ SEC.
0.2 μ SEC.
0.3 μ SEC.
3dB
Td DECREASING
> 50 dB — 525 MHz
> 70 dB — 550 MHz
Td(fo)
± 10 n SEC. B.W.
Td, (f) MHz
dB AMPLITUDE
Legend
• •AMPLITUDE
× ×RETURN LOSS
▲▲GROUP DELAY
7DB BW (AMPL/Td REF.)
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(301) 946-1800
CIROTEL INCORPORATED
10304 WHEATLEY ST.
KENSINGTON, MD 20895
FIG. 5C
(R.L.)
80 MHz, 110 dB
101.76 MHz, 110 dB
AMPLITUDE
BANDPASS FILTER
(TOPOLOGICALLY)
W-SYΘ, Ψ, ϕ, P
4 POLE, 2 ZERO,
HELICAL RESONATORS
Patent Applied For*

The PIN Diode - Uses and Limitations

by
Jack H. Lepoff
Applications Engineer
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ABSTRACT

The PIN diode is a useful element in the design of attenuators, switches, and modulators. Under ideal conditions the diode acts as a current controlled resistor. However, there are limitations on performance related to frequency and power.

This paper covers some of the low frequency and high frequency limitations of PIN diode applications and factors determining these limits. Other topics are diode parameters that control resistance and power limitations on attenuator performance.

INTRODUCTION

The PIN diode is a three layer device (figure 1) - an intrinsic high resistance I layer in the center with conducting P and N layers on either side. The conducting layers are formed by adding impurities to produce an excess of positive charges on one side and an excess of negative charges on the other. Diode resistance can be controlled by DC bias voltage. Both positive and negative charges injected into the I layer lower its resistance. Diode resistance is approximately proportional to the inverse of the current.

Ideally PIN diode resistance is controlled by the DC current and independent of the RF power level. However, at high power levels the charge in the I layer may vary at the carrier frequency. In attenuator applications this variation in diode resistance is responsible for distortion. The effect is most severe in absorptive attenuators at low frequencies, with some power also absorbed by diodes in reflective attenuators. Since the amount absorbed depends on the attenuation level, distortion in both types is a function of attenuation.

Most switches are reflective; power is either reflected or passed. Little power is absorbed by the diode so distortion in switches is not a problem. PIN diodes can have a wide range of switching times - from a few nanoseconds to close to a microsecond. The time depends on the combination of forward current for one state and reverse voltage for the other. Switching time is faster in the transition from reverse to forward bias.

Reverse recovery time is related to switching time. Forward current injects charge into the diode, then a reverse pulse removes the charge. Time for recovery to a low value of current is defined as reverse recovery time, and depends on the values of forward current and reverse voltage used in the measurement.

In addition to switches and attenuators, PIN diodes can be used as absorptive modulators. The diode resistance is varied at the modulating

frequency while passing a higher carrier frequency. The ability to modulate diode resistance is limited by the diode carrier lifetime, the time required to remove charges from the I layer. For efficient modulation the lifetime must be short compared to the modulation period, while low distortion requires the lifetime to be long compared to the carrier period. When these two frequencies are not far apart it may not be possible to satisfy both conditions, and a compromise value of lifetime is chosen.

Figure 2 shows the frequency limitations for diodes with lifetimes ranging from 10 nanoseconds to 2 microseconds. The fast switching diodes are best with carrier frequencies above a gigahertz and modulation frequencies below 100 kilohertz. The long lifetime diodes are best with carrier frequency above 10 megahertz and modulation frequency below 1 kilohertz. However, these limits are not rigid and diodes are useful beyond these limits.

In addition to the inverse current relation, I layer resistance varies as the square of the I layer thickness and Inversely as the lifetime. However, the lifetime is itself a function of I layer thickness so that a longer lifetime diode has more resistance in spite of this inverse relationship. Figure 4 shows that the 5082-3081 diode with 2 microseconds lifetime has 30 times the resistance of the 5082-3043 diode with 15 ns lifetime. Another example of resistance dependence on lifetime is seen in Figure 5. These diodes are in shunt so higher attenuation means lower resistance. The short lifetime 3141 has lower resistance because it has a thinner I layer.

The relation between resistance and current is not valid at high currents. The resistance levels off at a current which depends on the diode construction. This residual series resistance is usually guaranteed to be below a specified maximum.

Attenuator designers often need more information about the resistance current relationship. The specifications for current controlled resistor diodes such as the HPND-4165 shown in Figure 6 include maximum and minimum resistance values at 10 microamperes and at 1 milliampere. In addition, the slope of the curve, the exponent of current, must be matched to 0.04 for all diodes in a batch. Since the slope, x, can vary from 0.83 to 1.00 while satisying the resistance specs, this delta slope spec tightens the matching considerably.

A low frequency limitation of the PIN diode is the dielectric relaxation frequency. When current is removed from the diode most of the charges return to the p and n layers. However, some charges remain in the underpleted portion of the I layer. At low frequencies this undepleted I layer resistance shorts out the I layer capacitance. A capacitance measurement would be high because only a portion of the I layer, the depleted portion, would be measured. Capacitance measurements at low frequencies (1MHz) require the use of reverse bias to drive out the

charges in the undepleted I layer in order to measure the capacitance of the entire I layer. At higher frequencies the reactance of the undepleted I layer is small and the resistance of the undeplete charges is not small enough to cause this capacitance error, so no reverse bias is needed.

The dielectric relaxation frequency is the frequency where the resistance of the undepleted charges equals the reactance of the undepleted I layer. This frequency is about 80 MHz for general purpose diodes, about 16 GHz for the fast switching diodes. When operating below the dielectric relaxation frequency it is necessary to use reverse bias to reach the specified capacitance. Since reverse bias is normally used in switching applications to speed up the switching, the concept is not important for fast switching diodes.

We have seen two possible problems at low frequency. The resistance can vary at the carrier frequency and the capacitance can vary with reverse voltage. There is also a high frequency limitation. At zero bias we expect the diode to approximate an open circuit. This is true at low frequencies when the capacitive reactance is high. At higher frequencies the reactance decreases and the insertion loss of a shunt diode increases, related to the product of frequency and capacitance. Figure 8 shows how insertion loss varies. When this product is 3.2 for example, the loss is 1 dB.

Figure 9 indicates a technique for extending this frequency limitation. The diode capacitance may be included in a low pass filter with the lead inductances on either side of the diode. Package outline 60 and 61 diodes are made this way. The ribbons to the diode chip are properly shaped to provide the needed inductance. When chips are placed in other packages the limitations due to package parasitics appear at frequencies well below what is shown in Figure 8. Before the insertion loss increases because of low diode reactance, the package inductance resonates with the diode capacitance. Figure 11 shows this resonance for a 0.12 pF diode in packages 15 and 31 at 9.2 GHz and 14.5 GHz. Insertion loss due to diode capacitance alone at these frequencies is about 0.1 dB.

Figure 12 shows the problem at forward bias. The package parasitics resonate with each other changing the low resistance Rs to an open circuit. Similar problems limit the performance of series diodes to the VHF region. Figure 13 shows that isolation drops below 20 dB at a few hundred MHz. Chip isolation was calculated with 0.5 nH assumed for the lead inductance. The graph demonstrates that microwave applications for series diodes require the use of beam leads.

Isolation in a shunt switch is limited by the diode series resistance. Using two diodes together cuts the resistance in half and improves isolation 6 dB. Figure 14 shows the results of using two diodes spaced by 90 degrees. The dB isolation more than doubles, and the bandwidth is quite wide, exceeding 50 dB isolation for about a 10:1

frequency range. It might be expected that this two-diode switch would double the power handling ability, but there is no improvement. The second diode absorbs very little power and does not contribute to the power specification (Figure 15).

With 1 ohm resistance a shunt diode absorbs less than 10% of the incident power. In this application the incident power can be 10 times the power rating of the diode. In attenuator applications the multiplier is only two, corresponding to 6 dB of attenuation. Figure 16 shows this ratio as a function of attenuation. Switches can handle many times the diode power rating, since the loss switches from low insertion loss to high isolation. However, this assumes that switching time is fast compared to diode thermal time constant.

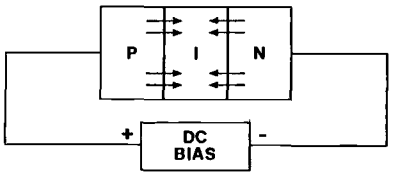
Both shunt and series diodes attenuate by reflecting most of the incident power. In many applications this reflected power disturbs the operation of another element of the system. Figure 17 shows a number of attenuator designs that maintain a low value of SWR at all attenuation levels. The π and T attenuators are symmetrical with the outer diodes set at the same resistance, but the inner diode set at a different value. Bias circuits may be built with "one knob" tuning providing the proper bias current to all three diodes.(1)

The ideal behavior of attenuation controlled by current, independent of RF power, is not valid at high power levels, due to rectification of the RF signal. Figure 18 shows how low level attenuation is increased at 1.6 watts, with the effect most severe at 3 dB attenuation. Rectification is easier with short lifetime diodes so the 5082-3141 curve is higher. Rectification is also easier at lower frequencies so we would see VHF curves above these. Bias resistance was zero for this data.

Since this increase in attenuation is due to rectified current we expect a reduced effect when bias resistance is increased. This is shown in Figure 19 where the effect is not seen until the power reaches a half watt with bias resistance increased to 100 kilohms. Above that level the opposite effect is seen. Attenuation decreases at higher power indicating an increase of diode resistance. This increase of resistance is the result of diode heating. In this example rectified current is small so the diode heating effect is dominant.

(1) Hewlett-Packard Application Note 936, High Performance PIN Attenuator For Low Cost AGC Application.

THE PIN DIODE



Q ∝ DC BIAS CURRENT

G ∝ Q

$$R = \frac{1}{G}$$

FIGURE 1

I LAYER RESISTANCE

$$R \propto \frac{W^2}{I\tau}$$

W IS I LAYER THICKNESS

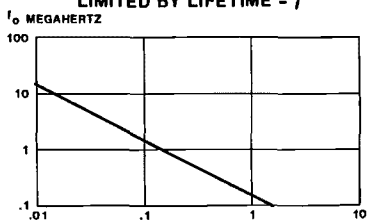
BUT LIFETIME IS LONG WHEN I LAYER IS THICK

USUALLY W^2 OVERCOMES τ EFFECT
SO FOR SAME CURRENT LONG LIFETIME DIODE HAS
HIGHER RESISTANCE THAN
SHORT LIFETIME DIODE

FIGURE 3

MODULATOR FREQUENCY LIMITATIONS

FREQUENCY PERFORMANCE LIMITED BY LIFETIME - τ

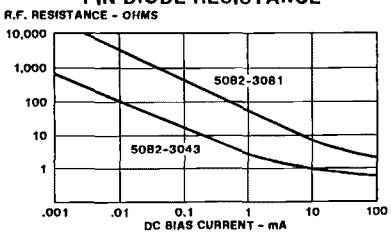


$$f_o = \frac{1}{2\pi\tau}$$

$$100\, f_m < f_o < .01 f_c$$

FIGURE 2

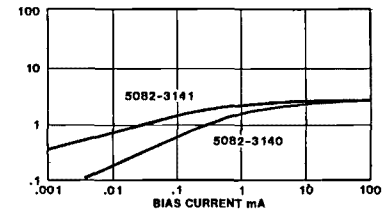
PIN DIODE RESISTANCE



DIODE 3081 HAS LONG LIFETIME 2μs
DIODE 3043 HAS SHORT LIFETIME 15ns

FIGURE 4

MATCHED ATTENUATOR



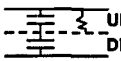
ATTENUATION = 20 LOG $(1 + \frac{25}{R})$

$R \propto \frac{W^2}{IT}$

FOR SAME CURRENT, HIGHER ATTENUATION FOR THINNER I LAYER NOT FOR LONGER LIFETIME.

FIGURE 5

DIELECTRIC RELAXATION FREQUENCY



AT LOW FREQUENCIES UNDEPLETED I LAYER RESISTANCE SHUNTS CAPACITANCE SO TOTAL CAPACITANCE IS HIGHER

$$R = \frac{1}{2\pi f_{DR} C}$$

FOR EXAMPLE:

$$R = \frac{\rho d}{A} \qquad C = \frac{\varepsilon A}{d}$$

for $\varepsilon = 10^{-12}$

$$f_{DR} = \frac{1}{2\pi\rho\varepsilon}$$

IF $\rho = 2000$, then $f_{DR} = 80$ MHz

or, IF $\rho = 10$, then $f_{DR} = 16$ GHz

FIGURE 7

CURRENT CONTROLLED RESISTORS

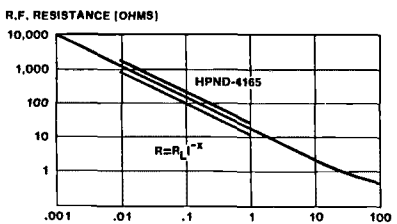


FIGURE 6

SHUNT DIODE INSERTION LOSS

10 LOG $\left[1+\left(\frac{\pi FC}{20}\right)^2\right]$

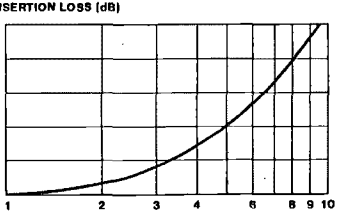
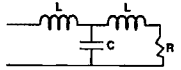


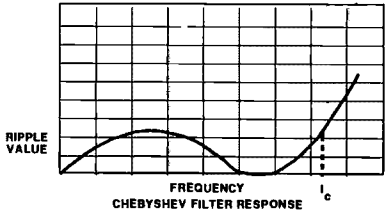
FIGURE 8

EXTENSION OF HIGH FREQUENCY LIMITATIONS

SOLUTION



LOW PASS FILTER WITH DIODE AS SHUNT CAPACITOR

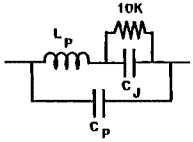


CHEBYSHEV FILTER RESPONSE
APPLICATION NOTE 957-2

FIGURE 9

FIGURE 10

PACKAGE LIMITATIONS



REVERSE OR ZERO BIAS

AT L_p C_J RESONANCE - LOW ISOLATION FOR SERIES DIODE - HIGH INSERTION LOSS FOR SHUNT DIODE; AT SECOND RESONANCE WITH C_p - GOOD PERFORMANCE

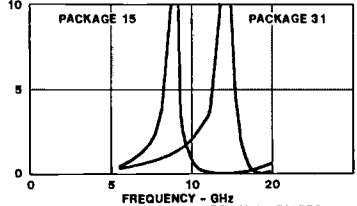
PKG.	15	31
C_p PF	.13	0.2
L_p nH	2.5	1.0

PACKAGE LIMITATIONS

HIGH INSERTION LOSS AT FIRST RESONANCE

$$F_{RES} = \frac{1}{2\pi\sqrt{L_p C_J}}$$

LOW INSERTION LOSS AT SECOND RESONANCE WITH PACKAGE CAPACITANCE

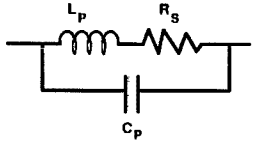


INSERTION LOSS OF PACKAGED SHUNT DIODES
.12 pF JUNCTION CAPACITANCE

FIGURE 11

FIGURE 12

PACKAGE LIMITATIONS

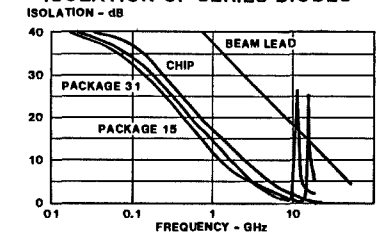


FORWARD BIAS

AT RESONANCE - HIGH INSERTION LOSS FOR SERIES DIODE - LOW ISOLATION FOR SHUNT DIODE

THIS PROPERTY IS USEFUL IN NARROW BAND WAVEGUIDE SWITCHES

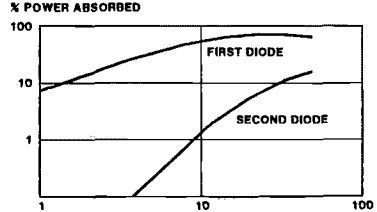
ISOLATION OF SERIES DIODES



0.12 pP JUNCTION CAPACITANCE FOR CHIP AND PACKAGED UNITS
0.02 pF BEAM LEAD DIODE CAPACITANCE
PACKAGE 1S RESONATES FIRST BECAUSE Lp LARGER
PACKAGE 31 WORSE BELOW RESONANCE BECAUSE Cp LARGER

FIGURE 13

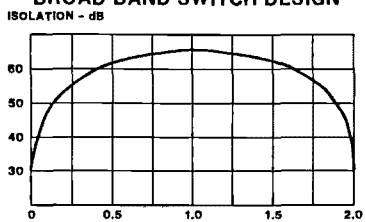
ABSORBED POWER DIVISION IN QUARTER WAVE PAIR



SECOND DIODE DOES NOT IMPROVE ABILITY TO HANDLE HIGH POWER

FIGURE 15

BROAD BAND SWITCH DESIGN



QUARTER WAVE PAIR
ONE OHM DIODES

ISOLATION MORE THAN DOUBLE SINGLE DIODE

FIGURE 14

RATIO OF INCIDENT POWER TO ABSORBED POWER

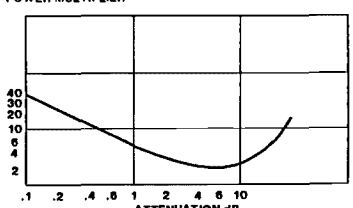


FIGURE 16

ABSORPTIVE ATTENUATORS

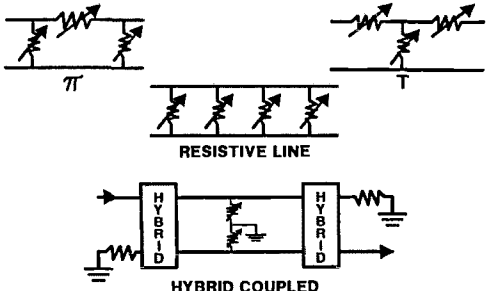
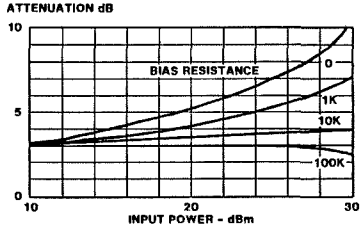


FIGURE 17

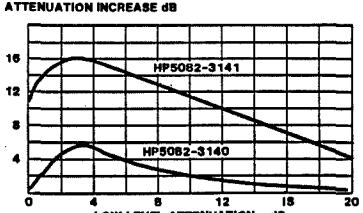
POWER SENSITIVITY IN A 3 dB PIN ATTENUATOR



FREQUENCY 10 GHz
DIODE HP5082-3141
REVERSE EFFECT AT HIGH VALUE OF BIAS RESISTANCE DUE TO TEMPERATURE EFFECTS.

FIGURE 19

POWER SENSITIVITY AT +32 dBm INPUT



DATA TAKEN AT 2 GHz ZERO OHMS BIAS RESISTANCE
THE INCREASE IS LESS AT HIGHER FREQUENCIES
THE INCREASE IS LESS FOR THE DIODE WITH LONGER LIFETIME (3140)
SEE AN 967-3

FIGURE 18

RF AND MICROWAVE TRANSISTOR BIAS CONSIDERATIONS

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INTRODUCTION

The purpose of this paper is to present an overview of the advantages and disadvantages of some common bias circuits. Resistive, diode, and active bias circuits will be examined and compared as to how well they stabilize the transistor bias point against DC parameter changes caused by temperature and device-to-device variations.

BIAS POINT STABILITY

Before examining the bias circuits, let's look at some of the reasons for being concerned about bias stability. Figure 1a shows a transistor biased for Class A operation which is not stabilized against DC parameter changes. Increasing temperature shifts the bias point further to saturation (Figure 1b), while decreasing temperature shifts the bias point closer to cutoff (Figure 1c). Temperature extremes caused the transistor's DC parameters to change which resulted in the shift of the bias point. In the above example the shift in the bias point was large enough to cause unwanted distortion in the output signal. Figure 2a and 2b show that both gain and noise figure of a bipolar transistor are also a function of the collector current.

Bias point shifts caused by temperature are not the only concern. The DC parameters also change due to device-to-device variations . The DC current gain of microwave bipolar transistors can vary over a range of 5:1 and still be within the manufacturer's electrical specification at 25 degrees C. This means that a shift in the bias point can be caused by temperature and device-to-device variations. Obviously , a bias circuit that can minimize these bias point shifts is desirable. The first step in understanding how to stabilize the bias point is to identify the DC parameters which affect the bias point the most and how these parameters respond to temperature variations.

TEMPERATURE SENSITIVE DC PARAMETERS

The principal dependent variable in DC stability analysis is the collector current (I_C)[1,2]. The following DC parameters, which are shown in the equivalent circuit of Figure 3 , are temperature sensitive and directly influence the collector current.

Base to Emitter Voltage (V_{BE}):

V_{BE} is internal to the transistor and has a negative temperature coefficient of 2 mV/degree C. Figure 4 shows the temperature characteristic of this parameter.

Reverse Collector Current (I_{CBO}):

I_{CBO} is the current flowing through the reversed biased PN

junction of the collector to base. Classically, this leakage current is expected to double for every 10 degrees C temperature rise in a silicon semiconductor junction. The leakage current for silicon is so low that under most conditions this parameter can be negected.

DC Current Gain (h_{FE}):

The h_{FE} of a transistor is defined as the ratio of the collector current to the base current. This parameter typically increases linearly with temperature at the rate of 0.5 % /degree C.

STABILITY FACTORS

Before we proceed to examine the bias circuits, it is useful to introduce the concept of stability factors. The stabiliy factors are defined as the ratio of the incremental change of I_C vs the incremental change of each of the three components I_{CBO}, V_{BE}', and h_{FE}. The stability factor equations are given below.

I_{CBO} STABILITY FACTOR

$$S_{ICBO} = \frac{\partial I_C}{\partial I_{CBO}} \Big|_{h_{FE}, V_{BE}' = \text{constant}}$$

V_{BE}' STABILITY FACTOR

$$S_{VBE'} = \frac{\partial I_C}{\partial V_{BE}'} \Big|_{h_{FE}, I_{CBO} = \text{constant}}$$

h_{FE} STABILITY FACTOR

$$S_{hFE} = \frac{\partial I_C}{\partial h_{FE}} \Big|_{I_{CBO}, V_{BE}' = \text{constant}}$$

The total change in collector current can be expressed as the sum of each incremental change caused by I_{CBO}, V_{BE}', and h_{FE}.

$$\Delta I_C = S_{ICBO}\,\Delta I_{CBO} + S_{VBE'}\,\Delta V_{BE'} + S_{hFE}\,\Delta h_{FE}$$

Unfortunately, the stability equations can become very complicated even for a simple bias circuit such as the one shown in Figure 5. The equation of Figure 5 can be easily digested by a computer, but it doesn't help the designer gain any insight into selecting component values or in making circuit comparisons. Fortunately, the following approximations can help simplify the stability equations:

* Neglect I_{CBO} when using silicon transistors. As previously stated, the leakage current for silicon is typically so low that neglecting I_{CBO} will have negligible effect on the accuracy of the stability equations.

* Drop the hie term, which is the hybrid-pi input impedance for common emitter configuration. The external biasing resistance is usually much greater than hie, and neglecting the hie term will not upset the accuracy of the equations.

* Assume that $h_{FE} \gg 1$ then ($h_{FE} + 1$) simplifies to h_{FE}.

The stability factor S_{hFE} can be expressed as a percentage change in I_C vs a percentage change in h_{FE}[3] . The new variable is defined as K_{hFE} . The same procedure is used to define K_{VBE}

$$K_{hFE} = \frac{\Delta I_C / I_C}{\Delta h_{FE} / h_{FE}} = \frac{S_{hFE}}{I_B}$$

$$K_{VBE'} = \frac{\Delta I_C / I_C}{\Delta V_{BE'} / V_{BE'}} = -\frac{V_{BE'}}{I_C} S_{VBE'}$$

The stability equations for the previous example (Figure 5) now simplify to the following:

$$K_{hFE} = \frac{1}{(1 + \frac{hFE\ RC}{R_B})}$$

$$K_{VBE'} = \frac{1}{(1 - \frac{VCC}{V_{BE'}})}$$

The simplified stability factors are easier to handle and it is now apparent that increasing the R_C / R_B ratio will decrease K_{hFE} and improve collector current stability against h_{FE} changes. We now have the tools to examine the bias circuits.

RESISTIVE BIAS CIRCUITS

* Fixed Bias

The fixed bias circuit shown in Figure 6, is the simplest and one of the worst methods of biasing a transistor because it has a very high sensitivity to h_{FE} variations. Notice that K_{hFE} is unity, which means that a 20 % change in h_{FE} will result in a 20 % change in collector current. Since h_{FE} can vary by as much as 5:1 from device to device, the transistor could be at cutoff with one device and at saturation with another. The base current, which is fixed by the voltage difference between the supply voltage and $V_{BE'}$, is the cause of the poor bias stability. If the base current were made to decrease with increasing h_{FE} and increase with decreasing h_{FE} the bias stability would improve greatly, which exactly describes the operation of the next circuit.

* Voltage Feedback Bias

The voltage feedback bias circuit shown in Figure 7 improves bias stability by allowing the base current to respond to changes in the collector current. If the collector current increases, the voltage drop across R_C increases which results in a lower collector to emitter voltage (V_{CE}). Since the base current is set by the resistor R_B and the voltage difference of V_{CE} and $V_{BE'}$, a lower V_{CE} decreases the base current which stabilizes I_C to a current closer to the quiescent bias point. The circuit will handle a decrease in I_C in a similar manner.

A circuit designed with I_C = 10 ma, V_{CE}= 10 V, V_{CC}= 12 V, h_{FE}= 50 results in K_{hFE}= 0.826. This means that the collector current will change by 82.6 % of the change in h_{FE} as compared to the 100 % change that would be expected from the fixed bias circuit. This is approximately a 17 % improvement over the fixed bias circuit for this set of conditions. The K_{hFE} stability factor shows that increasing the R_C / R_B ratio decreases the sensitivity of I_C to h_{FE} changes. A small value of R_B improves the h_{FE} stability, but it isn't alway easy to get a small value of R_B. A smaller effective value of R_B is possible using the

emitter resistor feedback circuit.

* Voltage Feedback and Constant Base Current Source

The circuit of Figure 8 can be considered to have a constant base current source, formed by the resistor network of R_B, R_{B1} and R_{B2}. The collector current can be made relatively stable if I_{BB} is chosen to be much greater than the transistor base current I_B. A good choice, somewhat arbitrary , is to pick $I_{BB} = 5I_B$ to $10I_B$. A value greater than $10I_B$ gives little improvement in stability.

* Emitter Resistor Feedback

The bias circuit of Figure 9 is one of the best methods of biasing a transistor. The circuit operates in the following manner. When the collector current and therefore the emitter current increases, the voltage drop across R_E increases. The polarity of this voltage opposes the forward bias voltage between base-to-emitter. The reduced V_{BE} decreases I_B and therefore I_C, which stabilizes the collector current closer to its initial value. The stability factor(K_{hFE}) for this circuit is 0.169 when calculated using the design values previously given for the voltage feedback circuit, and $I_{BB} = 5I_B$. A $K_{hFE} = 0.169$ represents a considerable improvement in stability over the previous circuits.

The V_{BE} stability factor for this circuit is:

$$S_{VBE} = \frac{-1}{R_E} \quad (\text{assuming } R_E >> \frac{R_B}{h_{FE}})$$

This equation implies that, the larger the R_E, the better the stability against V_{BE} variations. There is a limit to the size R_E can be, since the voltage drop across R_E will become excessive. The next circuit examined (diode temperature compensation) presents a method of stabilizing against V_{BE} temperature variations without resorting to large R_E values.

The emitter resistor feedback circuit does require special RF considerations which are covered in detail later in this paper.

* Diode Temperature Compensation

The emitter-base voltage has a negative temperature dependence of about 2 mv/ degree C, which can be compensated by introducing diodes into the voltage divider network as shown in Figure 10[4,5].

The calculated stability factor for this circuit is $S_{VBE} = 1/ 5.65R_E$, which is a 5.65 times improvement over the emitter feedback circuit of Figure 9. The above calculation was made with the design values from the voltage feedback example, and assumed compensation was done with a single diode that had a temperature characteristic identical to the transistor emitter-base junction.

* Zener Diode Bias

The Zener diode shown in Figure 11 determines the collector

to base voltage V_{CB} of the transistor. The collector to emitter voltage V_{CE} is fixed by the sum of V_{BE} and the Zener diode voltage (V_Z). The current through R_C divides between the transistor and D_1. Temporarily ignoring the current through R_B, the only current flowing through D_1 is the base current of the transistor. Most of the current flows through the collector as I_C. If the h_{FE} is low, the current through D_1 will increase accordingly. However, if h_{FE} is high, the current through D_1 is low and the regulation as a Zener is poor. Therefore, R_B is added to the bias circuit to ensure that enough current flows through the Zener for good voltage regulation[6].

This circuit is more stable than the voltage feedback circuit, but the Zener diode is noisy and may require a large value bypass capacitor to prevent the Zener's noise from modulating the amplified RF signal.

* Active Bias Circuit

An active bias circuit is shown in Figure 12, which uses a PNP transistor (Q_2) to help stabilize the bias point of the RF transistor (Q_1). The transistor Q_2 acts as a DC feedback circuit that senses the collector current of Q_1 and adjusts Q_1's base current to hold the collector current I_{C1} constant. The circuit operates in the following manner. If I_{C1} increases, the voltage drop across R_C increases and opposes the forward bias of the PNP transistor which decreases I_{E2}. The decrease in I_{E2} causes I_{C2} and I_{B1} to decrease. The lower base current into Q_1 decreases I_{C1} which opposes the original increase in the collector current.

The collector current equation for the RF transistor is shown in Figure 12. Notice that if $(1+h_{FE1})R_C \gg R_B/(1+h_{FE2})$, then the collector current is essentially independent of the DC current gains of either of the transistors. A very detailed analysis of this circuit is available in the literature[7].

The active bias circuit has the best stability of all the circuits examined, but does require the most parts. The PNP transistor does form a feedback circuit, which must be carefully RF bypassed to prevent bias oscillations.

EMITTER RESISTOR BYPASS

The emitter resistor improves bias stability through the use of negative feedback which is desirable at DC, but not at RF frequencies. The RF gain will be reduced if the resistor is not RF bypassed. Bypassing the emitter resistor does require two special precautions to prevent possible oscillations.

First, the emitter bypass capacitor must be large enough to provide an effective RF ground at both the design frequency and lower frequencies. The Smith Chart of Figure 13 shows the effect on the transistor S-parameters when the bypass capacitor (C_E) is too small. Changes in the transistor's S_{11} and S_{22} parameters are

shown on the Smith Chart as S_{11}, and S_{22},. A good RF bypass capacitor should cause little or no effect on the S-parameters . Both S_{11} and S_{22} at 4 GHz remains unchanged after the emitter resistor and 100 pF capacitor are added, but move off the Smith Chart as the frequency decreases. Reflection coefficients greater than 1 indicate conditional stability and are likely to oscillate. A value of 1000 pF would be a much better bypass capacitor value.

The second precaution is to minimize the inductance added in the emitter caused by the resistor and capacitor parasitics. The Smith Chart of Figure 14 shows the effect of emitter inductance on the transistor's S-parameters. Inductance in the emitter can potentially cause conditional stability. In this case, a rather large value of 5 nHy was selected to illustrate the effect. At a frequency of 4 GHz S_{22}, has moved off the Smith Chart which indicates that the circuit is conditionally stable.

An effective RF bypass of the emitter resistor is a relatively straightforward procedure as long as the above precautions are taken.

SUMMARY

This paper has shown that bias stability is more a function of the bias circuit design than of the transistor's characteristics. The RF and bias circuits should be designed with equal consideration, since the RF performance of an amplifier was shown to be dependent on the bias stability.

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1. Philip Cutler," Electronic Circuit Analysis ", Vol. 2, McGraw-Hill 1967. Chapters 4-11, pp. 220-228.

2. Hewlett-Packard Application Note 944-1, "Microwave Transistor Bias Considerations"

3. Albert Malvino, "Transistor Circuit Approximations", McGraw Hill Book Company, 1968, pp. 202-234.

4. G.J Ritchie, "Transistor Circuit Techniques , Discrete and Integrated ", Van Nostrand Reinhold, 1983, pp. 82-84.

5. D. Schilling, C. Belove, " Electronic Circuits: Discrete and Integrated ", 2 nd Edition pp. 190-192.

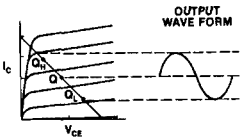
6. J.H. Reisert,Jr.," Ultra Low-Noise UHF Preamplifier", Ham Radio Magazine, pp. 8-19, March 1975.

7. Ralph Carson, " High Frequency Amplifiers ", Wiley, 1982, 2nd Edition, pp. 145-187.

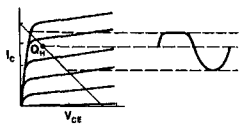
FIGURE 1

EFFECT OF TEMPERATURE ON THE BIAS POINT

A. BIAS POINT: AT 25°C



B. BIAS POINT SHIFT DUE TO INCREASING TEMPERATURE, AND DISTORTION IN *OUTPUT* WAVE FORM



C. BIAS POINT SHIFT DUE TO DECREASING TEMPERATURE, AND DISTORTION IN OUTPUT WAVE FORM

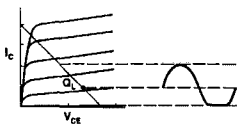
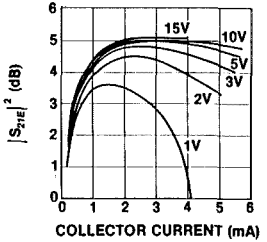


FIGURE 2

A. RF GAIN ($|S_{21}|^2$) VS. BIAS POINT



B. NOISE FIGURE VS. BIAS POINT

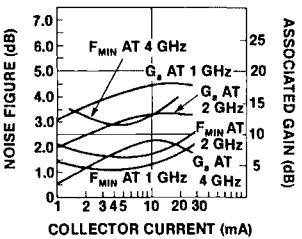

NOISE FIGURE (dB)
ASSOCIATED GAIN (dB)
F_{MIN} AT 4 GHz
G_a AT 1 GHz
G_a AT 2 GHz
F_{MIN} AT 2 GHz
G_a AT 4 GHz
F_{MIN} AT 1 GHz
1 2 3 4 5 10 20 30
COLLECTOR CURRENT (mA)

FIGURE 3

PARAMETERS THAT DOMINATE CHANGES IN I_C AND V_{CE} WHEN TEMPERATURE VARIES:

- $V_{BE'}$ (BASE TO EMITTER VOLTAGE)
- I_{CBO} (REVERSE COLLECTOR CURRENT)
- h_{FE} (DC CURRENT GAIN)

DC TRANSISTOR MODEL

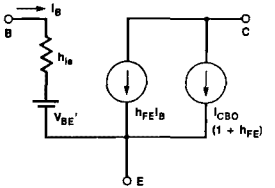


FIGURE 4

COLLECTOR CURRENT VS. V'_{BE} AND TEMPERATURE

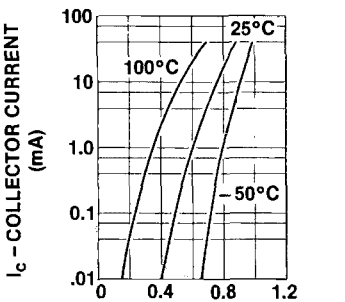
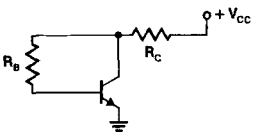


FIGURE 5

EVEN FOR SIMPLE BIAS CIRCUITS THE EQUATIONS BECOME COMPLICATED



$$\bullet\ Sh_{FE} = \frac{h_{FE}R_C + R_B + h_{IE} + R_C)\,(V_{CC} - V'_{BE} + KI_{CBO})}{(h_{FE}\,R_C + R_B + h_{IE} + R_C)^2}$$

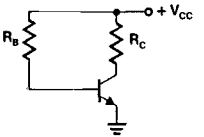
$$- R_C \left[\frac{(h_{FE}\,(V_{CC} - V'_{BE} + KI_{CBO}) + KI_{CBO})}{(h_{FE}R_C + R_B + h_{IE} + R_C)^2} \right]$$

Where: $K = h_{IE} + R_B + R_C$

• GOT ALL THAT?

FIGURE 6

FIXED BIAS



$$\bullet\ I_C = \frac{h_{FE}\,(V_{CC} - V'_{BE})}{R_B}$$

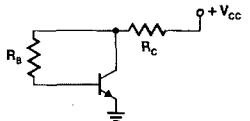
$$\bullet\ Kh_{FE} = 1$$

$$\bullet\ KV'_{BE} = \frac{1}{(1 - \frac{V_{CC}}{V'_{BE}})}$$

ADVANTAGE: FEW COMPONENTS.
DISADVANTAGE: INFERIOR TEMPERATURE STABILITY, LARGE I_C VARIATIONS

FIGURE 7

VOLTAGE FEEDBACK BIAS



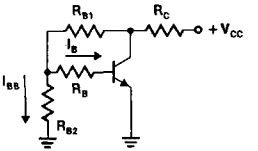
- $I_C = \dfrac{h_{FE}(V_{CC} - V_{BE})}{R_B + h_{FE}R_C}$
- $Kh_{FE} = \dfrac{1}{(1 + \dfrac{h_{FE}R_C}{R_B})}$
- $KV_{BE} = \dfrac{1}{(1 - \dfrac{V_{CC}}{V_{BE}})}$

ADVANTAGE: SAME AS FIXED BIAS, PLUS BETTER TEMPERATURE STABILITY

DISADVANTAGE: A HIGH R_C/R_B RATIO IMPROVES Kh_{FE}, BUT LOW VALUES OF R_B ARE DIFFICULT TO ACHIEVE

FIGURE 8

VOLTAGE FEEDBACK AND CONSTANT BASE CURRENT SOURCE



- $I_C = h_{FE}\left[\dfrac{-V'_{BE}A - R_{B2}V_{CC}}{R_BA + R_{B2}(h_{FE}R_C + R_C + R_{B1})}\right]$
- $KV_{BE} = \dfrac{1}{(1 - \dfrac{V_{BB}}{V'_{BE}})}$

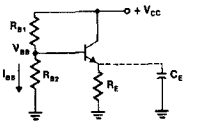
Where: $A = R_{B1} + R_{B2} + R_C$

ADVANTAGE: SAME AS VOLTAGE FEEDBACK PLUS CAN BE MADE h_{FE} INSENSITIVE BY SELECTING $I_{BB} > I_B$

DISADVANTAGE: MORE PARTS

FIGURE 9

EMITTER RESISTOR FEEDBACK



- $I_C = \dfrac{(V_{BB} - V'_{BE})h_{FE}}{h_{FE}R_E + R_B}$
- $Kh_{FE} = \dfrac{1}{\left[1 + \dfrac{h_{FE}R_E}{R_B}\right]}$
- $KV'_{BE} = \dfrac{1}{\left[1 - \dfrac{V_{BB}}{V'_{BE}}\right]}$, $SV'_{BE} = \dfrac{-1}{R_E}$

Where: $R_B = R_{B1} \parallel R_{B2}$

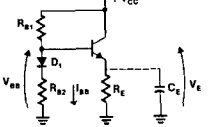
$$V_{BB} = \left[\frac{R_{B2}}{R_{B1} + R_{B2}}\right] V_{CC}$$

ADVANTAGE: VERY STABLE WHEN $h_{FE}R_E \gg R_B$. FEW PARTS

DISADVANTAGE: ADDED INDUCTANCE CAUSED BY R_E AND C_E

FIGURE 10

DIODE TEMPERATURE COMPENSATION



- $SV_{BE} = \dfrac{-1}{R_B(1 + \dfrac{R_{B1}}{R_{B2}})}$
- $V_E = V_{BB} - V_{BE}$

$$= \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC} + \left[\frac{R_{B1}}{R_{B1} + R_{B2}} V_D - V_{BE}\right]$$

- FOR TEMPERATURE INDEPENDANCE OF I_C VS V_{BE} THEN:

$$\left[\frac{R_{B1}}{R_{B1} + R_{B2}} V_D - V_{BE}\right] = 0$$

THEN:

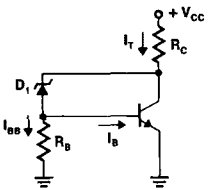
$$V_E \simeq \frac{R_{B2}}{R_{B1} + R_{B2}} V_{CC}$$

ADVANTAGE: STABILIZES I_C AGAINST V_{BE} CHANGES

DISADVANTAGE: EMITTER NOT GROUNDED. REQUIRES MORE PARTS

FIGURE 11

ZENER DIODE BIAS

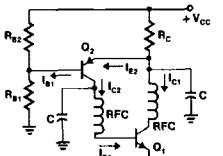


- $V_Z = V_{CE} - V'_{BE}$
- $R_C = \dfrac{V_{CC} - V_{CE}}{I_T}$
- $R_B = \dfrac{V'_{BE}}{I_{BB}}$

ADVANTAGE: EMITTER GROUNDED MORE STABLE THAN WITH A RESISTOR IN PLACE OF THE ZENER
DISADVANTAGE: NOISY

FIGURE 12

ACTIVE BIAS CIRCUIT



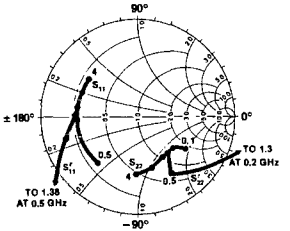
- $I_{C1} = \dfrac{h_{FE1}\left[\dfrac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} - V'_{BE2}\right]}{(1+h_{FE1})R_C + R_B/(1+h_{FE2})}$

  WHERE: $R_B = R_{B1} \| R_{B2}$
- If $(1+h_{FE1})R_C > \dfrac{R_B}{(1+h_{FE2})}$ THEN
- $I_{C1} = \dfrac{h_{FE1}}{(1+h_{FE1})}\left[\dfrac{\dfrac{R_{B2}}{R_{B1}+R_{B2}} V_{CC} - V'_{BE2}}{R_C}\right]$

ADVANTAGE: EMITTER GROUNDED, VERY STABLE, LOW POWER CONSUMPTION
DISADVANTAGE: USES THE GREATEST NUMBER OF PARTS, LOW FREQUENCY OSCILLATIONS POSSIBLE

FIGURE 13

EFFECT OF POOR EMITTER RESISTOR BYPASS



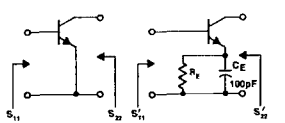
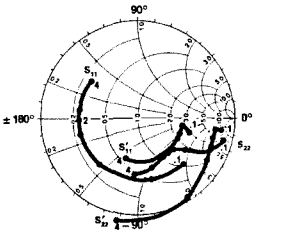
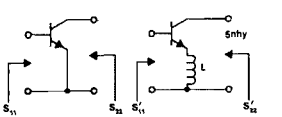


FIGURE 14

EFFECT OF EMITTER INDUCTANCE





PRACTICAL WIDEBAND RF POWER TRANSFORMERS, COMBINERS, AND SPLITTERS

by

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INTRODUCTION

This paper will deal with the practical aspects of designing and building wideband RF power transformers, combiners (or hybrids), and splitters. Emphasis will be on topology. A consistent approach to represent these transformers pictorially and schematically with equivalent circuits showing source and load connections will be developed to help provide an intuitive understanding of the devices. Laboratory test data comparing various designs and topologies is included.

Modern solid state HF power amplifiers are required to operate over increasingly wider bandwidths and at higher power levels for applications in communications as well as electronic countermeasures. Wideband RF power transformers are required for coupling into and out of the solid state devices. The conventional or so-called "wire-wound" transformer and two topologies of the transmission line transformer (conventional and equal delay) are presented.

A wideband RF power combiner (or hybrid) is required to achieve output levels above the capabilities of a single solid state amplifier stage. The RF outputs of two or more identical amplifier modules can be combined to reach these higher powers. Design examples of in-phase, 180-degree, and quadrature combiners are detailed. Two basic topologies for in-phase and 180-degree combiners are presented.

A wideband RF power splitter (or divider) is simply a combiner or hybrid used in reverse. The splitter topology is the same as a combiner, however splitters are usually operated at lower power levels. The discussion centers around combiners but is equally applicable to power splitter applications.

TRANSFORMERS

The bandwidth of rf transformers does not refer to the usual -3 dB points since in power applications this represents an unacceptable loss. Typical HF amplifier designs require operation from 2 to 30 MHz and sometimes lower to 1.6 MHz. The transformer losses must be as low as possible over this operational bandwidth. Transformer losses translate to heat that must be removed as well as extra power that must be supplied by the transistors (at the collector/drain efficiency) and ultimately by the power supply (at its conversion efficiency). A few tenths of a dB of unnecessary loss in output

transformers or combiners can mean significant increases in primary power consumption.

New RF power FET devices have operational bandwidths of 1 to 175 MHz making possible extended range amplifiers covering HF and the lower VHF frequencies. Transformer designs covering over six octaves of bandwidth are required.

A wideband RF power transformer performs one or more of any combination of three basic functions:

(a) Impedance transformation

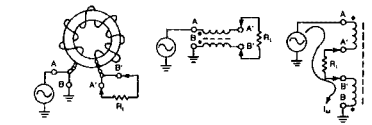
(b) Balanced to unbalanced transformation

(c) Phase inversion

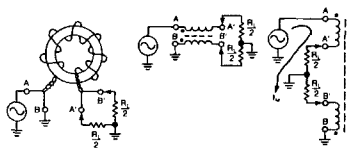
Transformation of a secondary load to a desired load impedance at the primary of the transformer is the most common function. RF transformers are often referred to by their impedance transformation ratio rather than primary to secondary turns ratio. The former is simply the turns ratio squared. In this application, we are most often interested in manipulating impedances rather than voltages or currents with the transformers. Balanced-to-unbalanced transformers, commonly termed "Baluns" are extremely useful in wideband amplifier designs. A single-ended load can be driven by a push-pull (balanced) source or vice-versa by using a balun transformer. A wideband transformer can also perform a phase reversal from primary to secondary by proper winding connections.

Transformer connections between a source and a load may be either balanced or unbalanced. Additionally, the balanced source or load may be either entirely floating or with center grounded such as two single ended sources phased 180-degrees apart or a load resistor with grounded center tap. The distinction between "balanced, floating" and "balanced, center grounded" may seem unimportant for wideband transformer design, but it is not. A proposed balun transformer equivalent circuit with source and load connected should be drawn showing the magnetization current path.

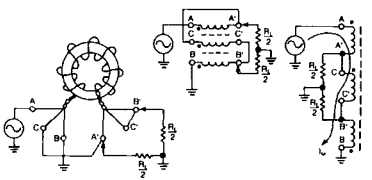
Figure 1 (a) is an example of a simple 1:1 balun with a floating balanced load. The magnetization current, i_m, flows through the load resistor as shown. Figure 1 (b) illustrates what happens to the magnetization current path if the balanced load is changed to a balanced, center tap grounded load. The magnetization current flows through only one winding and only one-half of the load resistance. This causes undesirable phase and amplitude imbalance in the balun restricting the bandwidth. The balance can be restored by using a third or tertiary winding, as shown in figure 1 (c), to shunt the magnetization current around the load. This illustrates the necessity of considering the type of source and load connections when selecting wideband transformer topologies.



(A) BALANCED LOAD, FLOATING



(B) BALANCED LOAD, CENTER GROUNDED



(C) BALANCED LOAD, CENTER GROUNDED WITH TERTIARY WINDING (C–C')

FIGURE 1. 1:1 TRANSMISSION LINE BALUN TRANSFORMERS

The nine possible transformer connections are given below:

SOURCE	LOAD
Unbalanced	Unbalanced
Unbalanced	Balanced, floating
Unbalanced	Balanced, center grounded
Balanced, floating	Unbalanced
Balanced, floating	Balanced, floating
Balanced, floating	Balanced, center grounded
Balanced, center grounded	Unbalanced
Balanced, center grounded	Balanced, floating
Balanced, center grounded	Balanced, center grounded

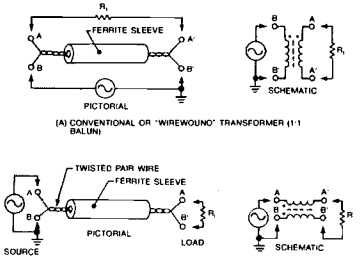
Wideband RF transformers and combiners typically use a magnetic core. The magnetic cores used in wideband RF transformers are available in a wide variety of shapes and sizes. Balun core, toroidal, sleeves, tubes, beads, and cup cores are the common names for the various shapes. The earliest material used was powdered iron followed by modern ferrites. Ferrite is composed of iron oxide in combination with various proportions of oxides of manganese, magnesium, nickel, and zinc. In general the ferrites composed of iron, nickel, and zinc are applicable for the HF/VHF frequencies. Various mixes of ferrites are available. A high permeability and moderately low loss material is used for HF/VHF power transformers. Operational flux densities must be kept well within the linear portion of the B-H curve of the material. The area inside the

B-H curve represents the relative loss, therefore the narrow curves are preferred for low loss designs. Detailed information is available from the various ferrite manufacturers.

Core losses and winding dielectric losses heat the core. The core temperature must be held well below the Curie temperature of the ferrite, otherwise the magnetic properties of the ferrite will be permanently altered. Operation near the Curie temperature is not recommended as some materials can go into thermal runaway. The high temperature increases the core loss which in turn further increases the core temperature until the core is ruined.

CONVENTIONAL OR "WIRE-WOUND TRANSFORMERS"

The conventional broadband RF transformer is characterized by a power transfer from the primary to secondary windings via magnetic coupling through the ferrite core. The transmission line transformer, by contrast, is characterized by the use of a transmission line of characteristic impedance, Z_o, and a ferrite core. The core suppresses common mode or non-transmission line currents which would otherwise flow due to the transmission line interconnections. A core wound with wire may or may not be a conventional transformer, depending upon how the source and load are connected. Figure 2 illustrates this distinction.



(A) CONVENTIONAL OR "WIREWOUND" TRANSFORMER (1:1 BALUN)

(B) TRANSMISSION LINE TRANSFORMER (1:1 BALUN)

FIGURE 2 COMPARISON OF CONVENTIONAL AND TRANSMISSION LINE TRANSFORMERS

In general, the conventional transformer is inferior to the transmission line transformer for the combination of high power capability, low loss, and wide bandwidth. The conventional transformer can be constructed for a wider range of impedance transformation ratios than the transmission line type. Some ratios will have wider bandwidths than others due to the number of turns to achieve the desired turns ratio. There are no fractional turns. If the wire or line passes through the core, it is one turn.

Figure 3 is a conventional transformer that finds wide usage at low impedances (3 to 20 ohms). The core is commonly referred to as a balun core, yet the transformer may or may not be connected to perform as a balun. Metal sleeves of copper or brass are inserted into the core and connected together at one end to form a primary winding. Connections to the circuit are made at each of the two sleeves at the opposite end. Two pieces of copper clad G-10 circuit board work nicely at each end. The secondary winding is constructed by winding the required turns of insulated wire through the primary tubes.

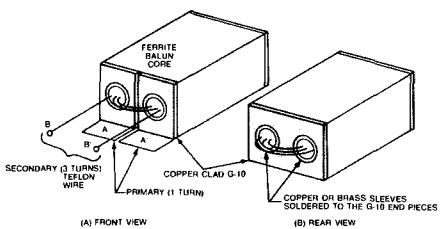


FIGURE 3. EXAMPLE OF A 1:9 IMPEDANCE RATIO CONVENTIONAL TRANSFORMER

One of the factors limiting the high frequency response of the transformer is leakage inductance. Leakage inductance is due to any flux lines that do not link the primary and the secondary. To minimize the leakage inductance, the primary copper tubes should fit quite close in the core holes. They should not be so tight that thermal expansion will cause the core to break. The lead inductances of the primary and secondary windings from the point they exit the core to the circuit connection will also limit performance at the high frequency end, especially on low impedance applications. Shunt capacitance on either the primary or secondary or both will compensate the leakage reactance and extend the useful high frequency limit.

TRANSMISSION LINE TRANSFORMERS

The simplest transmission line transformer is a quarter-wavelength line whose characteristic impedance, Z_C, is chosen to give the correct impedance transformation. This relationship is illustrated in figure 4. Note that this transformer is a narrowband device valid only at frequencies for which the line is odd multiples of a quarter wavelength. The *transformation ratio is given by* the square of the ratio of the line impedance to the load connected to the line.

FIGURE 4 SIMPLE QUARTER WAVE TRANSMISSION LINE TRANSFORMER

If a ferrite sleeve is added to the transmission line (see figure 5), common mode currents (currents flowing in both transmission line conductors in phase and in the same direction) are suppressed and the load may be balanced and floating above ground. The line can now be any length with characteristic impedance equal to the balanced load impedance. The result is a 1:1 balun. Low frequency operation is limited by the amount of impedance offered to common mode currents. A good rule-of-thumb requires the impedance presented to common mode currents be not less than five times the load impedance. The line length limits the high frequency response of transmission line transformers.

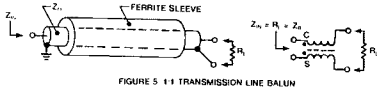


FIGURE 5 1:1 TRANSMISSION LINE BALUN

If the ferrite loaded length of transmission line in figure 5 is folded back so that the two ends may be interconnected, a 1:4 impedance transformer is formed. A load resistance, R_L, connected as shown in figure 6 is reflected to the input of the transformer as $R_L/4$. The line Z_0 should be equal to the geometric mean of R_L and Z_{in} for maximum bandwidth. The line length must be as short as possible for extended high frequency operation. The practical high frequency limit for this type of transformer is reached when the line length approaches 1/8 wavelength and appreciable phase error difference occurs at the interconnection of the lines.

A 1:4 transmission line balun transformer may be constructed as shown in figure 7. Two cores are required and may be either balun cores (as shown) or toroids or sleeve cores. The transmission line Z_0 should be the geometric mean of the input and load impedances. This transformer may also be used for balanced-to-balanced source and load connections. Transmission line baluns for 1:9 and 1:16 impedance ratios are constructed similarly as shown in figures 8 and 9. The limitation of squared integer transformation ratios is the biggest disadvantage of this type of transmission line transformer. The availability of coaxial cable in a variety of impedances is another limitation. 50 and 75-ohm cables are by far the most common but impedances of 25, 35, 60, 95, and 125-ohms are available.

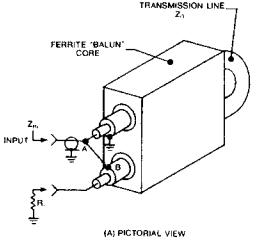


FIGURE 6. TRANSMISSION LINE TRANSFORMER; 4:1 UNBALANCED-TO-UNBALANCED

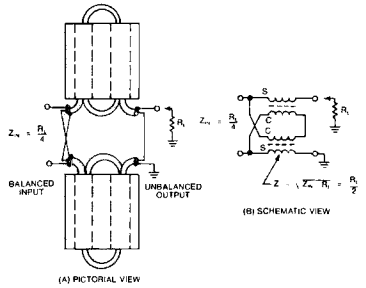


FIGURE 7. 1:4 TRANSMISSION LINE BALUN TRANFORMER

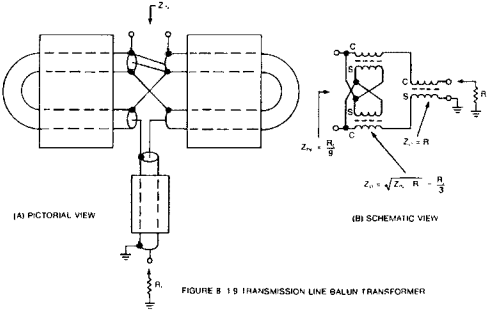
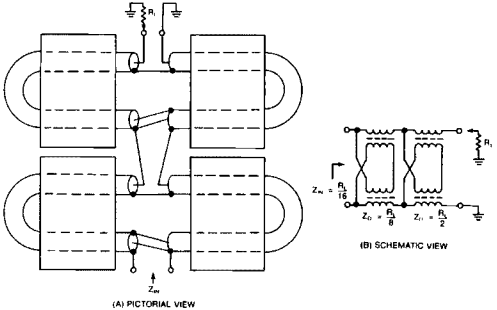


FIGURE 8. 1:9 TRANSMISSION LINE BALUN TRANSFORMER



(A) PICTORIAL VIEW

(B) SCHEMATIC VIEW

FIGURE 9. 1:16 TRANSMISSION LINE BALUN TRANSFORMER

Several techniques to achieve nonstandard impedance lines include simply parallel connecting two or more lines. For example, two parallel 50-ohm lines provide an effective 25-ohm line. The parallel lines do not have to be the same impedance either. Bifilar or twisted enameled wire can easily be constructed for odd characteristic impedances also. The impedance depends upon the wire diameter, insulation dielectric, spacing, and number of twists per unit length. Multiples of even numbers of wire may be twisted together and then parallel connected to achieve low characteristic impedances. The characteristic impedance of experimentally constructed bifilar or twisted pair transmission lines may be determined by measuring the reactance of an open circuit, 1/8-wavelength, sample. The magnitude of the reactance is equal to the line impedance at the frequency for which the line is 45-degrees in electrical length. Remember to account for the velocity of propagation when determining the frequency of 1/8 wavelength.

Micro-strip transmission lines on printed circuit boards is another technique for achieving virtually any desired line impedance. Mechanical problems with the strip lines in ferrite cores may be more difficult but interconnections with the amplifier circuit may be improved.

The bandwidth degradation experienced by not using the correct value of line impedance may be acceptable in some applications. Figure 10 is a comparison of two identical 1:4 balun transformers; one wound with the proper 25-ohm line, the other wound with 50-ohm line. The measurement was made by connecting two identical transformers back-to-back to provide matched 50-ohm impedance ports to interface with the network analyzer. The indicated loss of one transformer is half of the measured value. This technique is valuable for evaluating various transformer designs and initially chooseing values of compensation capacitors for leakage reactance.

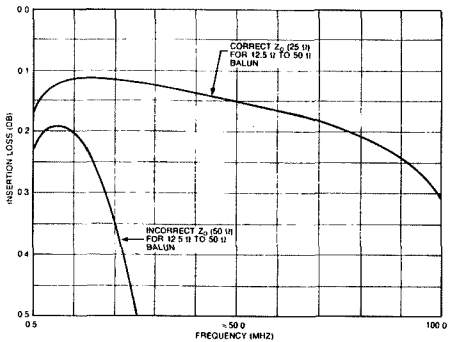


FIGURE 10. COMPARISON OF EFFECT OF Z_0 ON 1:4 BALUN TRANSFORMER

As pointed out earlier, the 1:4 transmission line transformers' high frequency response is limited when appreciable phase error is introduced at the interconnection point a-b shown in figure 11. If the connection a-b were made with a transmission line of equal impedance and length as the ferrite loaded line, the phase difference between input and output is eliminated. The transformer topology remains the same, except the a-b connection has the same phase delay as the main transformer line. For this reason this subclass of transmission line transformers are called "Equal Delay Transmission Line Transformers". The transformer input and output connections can be physically separated which is advantageous in some applications.

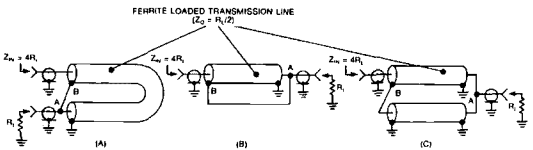


FIGURE 11. DERIVATION OF THE EQUAL DELAY TRANSFORMER

Figure 12 (a) is the usual pictorial and schematic representation of a 1:4 equal delay transformer. If a third line is stacked on the 1:4 design, a 1:9 impedance transformer results. In like manner, four lines produce a 1:16 transformer and so on. Figure 12 (b) and (c) illustrates these ratios. For comparison, if one unit of ferrite is required on the 1:4 transformer for a given bandwidth, then two units will be required for the third line on the 1:9 transformer. In like manner, the fourth line requires three units of ferrite for the same bandwidth. Notice that these designs are all unbalanced-to-unbalanced transformers. Suppose we add ferrite to the bottom line on the 1:4 transformer. Now we can lift the grounds on the parallel connected end (still keeping the shields

connected) and connect a balanced, floating load between the center conductors and the shields to form a 1:4 balun. The stray capacitance to ground can be balanced better by interconnecting the center conductor of one coax to the shield of the other coax. The result is the balun transformer described earlier in figure 7.

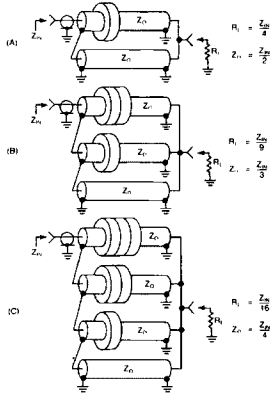


FIGURE 12 EQUAL DELAY TRANSFORMER CONFIGURATIONS

How much improvement in bandwidth does the equal delay transformer give compared to the conventional transmission line transformer? Figure 13 is a plot of insertion loss versus frequency for the two types constructed on identical cores. Again, the test consisted of measuring two identical transformers connected back-to-back, so the actual loss for one transformer is one-half the measured value.

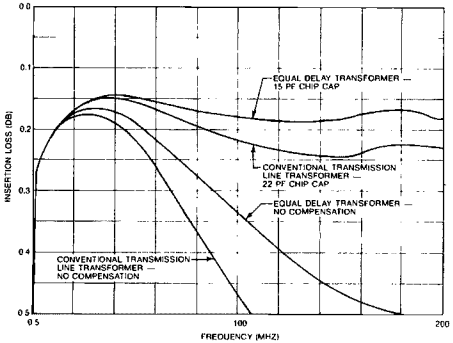


FIGURE 13 BANDWIDTH COMPARISONS OF CONVENTIONAL AND EQUAL DELAY 1:4 TRANSMISSION LINE TRANSFORMERS

COMBINERS AND SPLITTERS

When required output power levels exceed the capabilities of a single power amplifier stage, two or more stages or modules are combined to produce the required output. The combiner is closely related to wideband transformers in design and techniques. A power splitter is simply a lower powered version of the combiner used in reverse. The splitter divides the drive signal into multiple equal amplitude outputs to be applied to the amplifier inputs. The power combiner then recombines the amplified outputs into a single signal. Since the splitter is the same as a combiner, the following discussion will mention only combiners.

A wideband power combiner must perform the following basic functions:

a. Provide low insertion loss over the required bandwidth.

b. Provide isolation (minimum coupling) between the input ports.

c. Provide a low VSWR load at the input ports over the required bandwidth.

The operating bandwidth of combiners must be as wide or wider than the amplifiers to not restrict the overall bandwidth of the transmitter. Transmission line techniques are used for lowest loss and widest bandwidth. The primary function of the combiner is to maintain port-to-port isolation. By isolating the output of one amplifier from the others, multiple failures as a result of a single amplifier failure are avoided. For example, in a two-input-port combiner, if one amplifier is disabled the output power drops by 6 dB. The output drops 3 dB due to lack of power from the disabled module and an additional 3 dB is due to the power from the remaining module dividing equally between the bridging resistor and the output load.

The bridging resistor must dissipate -6 dB of the maximum combiner output power. The bridging resistor value is prescribed by the type and configuration of the combiner as detailed later. Some topologies require either single-ended or balanced, floating bridging resistors. Sometimes the bridging resistor is referred to as the "dump" load or "dump" port since power due to phase or amplitude imbalance is dumped to this load.

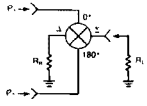
The bridging resistor dissipates power due to any slight differences in either the phase or amplitude of the input signals. This relationship is given in figure 14.

There are three basic types of combiners:

a. In-phase combiner or hybrid (two or more input ports)

b. 180-degree combiner or hybrid (two input ports)

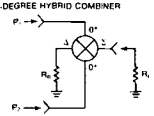
c. 90-degree combiner or quadrature hybrid (two input ports)



$P_{\Delta} = \frac{P_1 + P_2}{2} - \sqrt{P_1 P_2} \cos \theta$ WHERE θ IS DIFFERENCE IN PHASE BETWEEN INPUT PORT SIGNALS

$P_{out} = P_1 + P_2 - P_{\Delta}$

(A) 180-DEGREE HYBRID COMBINER



$P_{\Sigma} = \frac{P_1 + P_2}{2} + \sqrt{P_1 P_2} \cos \theta$ WHERE θ IS DIFFERENCE IN PHASE BETWEEN INPUT PORT SIGNALS

$P_{out} = P_1 + P_2 - P_{\Sigma}$

(B) IN-PHASE HYBRID COMBINER

FIGURE 14 HYBRID COMBINER POWR RELATIONSHIPS

If more than two signals are combined in-phase, the term "combiner" is used since the term "hybrid" refers to a device with two input ports. The topologies of each of the three basic configurations will be examined.

The following definitions apply:

R_L= output load resistance

R_B= bridging resistor

Z_O= transmission line characteristic impedance

Z_{in}= input impedance (with output port terminated)

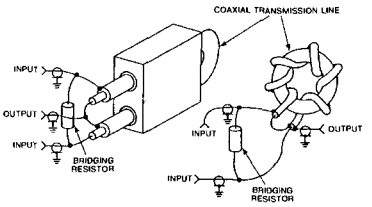
S = shield connection of coaxial cable

C = center connection of coaxial cable

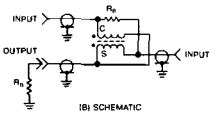
IN-PHASE COMBINERS

In-phase combiners operate with two or more inputs of equal phase and amplitude to combine into a single output. There are two basic topologies for in-phase combiners, examples of which are shown in Figures 15 and 16. The differences are in the number and configurations of the ferrite cores and the value of the bridging resistor. The type-I configuration has a single balun core or toroidal core and a bridging resistor equal to four times the output load. The type-II combiner has two separate cores; either sleeves or toroidal. The bridging resistor is equal to the load resistance. Consideration of physical layout, practical transmission line impedances (Z_O), and bridging resistance (R_B) will determine the best type of combiner for a particular design.

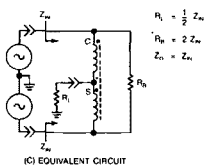
A comparison of input impedance and port-to-port isolation between typical type-I and type-II combiners yields interesting results as shown in Figure 17. Both combiners were constructed with a single turn of 50-ohm coax in the cores. Core material was Stackpole 7D for both types. The test data indicates superior port-to-port isolation with a type-II combiner while the type-I combiner exhibited lower input VSWR.



(A) PICTORIAL VIEW; BALUN CORE & TOROIDAL CORE

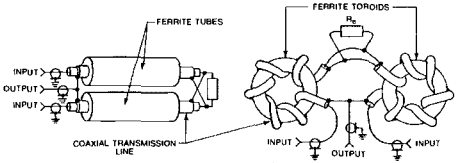


(B) SCHEMATIC

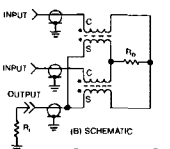


(C) EQUIVALENT CIRCUIT

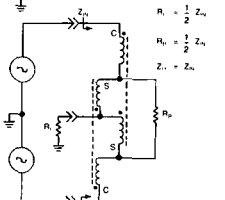
FIGURE 15 TYPE I IN-PHASE TWO PORT COMBINER



(A) PICTORIAL VIEW TUBULAR & TOROIDAL CORES

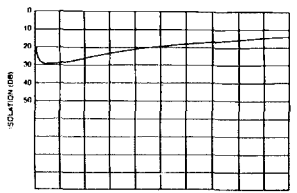


(B) SCHEMATIC

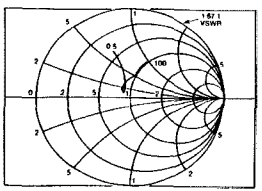


(C) EQUIVALENT CIRCUIT

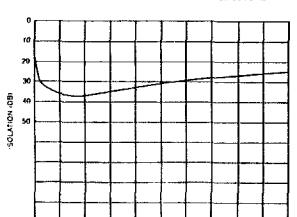
FIGURE 15 TYPE II IN-PHASE TWO-PART COMBINER



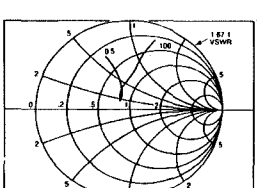
(A) PORT-TO-PORT ISOLATION, TYPE I IN-PHASE COMBINER



(B) INPUT IMPEDANCE, TYPE I IN-PHASE COMBINER



(C) PORT-TO-PORT ISOLATION, TYPE II IN PHASE COMBINER



(D) INPUT IMPEDANCE, TYPE II IN-PHASE COMBINER

FIGURE 17 COMPARISON OF TYPE I AND TYPE II IN-PHASE COMBINERS

The combiner output load impedance is usually transformed to another desired value such as 50 or 75 ohms. This is readily accomplished by one of the wideband transformers described earlier. Usually the output impedance transformer is physically integrated into the combiner assembly. The interconnection between combiner and transformer can be made using micro-strip line techniques if it is not a standard coax impedance.

Theoretically any number of inputs may be combined with an in-phase combiner, but a practical limit is reached when the output impedance becomes too low to allow efficient wideband transformation back to the desired load impedance. An example of a type-II four port in-phase combiner is given in figure 18.

Four-port combiners may also be implemented by cascading two port combiners. This technique is illustrated in figure 19 for both types of two port combiners.

In-phase combiners all use a floating bridging resistor. This may be difficult to implement, especially in combiners handling high power. A wideband balun transformer allows using a single-ended or unbalanced load. The balun could also transform the balanced impedance to 50 or 75 ohms. Standard coaxial dummy loads, connected to the combiner with coax cable, may then be used as bridging resistors.

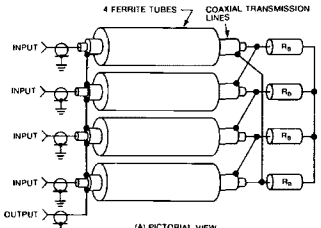


FIGURE 18 TYPE II FOUR PORT IN-PHASE COMBINER

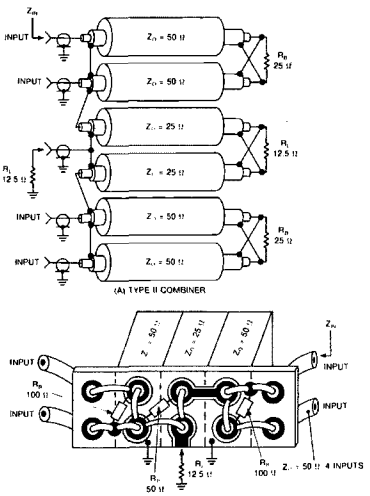


FIGURE 19 FOUR PORT COMBINERS IMPLEMENTED WITH TWO PORT IN-PHASE HYBRIDS

180-DEGREE HYBRIDS

If the roles of the bridging resistor and the load are interchanged, the result is a 180-degree hybrid combiner. The two input signals must be 180-degrees out of phase and of equal amplitude. The output is balanced to ground unless the usual balun is used. Examples of type-I and type-II 180-degree hybrid combiners with output baluns are shown in figures 20 and 21.

Many unique combiner designs are possible by using various combinations of basic combiner types and balun transformers. The combiner described in figures 22 (pictorial) and 23 (schematic) is an example of a four-port combiner using two each type-I in-phase combiners (cores A and F) and two each, parallel connected type-II 180-degree hybrid combiners (cores D and C) and a 4:1 balun transformer (cores B and E) to couple the combined output to a 50-ohm load. Connecting two 180-degree hybrids in parallel avoids using 25-ohm coax cable and provides the extra core material to handle the higher rf power.

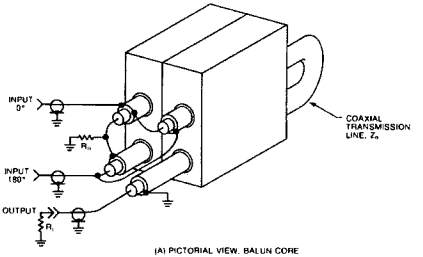
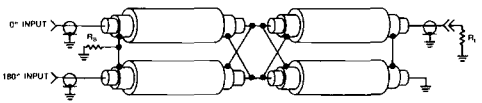
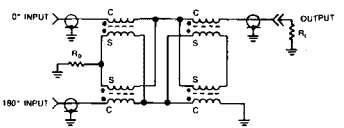


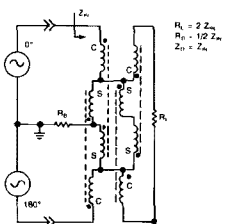
FIGURE 20 TYPE I 180-DEGREE HYBRID COMBINER



(A) PICTORIAL VIEW, TUBULAR CORES

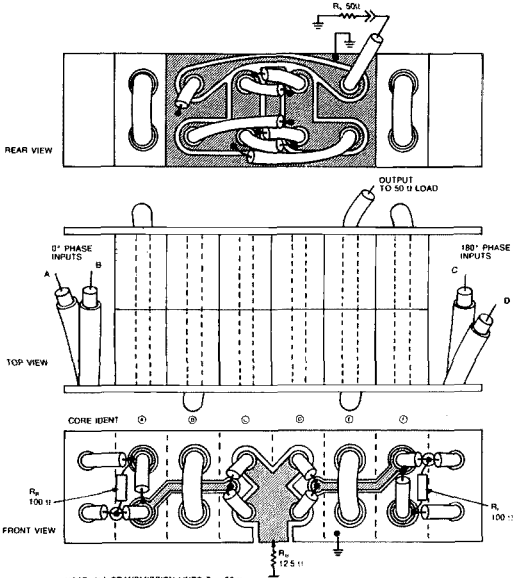


(B) SCHEMATIC



(C) EQUIVALENT CIRCUIT

FIGURE 21. TYPE II 180-DEGREE HYBRID COMBINER



NOTE: ALL TRANSMISSION LINES Z_0 = 50 Ω

FIGURE 22. FOUR PORT, TWO STAGE COMBINER USING TYPE I AND II HYBRIDS, PICTORIAL

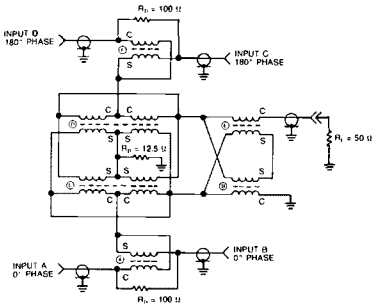

R_o = 100 Ω
INPUT D
180° PHASE
INPUT C
180° PHASE
R_o = 12.5 Ω
R_L = 50 Ω
INPUT A
0° PHASE
INPUT B
0° PHASE
R_o = 100 Ω
INPUTS A & B COMBINE IN-PHASE AS DO INPUTS C & D
THE A/B OUTPUT & THE C/D OUTPUT COMBINE IN TWO PARALLEL CONNECTED 180 DEGREE HYBRIDS. TWO IN PARALLEL AVOIDS 25 Ω Z_o COAX CABLE. 180 DEGREE COMBINER GIVES BALANCED 12.5 Ω LOAD IMPEDANCE, IDEAL FOR TRANSFORMATION WITH A 4:1 BALUN TO 50 Ω

FIGURE 23 FOUR PORT, TWO STAGE COMBINER USING TYPE I & II HYBRIDS; SCHEMATIC

QUADRATURE HYBRIDS

The quadrature hybrid has two input ports, each of equal amplitude but one is 90-degrees out of phase relative to the other. Four-phase combining of four amplifier modules is feasible using two quadrature hybrids and a 180-degree combiner.

The quadrature hybrid is constructed by using "all-pass" networks and a wideband hybrid as shown in the block diagram of figure 24. Two all-pass networks are required; one for 0-degree (reference) phase shift and the other for 90-degree phase shift relative to the reference output. The absolute phase shift across an all-pass network changes with frequency, however, the two networks are designed to maintain a constant 90-degree phase difference between their outputs as the input frequency to both networks is varied.

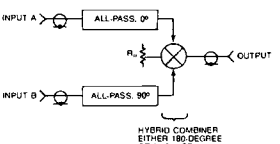


FIGURE 24 BLOCK DIAGRAM OF A QUADRATURE COMBINER

The all-pass networks may either be balanced or unbalanced circuits. Typical circuit topologies for both are shown in figure 25. Note that the mutual coupling in the unbalanced network must be negative and of a prescribed value.

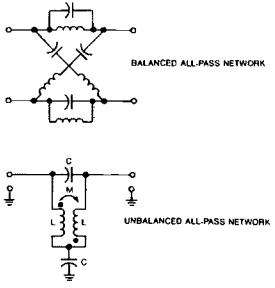


FIGURE 25. TYPICAL ALLPASS NETWORK TOPOLOGIES

Both circuits exhibit difficulties in practical implementation. The balanced lattice network may require long leadlengths and possibly a balun transformer for interface to an unbalanced hybrid. It requires more components than an equivalent unbalanced network and the component values must be closely matched to achieve low VSWR across the design bandwidth.

Implementation of an unbalanced all pass network allows shorter lead lengths and eliminates the balun transformer. It requires fewer components than an equivalent balanced all pass network. No closely matched component values are required, however, an exact amount of mutual coupling is required between two inductors.

The quadrature hybrid offers three advantages over the in-phase and 180-degree hybrids when used as an output combiner in solid state wideband power amplifiers. The third harmonic and certain other odd order harmonics cancel in the output port and add in the bridging resistor. The all pass phase shift networks and the basic combiner specifications must hold up to the frequency of the highest harmonic of concern to achieve this in practice. For example, the all-pass networks must provide the 90-degree phase difference up to at least 90 MHz in order to cancel the third harmonic of a 30 MHz fundamental signal in the hybrid's output.

RF power flowing into the output port of a quadrature hybrid will split, go through the all pass networks, partially reflect at the signal source impedance, go back through the all pass networks, and cancel in the output port and add across the bridging resistor. This is happens whether the power flowing into the output port is the result of a mismatched load or coupling from an adjacent transmitting antenna. The result is the combined power amplifier output behaves as though it has a matched source impedance. The situation of reverse power flow from adjacent transmitter coupling is especially important since the two signals cross modulate each other in the active devices. The

intermodulation products caused would be radiated along with the desired signal. The quadrature hybrid will cancel some of these "backdoor" IMD products in it's output port by terminating the energy in the bridging resistor.

Two wideband linear power amplifiers, combined with a quadrature hybrid, will exhibit nearly constant gain under varying load impedances (varying VSWR). The ratio of input power into the quadrature hybrid splitter to the forward power out of the quadrature hybrid combiner will be nearly constant in contrast to the same situation using in-phase or 180-degree hybrids.

Techniques for wideband RF power transformers, combiners, and splitters have been presented with emphasis on topology. Various types of transformers and combiners were examined and classified. Examples of each were presented in pictorial form, schematic, and equivalent circuit in an effort to bridge the gap from theory to working hardware. A rich variety of combinations of the basic transformers and combiners are possible though not covered here. It is hoped that a more complete understanding of the basic types presented here will enable the reader to produce more sophisticated designs.

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HIGH POWER UHF PULSED PUSH-PULL AMPLIFIER DESIGN

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Applications Engineer

October 1985

RF Push Pull amplifiers can be somewhat of a mystery to those engineers who've never designed one. This application note attempts to unlock some of that mystery by simplifying those nebulous areas that make a push pull amplifier different than a single ended or parallel amplifier. The name push pull in itself implies a different mode of operation than two transistors operating in parallel.

In a standard Class C amplifier, one half of the input sine wave (positive or negative) turns the amplifier on while the other half maintains a reverse bias. If a periodic sine wave symmetrical about a horizontal axis with positive and negative half cycles were being delivered to two Class C common emitter transistors in parallel, the positive half cycle would turn on both of the transistors while the negative half cycle would keep them reverse biased. In push pull operation, the sine wave is shifted 180 degrees for one of the two parallel transistors. The result is such that the positive half cycle is no longer delivered to each transistor simultaneously but instead separately so that when one transistor is on the other is off. This mode of operation has a lot of nice advantages not the least of which are thermal since two transistors in close proximity are not dissipating power at the same moment in time.

Figure 1 shows the current flow through a one to one transformer being delivered to two resistive loads where $R_S = R_1 + R_2$ and $R_1 = R_2$.

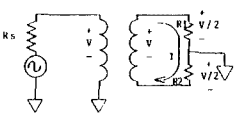


FIGURE 1

Since the primary voltage equals the secondary voltage and primary current equals secondary current, then the voltage drop across the two loads is equal assuming equal resistances. It's easy to see that during the positive half cycle current flows in a clockwise direction and R_1 has a positive voltage drop across it with respect to ground while R_2 has negative drop with respect to ground. If R_1 and R_2 were emitter base junctions, R_1 would be on and R_2 would be off during the positive half cycle. The negative half cycle is just the reverse.

Many times a one to one balun made out of a single piece of fifty ohm coax is used to generate push pull action in an RF amplifier. Figure 2 shows a typical arrangement. The electrical configuration is different than the one to one transformer in Figure 1, but the basic operation is the same.

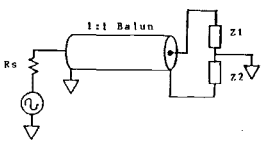


FIGURE 2

The center conductor acts as the primary and the outside shield acts as the secondary. The transformer coupling action between the primary and the secondary is identical to a one to one transformer in that there is an induced EMF in the secondary. The only difference between the coaxial transformer and a conventional transformer is the way the interwinding capacitance is laid out. In conventional transformers, the interwinding capacitance is an unwanted capacitance that limits high frequency performance because it resonates with the leakage inductance to produce a loss peak [1]. In transmission line transformers, the interwinding capacitance is arranged such that it is part of the characteristic impedance of the line. Therefore, if the transmission line transformer is terminated in its Z_0, there will be no resonances that will limit its upper frequency response. This means that the coaxial balun is a transmission line as well as a transformer.

Because the electrical configuration of the coaxial balun is identical to that of a twisted pair, the theoretical explanation of the balun will be carried out using the twisted pair. Figure 3A shows a conventional twisted pair. In order to maintain good transformer action, the primary and secondary must be tightly coupled. This results in interwinding capacitance which can be tolerated because it contributes to the Z_0 of the line. The inductance per unit length, along with the distributed interwinding capacitance, assigns some Z_0 to the transformer. The Z_0 simply becomes part of the matching circuit while the transformer allows for push pull action. If it were possible to achieve good coupling without interwinding capacitance, than push pull action could be achieved without the transmission line. Said another way, it is only necessary to have transformer action for the push pull effect, it is not necessary to have a transmission line.

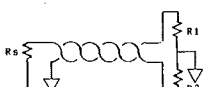
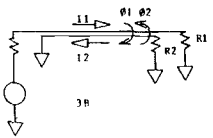


FIGURE 3A

Figure 3B shows the twisted pair in a simpler form so that it can be analyzed. During the positive half cycle, a current I_1 flows into the load R_1 causing an increasing magnetic field ϕ_1 in the direction shown by the right hand rule. The direction of the induced current in the secondary can be found by Lenz's Law: "If the external flux increases, the magnetic field of the induced current will be in the opposite direction" [2]. Therefore, ϕ_2 is responsible for the induced current I_2. The secondary is now a source with its own current and voltage. The voltage of this source is in such a direction as to maintain the direction of current I_2. [3] It's

important to mention here that thecurrents I_1 and I_2 are considered odd modes of currents which are the dominant modes in this type of transformer [4]. Even modes of current are not shown here but would be in the same direction instead of the opposite direction. Even modes of current are caused by flux linkages between the primary and secondary instead of linkages around each.

Summing up the voltages around the loop (Figure 3C) it's easy to see that the transformer primary voltage cancels the transformer secondary voltage so that the source voltage (Vs) is impressed across two equal loads just as originally shown in Figure 1. Since the current through the two loads is the same and the voltage across each is half the source voltage, the impedance of each is one half the source impedance. If a 50 ohm twisted pair (or coaxial line) is used, then each side of the balanced end is 25 ohm's to ground.



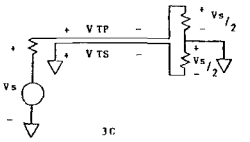


FIGURE 3B, C

DESIGN #1

A one to one coaxial balun will now be used in a push pull design. Inspection of Figure 2 shows that the length of the balun determines how much inductance to ground Z_2 will see. The impedance to ground of the outside shield of a coaxial cable is termed the rejection mode impedance. This is basically the X_L of this shield. If the balun is sufficiently long, this rejection mode impedance will not affect the match at Z_2 significantly. As a rule of thumb, the balun should be made long enough so that the rejection mode impedance is five times that of the Z_0 of the line [5]. If size constraints restrict the balun's length, an alternate solution would be to use the rejection mode impedance as a shunt L to ground at Z_2. This would then require an equivalent inductance to ground at Z_1 to insure that each side of the balun have the same complex impedance. The first design to be demonstrated will use this approach.

The SD1565 was selected for this narrowband 425 MHZ push pull 500 Watt application due to its excellent thermal characteristics under long pulse conditions. This transistor operates at 40 Volts and is capable of 500 Watts at 250 microseconds, ten percent duty cycle, Class C operation.

The input and output impedances from the data sheet are 1.75 + J2.75Ω and 1.8 + J.5Ω respectively. Referring to Drawing #1, which is normalized to 25Ω , the effect of shunt L can be seen. For convenience, the impedance and admittance coordinates have been reproduced on the left side of the chart. The inductive reactance of the outside shield of two inch semi-rigid coax was measured to be +J34.15Ω . Normalized to 25Ω this gives 34.15/25 = 1.366. Starting at the center of the chart at A (25Ω) and moving along the constant resistance circle to B gives a shunt inductive reactance value of 1.36 read at C. A series capacitance of value .48 read at D transforms the impedance to .65 at E. The unnormalized impedance at E is then (.65) 25Ω = 16.25Ω and the capacitance value at D is $C = 1/2 * F X_C$ where $C = 1/(2)\ (3.14)\ (425 \times 10^6)\ (.48)\ (25) = 31.2$ PF. This shunt L, series C high pass configuration will be the same for the input and output of the circuit (see Drawing #4) so that the rest of this example will be matched from the impedance of the device out to

16.25 Ω on input and output.

The output matching is configured using Drawing #2 and starts at 16.25 Ω at A (.65 normalized) and works back towards the generator (the transistor's output impedance). The movement from A to B represents a shunt capacitive reactance of (1.25) 25 Ω = 31.25 Ω at C. This reactance can be realized in a shunt configuration to ground or can be referenced to the opposite side of the balun. Since one side of the balun is always 180 degrees out of phase with respect to the other, the voltage across the balun is always twice the voltage to ground. Therefore, the same transformation can be realized by doubling the capacitive reactance to ground and referencing it to the opposite side of the balun. Instead of 31.25 Ω to ground then this becomes 62.5 Ω across the line. The value of capacitance across the line is given by:

$$(1)\ C = 1/(2\pi F X_C)\ (2)$$

where X_C is the unnormalized value.
Therefore $C = 1/(2)\ (3.14)\ (425 \times 10^6)\ (31.25)\ (2) = 5.9$ PF

Since the chart is normalized to 25 Ω all transmission line matching sections will be 25 Ω lines for simplicity. The first transmission line matching section transforms from B to E by rotating around the center of the chart along a constant VSWR circle from B toward the generator to the real axis. The length of line is determined by extending a straight line from the chart center through B. The value at D is then .054 wavelengths. One wavelength in free space equals

$$(2)\ \lambda_o = 11808/F\ (MHZ)$$

This becomes 11808/425 = 27.78 inches. The relative velocity of propogation for the substrate is .4729. The guided wavelength in the material is then

$$(3)\ \lambda_o \cdot V_p = \lambda_g$$

which gives $\lambda_g = (.4729)\ 27.78 = 13.137$ inches. The length of transmission line in inches is

$$(4)\ \lambda_g \cdot (\text{fractional wavelength}) = \text{physical length (inches)}$$

which gives 13.137 (.054) = .709 inches.

Another shunt capacitance moves from E to F which gives a reactance at G of (.5) 25 Ω = 12.5 Ω and a capacitance value from equation (1) of 15 pf. Another transmission line of length .037 read at H transforms from F to I. This length in inches is computed from (4) which makes it .486 inches. The last shunt capacitance moves from I to J and is computed from (1) to be 48 PF. The final transmission line is a movement from J to N and its length is computed from L minus M or .018 - .0035 = .0145. Then from (4) its length is .190 inches. Point N is the conjugate of the output impedance of the generator. Since the scheme here has been to match from the load towards the generator then it is necessary to match to the generators conjugate and not the output impedance of the generator itself. Point N is read as .072 - J.020, unnormalized is then 1.8 - J.5 Ω which is the conjugate of the output impedance of the transistor at 425 MHZ.

The input network will be configured on Drawing #3. The input impedance of the device is given to be 1.75 + J2.75 Ω and this is normalized at point A. Since this is the load the network configuration will still work towards the generator which is the 25 Ω point at the center of the chart. The first shunt capacitance immediately at the device leads is a movement from A to B and is read at C to be 50 PF from (1). A transmission line matching section from B to D is read at E to be .0535 which is .702 inches (4). The final shunt capacitance from D to F is read at G to be 13.5 PF (1). F is now matched to the center of the chart (25Ω) by the configuration of Drawing #1.

The completed circuit is shown in Drawing #4. Evaluation of this design showed very good performance at the 500 Watt level; however, a problem of instability was observed during drive up. To explain further, as the input power was varied, it was observed that the part would oscillate but once full power was applied complete stability was achieved. This is attributable to the fact that the part has higher gain at less than full power. Since the device is a common base configuration, at some frequency it has a negative resistance input component. This negative resistance component coupled with the

fact that the high pass (section from Drawing #1) has a series resonance which will reflect a zero impedance, at some frequency, to the device at the input and output sets the stage for potential instability. The solution for this is to get away from the series resonance by using a low pass configuration.

DESIGN #2

If a one to one balun is made long enough so that the rejection mode impedance does not contribute to the match, it can be characterized quite easily for the intended frequency of use. By connecting the balun as shown in Figure 2 and using good high frequency 25 Ω chip resistors for Z_1 and Z_2, the balun will show a low VSWR (50 Ω unbalanced impedance) for all frequencies where the unbalanced to balance transformation is occurring. At very low frequencies its input will simply be 25 Ω and at high frequencies it will be limited only by leakages [6]. No compensation for the rejection mode impedance is necessary if the balun is long enough. Drawing #7 shows a 5 inch balun suitable for UHF.

With the rejection mode impedance out of the way, the design will be fabricated between the device and 25 Ω . This second design will be broader bandwidth, from 400 to 450 MHZ which will require low Q matching. The Q is calculated from the following:

$$(5)\quad \frac{\sqrt{F1 \cdot F2}}{F2 - F1} = Q$$

For this example $Q = \frac{\sqrt{400 \cdot 450}}{450 - 400} = \frac{424.3}{50} = 8.5$

This is a 3 db Q which means that the half power points will be at the band edges. A more desirable situation would be to have 80% of max power at the band edges which would correspond to a .5 db Q. The conversion factor from a 3 db Q to a .5 db Q is .34 [7]. Therefore, 8.5 (.34) = 2.83. To be conservative, a Q of 2 will be used. A constant Q circle of 2, where Q = X/R, is plotted on Drawing #5.

Without the aid of an optimization program, the approach will be to select the transistors impedance at some frequency to design around. The center frequency is approximately 425 MHZ; however, all transistors exhibit some roll off with frequency so that an impedance point above center frequency will be used. A convenient point will be 435 MHZ. At 435 MHZ the transistors output impedance is 1.8 + J 2 Ω Drawing #5 is normalized to 25 Ω , point A. The first shunt capacitance from A to B is read at C to be 1.4 (25 Ω) = 35 Ω and from equation (1) C = 5.2 PF. From B to D is a length of transmission

line read from E to F as .0975 - .0609 = .0366. At 435 MHZ λ_0 = 11808/435 = 27.14 inches and λ_g = (.4729) 27.14 = 12.836. From equation (4) this length of transmission line is .470 inches. The shunt capacitance from D to G is read from C and H as

$$(6)\quad \frac{1}{X_1} - \frac{1}{X_2} = \frac{1}{X_C}$$

where X_C is the normalized reactance.

Therefore, $\frac{1}{.5} - \frac{1}{1.4} = \frac{1}{X_C}$ and X_C = .777. Unnormalizing and using equation (1), C = 9.4 PF. From G to J is a transmission line of length determined by I plus K where I = .0535 and K = .003. From equation (4) this length is .725 inches. The value of capacitance from J to M is read at L and N using equation (6) but now X_2 is a negative quantity since it's on the opposite side of the chart.

$$1/.142 - (-1/44) = 1/X_C$$

where X_C = .1415. From equation (1) and unnormalizing, C = 51.6 PF. The length of transmission line form M to P is read at O as .01558. This length is .200 inches. The impedance at P unnormalized is 1.8 - J.2 Ω which is the conjugate of the collector output impedance.

The input circuit is shown on Drawing #6. The input impedance at 435 MHZ is 1.75 + J2.65 Ω and is shown at A. The capacitance from A to B is measured at C plus D and computes to be 52 PF. The transmission line from B to E and measured at F plus G and computes to be .810 inches. The second capacitance from E to H read at I minus J is 8.7 PF. Another transmission line from H to M read at L minus K is .450 inches. Then the last capacitance from M to O measured at N is 4.9 PF which matches to 25 Ω .

The completed circuit is shown in Drawing #7 and provides excellent broadband performance. Typical performance shows in excess of 500 Watts at 400 MHZ through 430 MHZ and 480 Watts at 450 MHZ. The design is very stable with changes in power levels, changes in tuning and changes in collector voltage thus proving that the high pass design was the reason for some previous instability.

Conclusion:

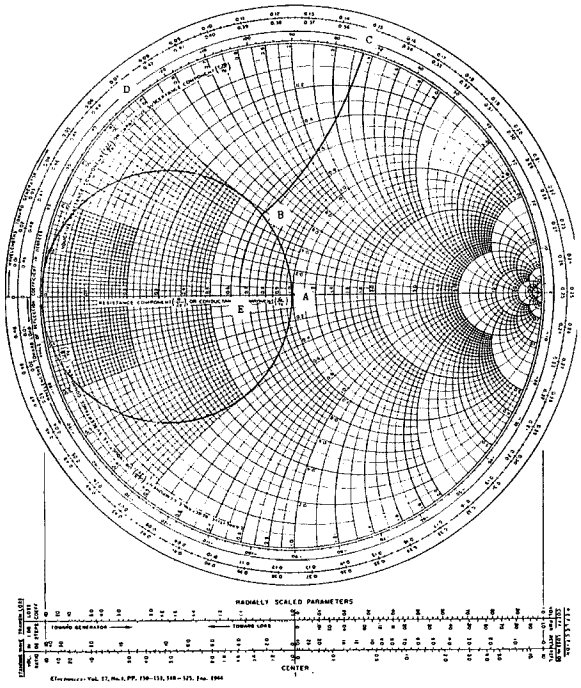
The theory of a one to one balun was described along with two applications. Both applications have definite advantages. In no way does this device note intend to imply that the high pass configuration is inferior. However, the conclusion is drawn that its application is better suited to high power common emitter or lower power common base devices.

It is recommended that all baluns are characterized before being used in a new design. Experience proves that the additional time to characterize baluns is worth avoiding the frustration of not knowing whether an inoperable circuit is due to the balun or matching components.

NAME	TITLE	DWG. NO.
D'Agostino	1565 Engineering Prototype	1
SMITH CHART FORM 823SPR (2-49)	RAY ELECTRIC COMPANY, PINE BROOK, N.J. 07058 PRINTED IN U.S.A.	DATE

Supersedes G R Form 5301 7560 N

IMPEDANCE OR ADMITTANCE COORDINATES

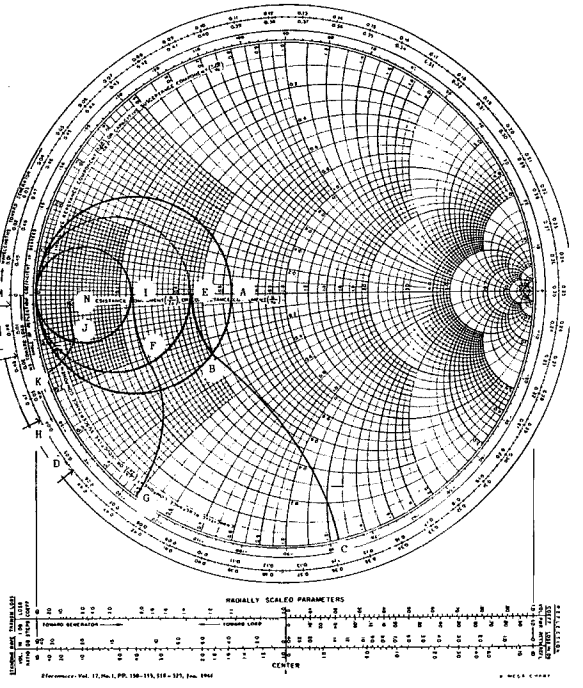


Electronics Vol. 17, No. 1, PP. 150–153, 310–325, Jan. 1944

NAME	TITLE	DWG. NO.
D'Agostino	1565 Eigineering Prototype	2
SMITH CHART FORM 823SPR (2-49)	RAY ELECTRIC COMPANY, PINE BROOK, N.J. 07058 PRINTED IN U.S.A.	DATE

Supersedes G R Form 5301 7560 N

IMPEDANCE OR ADMITTANCE COORDINATES

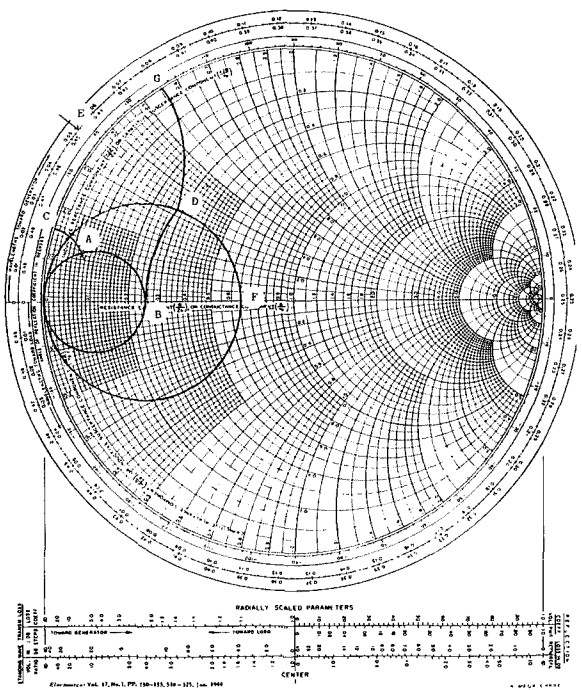


Electronics Vol. 17, No. 1, PP. 150–153, 310–325, Jan. 1944

NAME	TITLE	DWG. NO. 3
D'Agostino	1565 Engineering Prototype	DATE
SMITH CHART FORM 823SPR (2-48)	RAY ELECTRIC COMPANY, PINE BROOK, N.J. ©1958 PRINTED IN U.S.A.	

Supersedes G.R. Form 5301 1960 N

IMPEDANCE OR ADMITTANCE COORDINATES



Drawing # 4

THOMSON-CSF

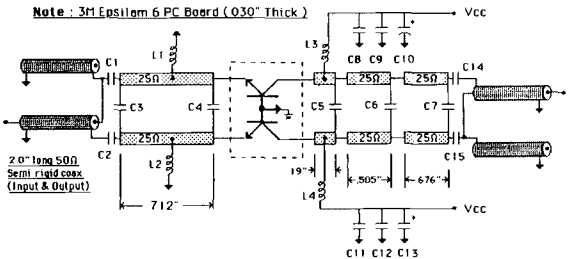
MONTGOMERYVILLE, PENNSYLVANIA

SEMICONDUCTOR DIVISION

SD1565-H8
Circuit Diagram
425 MHz Engineering Prototype

.400 X .500
4 Lead Flange

Note : 3M Epsilam 6 PC Board (.030" Thick)



Component	C1,C2,C14,C15	C3	C4	C5	C6	C7	C8,C11	C9,C12	C10,C13	L1,L2,L3,L4
Value	32	13	50	48	15	5	1	1000	1000	12.5 turns Number 24 Wire
Units	pF	pF	pF	pF	pF	pF	pF	pF	µF	

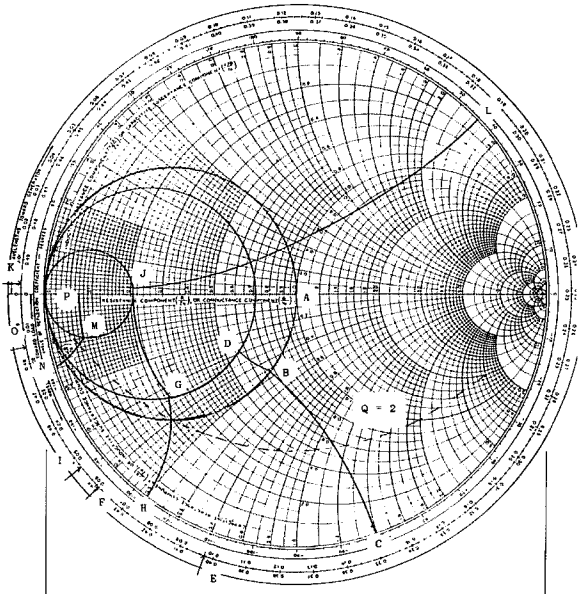
Comments: This engineering prototype circuit works well but it is unstable on drive up. Once the circuit is into saturation the stability is fine

NAME	TITLE	DWG. NO.
D'Agostino	1565 Broadband Circuit	5
		DATE

SMITH CHART FORM #893PR (2-68) KAY ELECTRIC COMPANY, PINE BROOK, N.J. 07058 PRINTED IN U.S.A.

Superseding K. P. Form 5301 7560 N

IMPEDANCE OR ADMITTANCE COORDINATES

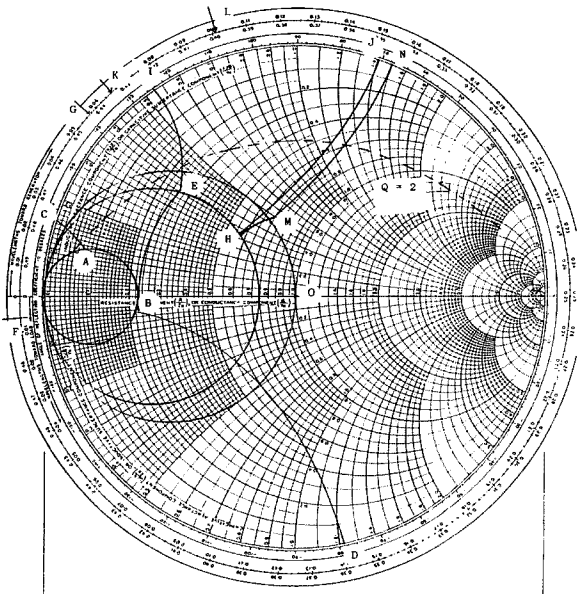


NAME	TITLE	DWG. NO.
D'Agostino	1565 Broadband Circuit	6
		DATE

SMITH CHART FORM #893PR (2-68) KAY ELECTRIC COMPANY, PINE BROOK, N.J. 07058 PRINTED IN U.S.A.

Superseding K. P. Form 5301 7560 N

IMPEDANCE OR ADMITTANCE COORDINATES



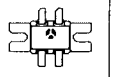
THOMSON-CSF Drawing # 7

MONTGOMERYVILLE, PENNSYLVANIA

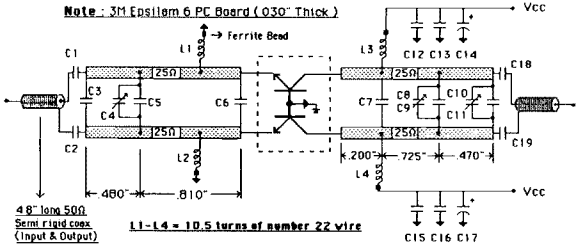
SEMICONDUCTOR DIVISION

SD1565-H0
Circuit Diagram
425 MHz Wide Band

.400 X .500
4 Lead Flange



Note: 3M Epsilam 6 PC Board (.030" Thick)



L1-L4 = 10.5 turns of number 22 wire

Component	C1,C2,C18,C19	C3,C11	C4,C10	C5	C6,C7	C8	C9	C14,C17	C15,C18	C16,C19
Value	470	5	.4-4.0	8	52	8-8.0	7	.1	1000	1000
Units	pF	pF	pF	pF	pF	pF	pF	µF	pF	µF

Symbols	Values			Units	Test Conditions
	Min.	Typ	Max.		
Po *	500.0	-	-	W	f = 425MHz Vce = 40.0V Pin = 54W
Po *	450.0	480.0	-	W	f = 400 - 450 MHz Vce = 40.0V
Nc	50.0	55.0	-	%	f = 425MHz Vce = 40.0V Po = 500W
VSWR**	-	30:1	-	-	f = 425MHz Vce = 40.0V Po = 500W

*Pulse Width 250µS, 10% Duty Cycle
**All Phase Angles

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A 350 Mhz Dual-gate GaAs FET Frequency Multiplier

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Abstract

This paper describes a dual-gate FET frequency multiplier with 13 dB conversion gain for an input frequency of 350 Mhz. The bias on the second gate provides gain control in excess of 40 dB while maintaining better than 20 dB return loss.

I. Introduction

Since its development in 1966 [1], the GaAs MESFET has continually increased in popularity. In its youth, the GaAs MESFET was used almost exclusively in high microwave frequency and low noise applications where low cost silicon transistors were not functional. An increased interest in GaAs technology has produced a variety of GaAs FETs including the dual-gate GaAs FET which was developed in 1971 [2]. The dual-gate FET has been widely used in mixers, variable gain amplifiers, and in modulators [3]-[5]. It has also been reported as a frequency multiplier with 8 dB conversion gain at Ku band [6].

Eventually, fabrication techniques have brought the cost down, and the high volume demand of such industries as mobile cellular radio has in particular brought about the development of a low frequency (less than 1 GHz), low cost dual-gate GaAs FET.

The purpose of this paper is to demonstrate the feasibility of using a low cost dual-gate GaAs FET as a frequency multiplier and to indicate the important parameters in the design of this multiplier. This paper presents the design of a frequency doubler with 10 dBm output power and 13 dB conversion gain for an input frequency of 350Mhz.

II. The Dual-gate FET

The characteristics of the dual-gate FET have been well documented [1]-[6], and will be presented here as a brief summary. The forward transconductance of a dual-gate FET has inherent non-linear characteristics which can be used to generate harmonics of the drive frequency. The addition of a second gate provides a simple means to vary the device gain, with little effect on the characteristics of the first gate. In addition, with proper RF termination of the second gate, the dual-gate FET has higher gain than the single-gate FET of the same width [3].

III. Circuit Description

The dual-gate FET multipier can be used in a variety of applications requiring frequency doubling and gain control. The application discussed here is the replacement of current

circuitry which consists of a PIN diode attenuator and a bipolar multiplier. The redesign was motivated by three factors: first, the PIN diode attenuator reqires a fairly large amount of board space; second, the attenuator requires more current than can be provided by a common Op-amp, thus requiring additonal transistors for current supply; finally, the dual-gate FET is much easier to bias since the bias on the PIN diodes must inversely track each other to maintain 50 ohms input and output impedances.

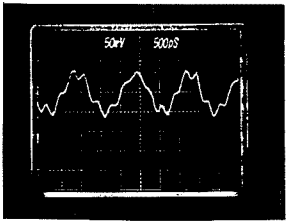
In order to be a functional replacement for the present circuitry, the dual-gate FET doubler is required to deliver an output power ranging from +8 dBm to -7 dBm with an input power to the multipier of -3 dBm at 350 Mhz.

The multiplying device used for this circuit is an MRF967. However, for commercial applications, the MRF966 or NEC's NE41137 could be used. The multiplier is constructed on 30 mil Teflon glass with 50 ohms input and output impedances.

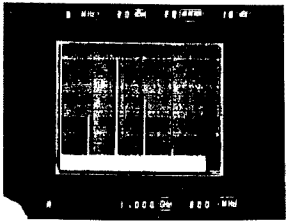
With sufficient RF voltage at the first gate, the FET generates harmonics in the drain current due to its non-linear transfer characteristics. The output circuit filters the desired harmonic while reflecting the unwanted components. It is important that at the fundamental frequency the filter produce a low impedance on the drain rather than a high impedance because, for a given peak drain voltage, any voltage at the fundamental frequency requires a corresponding decrease in the peak voltage of the second harmonic. Also, for power efficiency, it is important that there be a reactive load for the higher order harmonics. A square wave at 2 Fo yields a voltage component at 2 Fo of 1.3 times the voltage of the square wave. This suggests that the drain voltage should include odd harmonics of 2 Fo.

An output filter which is an open circuit above 2 Fo provides a means for the higher harmonic voltages to add to the second harmonic voltage to produce a square wave. In contrast, a filter that becomes short circuited at higher harmonics could also be used to reflect those components, but would reduce the possibility of generating a square wave voltage at the drain. Both types of filters were used, and while the open circuit filter gave better results, it is believed that this is a result of better reflection of the unwanted harmonics rather than improved drain voltage wave form.

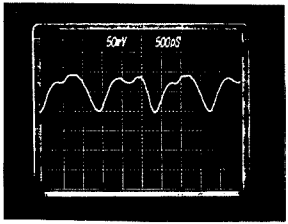
Figures 1a and 1b show the drain voltage and output spectrum, respectively, with the short circuit filter, while Figures 1c and 1d show the results with the open circuit filter. The figures show that the wave shape of the drain voltage is not an improved square wave when using the open circuit filter, however, the unwanted harmonics are better suppressed. It is believed that the reason the open circuit did not produce a square wave is that the harmonics were not added in proper phase. In fact, the filter was replaced with two quarter-wave stubs such that the impedance was a short at all odd harmonics of Fo, passed 2 Fo, was a short at even harmonics of 2 Fo and an open at odd



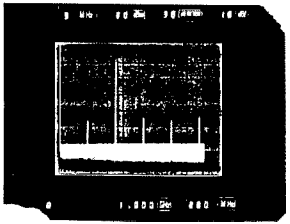
(a)



(b)



(c)



(d)

Figure 1. Drain voltage and output spectrum of multiplier different filter schemes. (a) and (b) correspond to a short circuit filter, (c) and (d) correspind to an open ciruit filter. NOTE: The voltages in (a) and (c) were measured through a resistive divider which corresponds to 5V/div.

harmonics of 2 Fo. This is the condition required for generating a square wave at 2 Fo; however, the odd harmonics of 2 Fo added to the voltage produced by the 2 Fo component in the wrong phase, and instead of a square wave, it produced a triangle wave which degraded performance. This experiment tends to verify the assumption that the improved performance due to an open circuit filter was the result of better filtering.

It has also been demonstrated that a reactive termination at the second gate is very important in maximizing gain [3]. A sliding short was used for RF termination on gate 2 to allow adjustments of the reactance in order to optimize conversion gain.

Finally, a triple stub tuner on the output and a series and shunt variable capacitor on the input were used to match into 50 ohms.

IV. Circuit Optimization

Figure 2 shows the circuit schematic. With Vd set at 5 volts and P_{in} at -3 dBm, Vg1, Vg2, the termination at g2, and the load impedance were simultaneously adjusted to give maximum conversion gain. The first attempt at optimizing the circuit was done by optimizing the gain with respect to one variable, then holding that variable constant, optimizing with respect to another variable, and then the next variable, etc., and continuing again with the first variable until all variables were

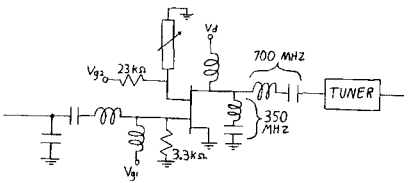


Figure 2. Circuit schematic showing open circuit type output filter.

optimized. It was found that by setting the voltage at g1 and adjusting the other variables a maximum could be reached where changes in Vg1 or any other variable only degraded performance, which indicated that the circuit was optimized. However, by setting Vg1 at a different value and re-optimizing the other variables, a different optimum (sometimes better) was reached. The same phenomenon was observed when holding any other variable constant. Therefore, one could not simply tune each variable one at a time and arrive at the global optimum. It was observed, however, that the optimum position of the sliding short did not change much from one optimum to the next, thus giving a good starting point for that variable. The optimum Vg1 and Vg2 were found by plotting optimum gain against set values of Vg1 and Vg2. This data was found by starting at a fixed Vg1 and Vg2, adjusting

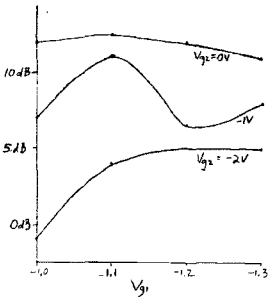


Figure 3. Optimum gain vs. Vg1 with Vg2 as a parameter.

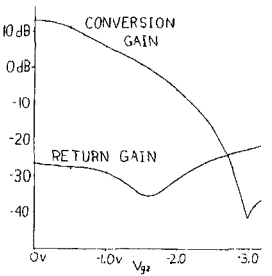


Figure 4. conversion gain and return loss vs. Vg2.

the output impedance to its optimum, and then adjusting the sliding short to its optimum position. The gain was then recorded, Vg2 was incremented, and the circuit was optimized again. After repeating this over the range of Vg2, Vg1 was incremented, Vg2 reset, and the process was repeated. This process gave the plot of optimum gain vs. Vg1 and Vg2 which was used to determine optimum bias conditions.

V. Results

The gain data obtained from optimizing at various bias conditions is shown in Figure 3. The optimum bias was determined

from Figure 3 to be -1.1 volts at g1 and 0 volts at g2. The corresponding termination on gate 2 was measured to have a reflection coefficient of $1\angle 36$deg. at 700 Mhz.

According to small signal theory, the optimum voltage on g2 should have been +2V [2],[3]. However, very little improvement was achieved here at higher voltages, and in fact, as Vg2 became positive,the circuit stability became very sensitive to changes in the termination at gate 2 and in the output circuitry.

With the variables held constant at the positions of maximum gain, Vg2 was decremented to give conversion gain and return loss as functions of second gate bias voltage. The shunt resistor on gate 1 degraded conversion gain by about 1 dB, but it improved the variation of the input impedance significantly. Figure 4 shows the conversion gain and return gain as functions of Vg2. As indicated in the figure, this circuit gave 12 dB conversion gain with -3 dBm input power, and demonstrated more than 50 dB gain control while maintaining better than 20 dB return loss.

VI. Conclusions

The usefulness of a low frequency GaAs dual-gate FET as a frequency multiplier has been demonstrated. This multiplier slightly exceeded its maximum output requirement of 8 dBm and exceeded its range requirement by almost 40 dB, demonstrating the dual gate FET's unique feature of gain control through the bias of its second gate. Furthermore, with the correct termination on the second gate, the dual-gate FET provides more gain than can be achieved from a single-gate FET of the same size.

Acknowledgements

The author wishes to thank J. P. Young for his participation in technical discussion.

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AIDING COMPUTER-AIDED DESIGN
Curve Fitting With Any Number of Variables

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Introduction

A large amount of specialized design data is not available in convenient form for use with computer-aided design (CAD) systems. This data may be in tabular form, graphical form, or as a large mathematical system requiring advanced solution techniques. A polynomial or other simple function can often be used to approximate the data over some limited range of independent variables. The resulting approximations are in a convenient form and can be used in existing CAD programs or with custom CAD software.

Multivariate Curve Fitting

If given a set of (n) observed data points (Y_i, i = 1 to n) and a set X of the m independent variables that generated them ($X_1, X_2, \ldots X_m$), it is convenient to approximate the Ys with some function:

$$Y = F(X_1, X_2, \ldots X_m). \tag{1}$$

The function F must be linear in its coefficients, its form must be:

$$[B_1 \times G_1 (X_1, X_2, \ldots X_m) + B_2 \times G_2 (X_1, X_2, \ldots X_m) + B_k \times G_k (X_1, X_2, \ldots X_m)] \tag{2}$$

Where each function G has no undetermined coefficients.

Equivalently:

$$\frac{dC_j}{dB_j} = 0 \tag{3}$$

and

$$\frac{dF}{dB_j} = G_j \tag{4}$$

for j from 1 to k.

With these restrictions it is possible to find the coefficient set B directly using linear algebra.

Utilizing the least squares method to find the set of B coefficients that form the best fit to the given data set, a function of the form

$$e = \sum_{i=1}^{n} [Y_i - F_i (X_1, X_2, \ldots X_m)] \tag{5}$$

needs to be minimized, where e is the sum of the squares of the errors (SSE).

By setting:

$$\frac{de}{dB_j} = 0 = \sum_{i=1}^{n} (Y_i - \frac{dF_i}{dB_j})^2 \tag{6}$$

a set of k equations in k unknowns is generated, and allows a solution for the elements of B.

Matrix Solution

There is a concise solution to the set of equations generated by Equation (6). The first step is to define the following matrices:

1. X is a matrix of n rows and k columns, where each row consists of the functions $G_1, G_2, \ldots G_k$ applied to the independent variable set
2. X^t is the transpose of X
3. Y is a column vector of the dependent variables to be approximated
4. B is a column vector of the coefficients B_k that we wish to find
5. e is a column vector of the errors in the approximation at each point.

It can be shown (Reference 1) that to determine B, the matrix equation

$$[X^t X] B = X^t Y \tag{7}$$

must be solved.

There are several ways to solve Equation (7), including methods that do not require forming the matrix inverse of $\mathbf{X}^t\mathbf{X}$. [Q-R Decomposition, (Reference 2)]. The general method of solving Equation (7) is to evaluate:

$$\mathbf{B} = [\mathbf{X}^t\,\mathbf{X}]^{-1}\,\mathbf{X}^t\,\mathbf{Y} \tag{8}$$

Although not as efficient as the Q-R Decomposition, its methodology is somewhat clearer and provides results adequate for the purpose at hand.

Choice of a Basis Function

Virtually any function with the appropriate number of variables is a suitable basis function, as long as it is linear in its coefficients. The following are some examples of linear and nonlinear basis functions:

$$F = Axy^2 + Byz^3\ COS(w) + C\sqrt{X} + De^{(2x+1)} \tag{9}$$

Equation (9) is linear, with coefficients A through D to be determined.

$$F = Ax^By^Cz^D \tag{10}$$

Equation (10) is also linear; however logarithms must be used to transform it to:

$$\log(F) = \log(A) + B\log(x) + C\log(y) + D\log(z). \tag{11}$$

Finally, the equation

$$F = A\cos(Bw + C) \tag{12}$$

is nonlinear in its coefficients, as there is no transform that will separate all unknowns (A,B,C) into linearly independent functions of the variables.

The choice of basis function depends largely on what result is desired. For multivariate problems, a family of polynomials is a good choice because of its simplicity and the ability to add as many variables as needed. Polynomials are also the easiest to implement in CAD programs, and run the fastest. It should be noted that a polynomial in the form

$$(Ax^3 + Bx^2 + Cx + D)(Ey^3 + Fy^2 + Gy + H)(Jz^3 + Kz^2 + Mz + N) \tag{13}$$

must be expanded to:

$$A_1X^3Y^3Z^3 + A_2X^2Y^3Z^3 \ldots A_{64} \tag{14}$$

to make the coefficient set linear. Also note that what initially appears to be a system with 12 unknowns actually requires solving for 64 coefficients. Given the 64 coefficients, it may be possible to separate them and solve for the set (A,B, ...N) but this is a difficult task and the coefficients are generally complex.

The degree of the individual polynomials should be chosen with some discretion. As the individual number of terms grow, the number of coefficients to be determined grows alarmingly. A large number of coefficients makes the matrix $\mathbf{X}^t\mathbf{X}$ large, and many data points are required to prevent it from becoming singular. If the system is not heavily overdetermined (i.e., n >> m) the fit will be "wavey" (Figure 1). In Figure 1, a 1st, 4th and 8th degree polynomial approximate a set of points. As the order of the polynomial increases, the error of the approximation *decreases until the SSE is 0. Although this fit is technically correct, as* it hits all the points, it clearly fails to provide a good interpolation to the data set.

The last basis set to consider is the function:

$$f = A0 + A1\sin(w) + A2\sin(2w) \ldots + Ap\sin(pw) + B1\cos(w) + B2\cos(2w) \ldots + Bq\cos(qw) \tag{15}$$

where both p and q do not both = 0.

When this series is truncated to some finite number of terms, the result is an approximation to a Fourier transform. The data must be transformed using equation (16) to the interval (-pi,pi) or (0,2pi). While this is not the most efficient method of calculating a Fourier transform, it does allow the freedom to make A, and B polynomial functions. The Fourier transform of some data set may then be calculated as a function of another variable, allowing one to optimize a particular coefficient.

Scaling

As higher degree functions are used to fit a particular data set, the individual terms in the **X** matrix become larger. When they differ by several orders of magnitude, the potential for numerical error increases, and inversion of $\mathbf{X}^t\mathbf{X}$ becomes a larger problem. To counter this, all of the dependent and independent variables should be mapped onto the range (-1,1) using a linear transform (Equation (9)). After the regression is performed, the inverse transform can be applied to map the function back to its original range. All terms of **X** and Y will then lie between $\pm$ 1:

$$Vl = \frac{2}{(Vmax - Vmin)} \times V + \frac{(Vmin + Vmax)}{(Vmin - Vmax)} \tag{16}$$

When scaled in this manner, the coefficients of the regression follow a set pattern. That is, the coefficient that makes the smallest contribution to the approximation has the smallest absolute magnitude. If the exact number of basis functions for optimum fit isn't known, one can begin with a large number of them, and repeatedly perform the regression, dropping the least important function until either the accuracy begins to erode or the desired number of functions remains.

Quality of the Fit

After approximating a set of data with some function, a natural question is "How good a fit is it?". In other words, does the derived function accurately model the data, or is a more or less elaborate model needed? A common way to answer this question is to consider the multiple regression coefficient, or R^2. R^2 is defined as:

$$R^2 = \frac{\sum_{i=1}^{n} (\hat{Y}_i - \bar{Y})}{\sum_{i=1}^{n} (Y_i - \bar{Y})} \qquad (17)$$

Where $\bar{Y}$ is the average value of y
$\hat{Y}$ is the predicted value of y
Y is the data set
i is taken over the range 1 to n.

R^2 varies from 0 to 1. A value of 0 indicates that the fitted function approximates the data no better than $\hat{Y} = \bar{Y}$. A value of 1 means that the approximation has matched all the points exactly. This should be viewed with some skepticism, as R^2 can be made to equal exactly 1 by choosing as many coefficients as there are data points. (Again, see Figure 1 and its "wavey" fit.)

Limitations of Curve Fitting

Although curve fitting is a very powerful tool in many branches of science and engineering, its results must be taken with a grain of salt. The resulting equations must be viewed for what they are - an approximation over a limited range to a physical phenomenon. When using fitted curves, one must be careful to limit them to the range of data from which they were derived. They can be used for interpolation, but not for extrapolation. Outside of the intended range, the equations might do anything, and it certainly has no particular relationship to what the modeled system would do. And, if the system is not over determined to a sufficient degree, a "wavey" function may well result. Always plot your results to perform a visual inspection.

Example 1 - Suspended Stripline

A function for a frequency dependent suspended stripline transmission line is generated (Figure 2). The three parameters to be considered are strip width, dielectric constant of the substrate, and operating frequency. We will predict wave impedance (Zo) and effective dielectric constant (keff). The data will be scaled to the interval (-1,1). Variables mapped to this region are primed. Initial values were determined from a standard paper on suspended stripline (Reference 3) using the program SuperCompact. The time needed to calculate the 125 values for the regression took well over an hour on SuperCompact, which was running on the Apollo Domain System. The resulting polynomials run considerably quicker.

The curve is valid over the following range of input parameters with the corresponding transfer functions:

$$\text{Freq}' = (0.05714 \times \text{Frequency}) - 1 \quad [\text{GHz, from 0 to 35 GHz}] \qquad (18)$$

$$\text{Width}' = (0.04082 \times \text{Strip Width}) - 1.04082 \quad [\text{mils, from 1 to 50 mils}] \qquad (19)$$

$$Er' = Er - 3.2 \quad [\text{unitless from 2.2 to 4.2}] \qquad (20)$$

$$Zo = (Zo' + 1.41473)/0.01686 \quad [\text{in Ohms}] \qquad (21)$$

$$Keff = \frac{(Keff + 2.87945)}{1.09589} \quad [\text{unitless}] \qquad (22)$$

Additional parameters describing the stripline are:

$\frac{B_1}{h} = 3$, $\frac{B_2}{h} = 3$, $\frac{a}{h} = 10$ and the metal has zero thickness and is a perfect conductor.

The resulting functions are good over these ranges to within 2.67% for Zo and 4.5% for Keff.

(23)

$$
\begin{aligned}
Zo' = \; & -0.6385352098 - 0.1067620906\ Er' \\
& +3.481023304E\text{-}03\ Freq' + 2.435179168E\text{-}03\ Er' \times Freq' \\
& -0.5161190977\ Width' + 6.722957429E\text{-}02\ Width' \times Er' \\
& -2.867867028E\text{-}04\ Freq' \times Er' \times Width' \\
& 0.5297363704\ Width'^{2} - 6.539253142E\text{-}02\ Er' \times Width'^{2} \\
& -8.288004956E\text{-}04\ Er' \times Freq' \times Width'^{2} \\
& -0.3191094332\ Er' \times Width'^{3} + 3.948039494E\text{-}02\ Freq' \times Width'^{3}
\end{aligned}
$$

(24)

$$
\begin{aligned}
Keff' = \; & -0.1607894999 + 0.7549461296\ Er' \\
& +0.0814640615\ Freq' + 0.0572409262\ Er' \times Freq' \\
& +0.2464396608\ Width' + 0.1040612513\ Width' \times Er' \\
& +0.0454664369\ Width' \times Freq' + 0.0421388077\ Width'^{2} \\
& -0.1771355908\ Er' \times Width'^{3} - 0.0459836924\ Freq' \times Width'^{3}
\end{aligned}
$$

Waveguide E-Plane Septum Filter

A popular way of building waveguide filters is to place an array of rectangular strips of metal (called septa) in the E-plane of the waveguide. These septa may be etched, allowing easily repeatable filters to be built at a very low cost (Reference 4). To build such a filter, the septum is modeled as a Tee of inductors (Figure 3). The values Xs and Xp are a complex function of the septum, waveguide dimensions, and frequency (Reference 5). Owing to the dispersive nature of waveguide, Xp and Xs can be modeled *as physical inductors over only a narrow* bandwidth. Plots of Xs and Xp as a function of W with frequency as a parameter are available as small plots in the published literature. Approximate solutions for Xp and Xs as functions of physical dimensions may be had by solving a complex set of equations using the variational method (Reference 5). Since graphical data is available in the region of interest (i.e., WR-28), the simplest way to determine Xs and Xp is to fit a curve to the graphical data and use the resulting equations to design the filter. Initial values for the filter are generated from classical filter design methods (Reference 6).

The first step is to enlarge the graphical data so that values may accurately be read from it. An enlarging photo-copier works well, but it is also possible to use an overhead projector, a microscope with digital positioning, or whatever is most easily accessible. This data is operated on by Equation 8, yielding regression coefficients for the data set, along with the R^2 value and the SSE value. These coefficients are listed in Equations 29 and 30. Over the range 28 to 38 GHz and septum widths form 1 to 200 mil, the error is less than 2.6 and 2.5% for these equations:

$$W' = (0.01111 \times Width) - 1.22222 \tag{25}$$

$$F' = (0.16667 \times Frequency) - 5.33333 \tag{26}$$

$$Xp' = (2.41525 \times Xp) - 1.00977 \tag{27}$$

$$Xs' = (3.41329 \times Xs) - 1.25031 \tag{28}$$

(29)

$$
\begin{aligned}
Xp' = \; & -0.7348365815 - 0.4007322178\ W' \\
& +0.2520677187\ W'^{2} - 0.2189697101\ W'^{3} \\
& +0.1627606451\ W'^{4} + 0.2697266795\ F' \\
& -0.2522981693\ F' \times W' + 0.8263478164E\text{-}01\ F' \times W'^{2} \\
& 0.7993333394E\text{-}01\ F'^{2} - 0.4333514566E\text{-}01\ F'^{2} \times W'^{2} \\
& -0.8596676895E\text{-}01\ F'^{3} \times W'^{2} + 0.9651804516E\text{-}01\ F'^{3} \times W'^{4}
\end{aligned}
$$

(30)

$$
\begin{aligned}
Xs' = \; & 0.4674951695\ W' - 0.2667132517\ W'^{2} \\
& 0.1441766713\ W'^{3} + 0.5238057254\ F' \\
& +0.2172888051\ F' \times W' - 0.1135707485\ F' \times W'^{2} \\
& +0.5170873288E\text{-}01\ F' \times W'^{3} - 0.2741439220E\text{-}01\ F'^{2} \times W' \\
& +0.7424136480E\text{-}01\ F'^{2} \times W'^{2} - .8060922104E\text{-}01\ F'^{2} \times W'^{4}
\end{aligned}
$$

With a simple set of expressions for the reactance values, the filter design procedes along well worn paths (Reference 6). A 1 GHz bandwidth 3 dB ripple Chebychev filter was designed with a 35 GHz center frequency (Figure 4).

Conclusion

A method to fit a set of data to a group of basis functions in any number of variables has been described, along with criteria for judging the quality of the fit and the appropriateness of the basis functions used. Several design examples were used to show the application of curve fitting to typical microwave engineering problems. The limitations of curve fitting were discussed.

I would like to thank Joe Chenkin for the valuable help he has provided, particularly for the design of the filter.

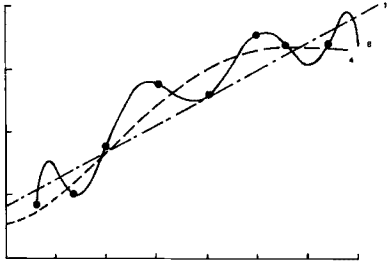

Figure 1. Increasing the degree of approximation improves the accuracy of the fit on a point by point basis, at the expense of a "wavey" fit.

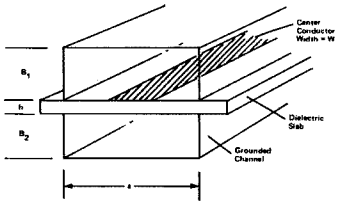

Figure 2. The 3 parameters to be considered in this suspended stripline are strip width, dielectric constant of the substrate and operation frequency.

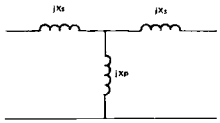

Figure 3. The e-plane waveguide septum filter was built by placing rectangular strips of metal (septa) in the e-plane of the waveguide.

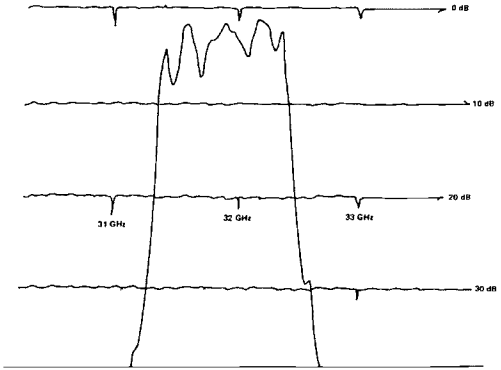

Figure 4. A 1 GHz bandwidth 3 dB ripple Chebychev filter, designed with a 35 GHz center frequency will produce the above response curves.

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OSCILLATOR DESIGN USING THE DEVICE LINE METHOD

AND LOAD PULL METHOD

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INTRODUCTION

The purpose of this paper is to examine two methods of oscillator design. The general requirements for designing an oscillator using the concept of the negative resistance one port will be covered, along with how the device line and load pull methods are used to determine the load impedance necessary for maximum oscillator output power.

NEGATIVE RESISTANCE ONE PORT

The design examples in this paper use the concept of transforming a three port bipolar transistor into a negative resistance one port. Before proceeding with a design example, the concept of the negative resistance one port needs to be examined. Figure 1 shows a negative resistance one port connected to a load which has both a reactive and resistive component. This network combination will start oscillating if the magnitude of the small signal resistance ($|R_D|$) is greater than the load resistance R_L, and at a frequency where the reactive components X_D and X_L are equal but of opposite sign. The steady state oscillation condition requires that $|R_D| = R_L$, which implies that the S-parameters of the one port decrease with increasing power. Computer programs can be used to design the one port and the output matching circuit required for oscillation, if the large signal impedances of the one port are known. The device line and load pull method provide a means of measuring the large signal impedances of the one port.

DEVICE LINE METHOD

As was pointed out above, one problem when designing an oscillator is not knowing what load impedance should be placed on the one-port to deliver the required output power and frequency. One solution to this problem is to measure the one-port impedance as a function of output power. The impedances can be measured by first designing the one-port not to oscillate when loaded by a 50 ohm generator. A network analyzer is used to measure the impedances as the one-port is driven by increasing input power. Since the one-port is a negative resistance device, the reflected power is greater than the input power. The added power is the reflected power minus the input power and will reach a maximum.

The above procedure has generated the device line for the one-port[1]. All of this may seem very complicated, but is really nothing more than the measurement of large signal S-parameters for an amplifier. In this case the amplifier is a one-port device and the test is limited to the measurement of S_{11}.
The design procedure may be summarized as follows:

1. Choose a transistor circuit topology that will induce a negative resistance on the terminal used as the output port. This circuit configuration will be determined in part by the transistor package used, and how the device will be biased.

2. Maximize the reflection coefficient of the one port using the transistor's small signal S-parameters. Figure 2 shows that when the one port reflection coefficent is infinity, the one port impedance is equal in magnitude to the load impedance, but with opposite sign.

3. If the circuit of step 2 does not oscillate into 50 ohms, then use the device line method to measure the load impedance for maximum output power.

4. If the circuit of step 2 does oscillate into 50 ohms, then use the load pull method to measure the load impedance for maximum output power[2]. Details of the load pull method will be covered later in this paper.

5. Design an output matching network using the measured load impedance.

6. Build a complete oscillator by combining the circuits of steps 2 and 5.

An example will help clarify the above procedure and how the negative resistance port is designed.

FIRST EXAMPLE

The first example uses an HXTR-4101 common base bipolar transistor. The goal is to design an oscillator at 4.3 GHz that will deliver the maximum output power from the transistor (about + 20 dBm)[3]. The objective is to place the transistor in some type of circuit topology that will produce a negative resistance on its output port. Using the transistor's small signal S-parameters and with the help of a computer analysis program, several different circuit topologies were examined for the ability of inducing a negative resistance. Figure 3 shows the circuit topology finally selected. This circuit must have a large signal negative resistance magnitude less than 50 ohms so it will not oscillate when loaded by the test equipment. Remember that our purpose thus far is to design and build a non-oscillating circuit from which we can measure its negative resistance as a function of output power.

A COMPACT[4] computer program was written to maximize S_{22}' by varying transmission line lengths L_1 and L_2 (Figure 3). The minus sign in line 14 instructs the optimization program to maximize the reflection coefficient. Optimizing the circuit for maximum S_{22}' also sets the negative resistance magnitude to be equal to the load resistance (refer back to Figure 2). It was convenient to design for a negative resistance of 50 ohms. The first line of the COMPACT program specifies the open stub on the emitter with an estimated line length of 2.54 mm (0.100 inch) to be optimized. The shorted stub on the base (Figure 3) is actually composed of two parallel shorted stubs which are specified in

lines three and four. After maximizing for S_{22}', the emitter stub length was increased to 2.96mm (0.117 inch) and the base stubs to 7.86mm (0.310 inch). The circuit was constructed on 0.031 inch thick Duroid™ 5880, and is shown in Figure 4. We will come back to the circuit shortly, but for now continue with another example.

SECOND EXAMPLE

In this second example the objective is to design a medium power (1 watt) oscillator at 2.0 GHz. For this design an HXTR-4103 common collector bipolar transistor will be used[5]. This transistor is housed in a flange mounted package, the HPAC-200GB/GT. Once again a circuit topology is selected (Figure 5) and the circuit element optimized to maximize S_{22}' using the transistor's small signal S-parameters. The impedance of the open transmission line was arbitrarily picked to be 50 ohms and only the length of the transmission line optimized. This circuit was also constructed on 0.031 inch thick Rogers RT/Duroid™ 5880 and is shown in Figure 6.

DEVICE LINE METHOD

The 4.3 GHz circuit using the HXTR-4101 transistor did not oscillate into 50 ohms ; therefore, the device line method was used to measure the load impedance for oscillation. The test set-up is shown in Figure 7. Since the resistance is negative the reflection coefficient exceeds unity and the impedance lies outside the normal Smith Chart. Displaying a reflection coefficient greater than one is possible by interchanging the test and reference ports on the HP 8411A harmonic frequency converter. This inverts the reflection coefficient so that the analyzer shows the circuit impedance with the sign changed. This is exactly the impedance that must be connected to the circuit to complete the oscillator. Figure 8 shows the admittance load line measured for the circuit. The admittance of 0.26 + j0.32 corresponds with the maximum added power of the circuit which is the output power expected when the oscillator is completed.

4.3 GHz OUTPUT MATCHING NETWORK

The output matching network must transform the 50 ohm load to a normalized admittance of 0.26 +j 0.32 at point A (Figure 9). First an open shunt line is added to move the 50 ohm load to point B. A 50 ohm transmission line then rotates the admittance at point B to point A. The final 4.3 GHz oscillator circuit is shown in Figure 10. The measured output power of the oscillator agreed very well with the predicted P_{max} of 19.6 dBm (Figure 11). Figure 12 shows the phase noise for the final oscillator. This completes the design and testing of the 4.3 GHz oscillator. Now we will return to the 2 GHz oscillator.

LOAD PULL METHOD

The 2 GHz circuit using the HXTR-4103, did oscillate into 50 ohms, which prevents the use of the device line method. Re-optimizing the circuit with a load resistance lower than 50 ohms may result in a circuit that will not oscillate, but the

decision was made to use the load pull method to measure the load resistance necessary for maximum oscillator output power. Figure 13 shows the test set-up for the load pull measurement system. The output of the oscillator is connected to a sliding tuner and 50 ohm load combination. The output power of the oscillator, and the load impedance presented to the oscillator is measured as the tuner is varied. The spectrum analyzer is used to verify that the output spectrum of the oscillator is a stable single frequency before an impedance measurement is made. Figure 14 shows the optimum load impedance measured for the 2.0 GHz circuit (115 + j 70 ohms). The output network for the 2.0 GHz circuit was then designed.

2.0 GHz OUTPUT MATCHING NETWORK

The load impedance for maximum output power at 2.0 GHz is first normalized to 70 ohms and plotted as an admittance at point A (Figure 15). The output matching network must transform the 50 ohm load to a normalized admittance of .444 - j0.270 at point A. First an open shunt line is added to move the 50 ohm load to point C. A 70 ohm transmission line of 0.201 wavelength then rotates the admittance at point C to point B. The design is completed by adding another open shunt line to move the admittance at point B to point A. The PC board artwork layout forthe final oscillator is shown in Figure 16. The output power of the oscillator is typically + 30 dBm. The phase noise of the oscillator is shown in Figure 17 . This completes the design of the 2.0 GHz oscillator.

SUMMARY

The two examples given in this paper have shown that the device line and load pull methods are useful tools for the designer. The methods help bring a systematic approach to the design of oscillators in an area where empirical methods abound.

REFERENCES

1. Walter Wagner, "Oscillator Design by Device Line Measurement", Microwave Journal February 1979 pp. 43-48.

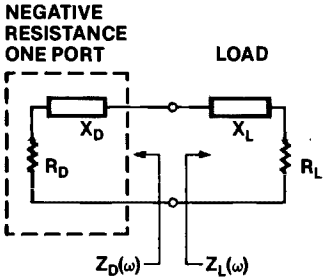
2. Dennis Poulin, "Load-Pull Measurements Help Meet Your Match", Microwaves November 1980 pp. 61-65.

3. Hewlett-Packard Application Note 975, " A 4.3 GHz Oscillator Using the HXTR-4101 Bipolar Transistor."

4. Compact Software

5. Hewlett-Packard Application Note 994, " A 2 GHz Power Oscillator Using the HXTR-4103 Bipolar Transistor."

FIGURE 1



■ START-UP CONDITION

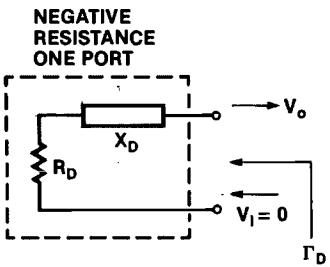
$$|R_D(\omega_o)| > R_L$$

$$\text{AND } -X_D = X_L$$

■ STEADY STATE CONDITION

$$|R_D(\omega_o)| = R_L$$

FIGURE 2



■ $\Gamma_D = \dfrac{V_o}{V_i} = \dfrac{V_o}{o} = \infty$

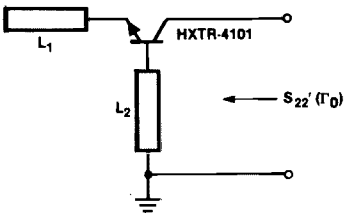
■ SINCE $\Gamma_D = \dfrac{Z_L - Z_D}{Z_L + Z_D}$

■ THEN $Z_L = -Z_D$

FIGURE 3

EXAMPLE NO. 1

COMMON BASE BIPOLAR



COMPACT PROGRAM TO MAXIMIZE S_{22}'

```
OST   AA    PA    50    -100    1.9     0      0
TWO   BB    B1    50
RET   CC    PA    50    -300    1.9     0      0
CAS   CC    CC
SER   BB    OC
CAS   AA    BB
PRI   AA    OR    50    1E9
END
4300
END
1.02    104    1.88    -142    .142    78    1.14    -109
END
.001
-100    0    0    0
END
Optimization begins with following variables and gradients
        VARIABLES                    GRADIENTS
    ( 1):   100.000              ( 1):  -26.5006
    ( 2):   300.000              ( 2):  -49.3956
ERR. F =      3.503
          ---*****---
ERR. F =       .566
ERR. F =       .003
    ( 1):   116.557              ( 1):  -.130112
    ( 2):   309.843              ( 2):  .964984E-01
ERR. F =       .000
          ---*****---
Function termination with above values  Final analysis
follows
4300.00    ****    131.9    58.18    -49.92    .00
```

FIGURE 4

TOPOLOGY OF NON-OSCILLATING CIRCUIT

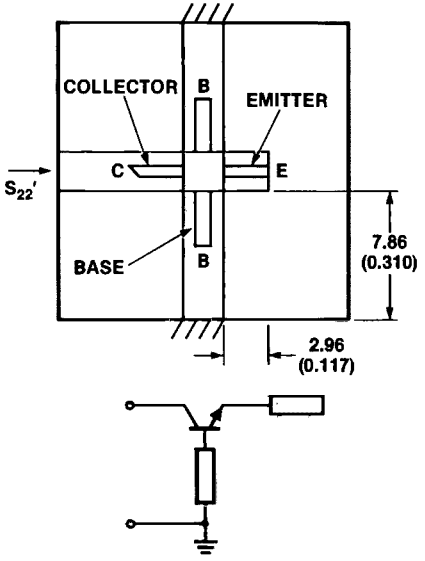
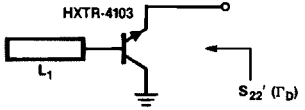


FIGURE 5

EXAMPLE NO. 2

COMMON COLLECTOR BIPOLAR



COMPACT PROGRAM TO MAXIMIZE S_{22}'

```
DST AA PR -50(20,100) -150(110,250) 1.0
TWO PR 01 50
CAY AA DR
PRI AA DR 50 10000 .0001
END
ZOOM
END
 1.014 -144.6 1.324 -108.7 .476 -24.9 .608 95.6
END
 .001
-100 0 0 0
END

OPTIMIZATION BEGINS WITH FOLLOWING VARIABLES AND GRADIENTS
     VARIABLES                    GRADIENTS
  ( 1): 50.0000                ( 1):-6.19617
  ( 2): 1500.00                ( 2):-244.662
ERR. F.=     35.250
             ****
  ( 1): 50.1295                ( 1):-.312179
  ( 2): 1745.01                ( 2):-1.72275
ERR. F.=      .044
             ****
  ( 1): 50.1347                ( 1): .246614E-01
  ( 2): 1765.50                ( 2): .4217a1
ERR. F.=      .047
             ****
GRADIENT TERMINATION WITH ABOVE VALUES. FINAL ANALYSIS FOLLOWS

 F(MHZ)    RHO(MAG.<ANGLE)          RET L/G (DB)    IIR-JX(OHM

2000.000    48.106   <166.1          33.44    -48.0C   -.48
```

FIGURE 6

TOPOLOGY OF CIRCUIT

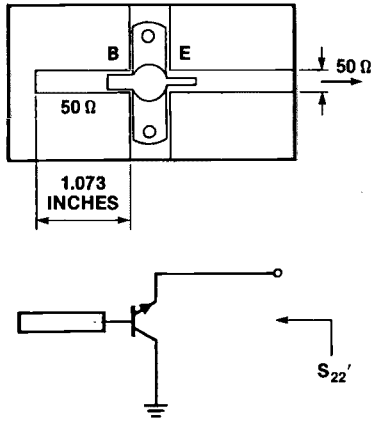


FIGURE 7

TEST SET-UP FOR NON-OSCILLATING SYSTEM

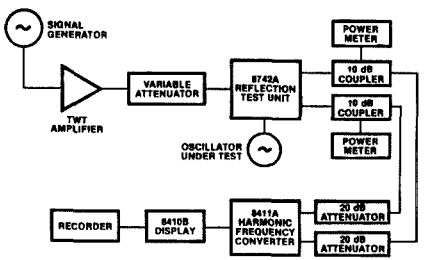


FIGURE 8

ADMITTANCE LOAD LINE

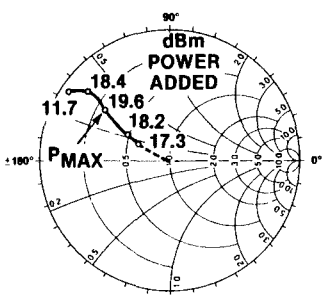


FIGURE 9

OUTPUT NETWORK DESIGN

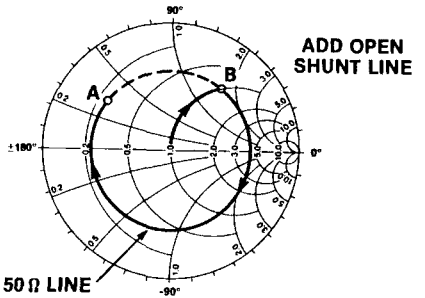


FIGURE 10

4.3 GHz FINAL OSCILLATOR CIRCUIT

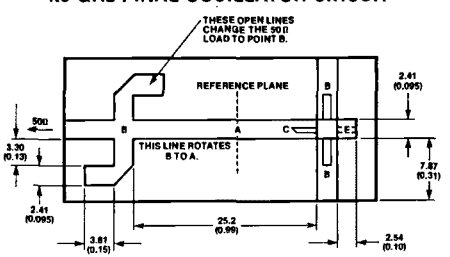


FIGURE 11

OSCILLATOR POWER CHARACTERISTIC

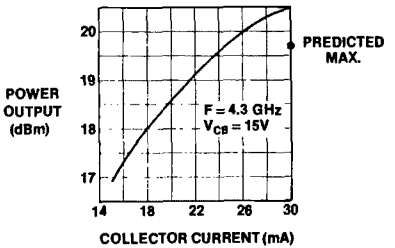


FIGURE 12

PHASE NOISE

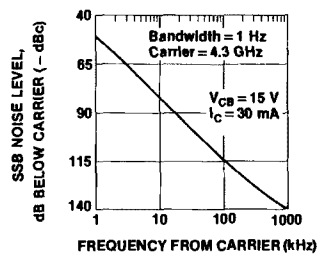


FIGURE 13

LOAD-PULL BASIC MEASUREMENT SYSTEM

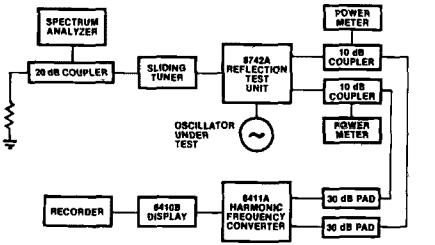
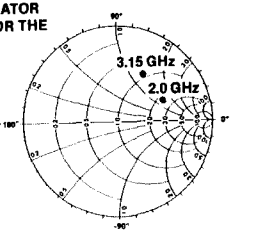


FIGURE 14

LOAD IMPEDANCE FOR MAXIMUM OSCILLATOR OUTPUT POWER FOR THE HXTR-4103



18 V
130 mA

FIGURE 15

OUTPUT NETWORK DESIGN

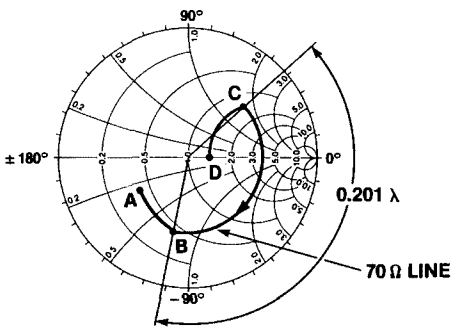


FIGURE 16

FINAL CIRCUIT TOPOLOGY FOR THE 2.0 GHz OSCILLATOR

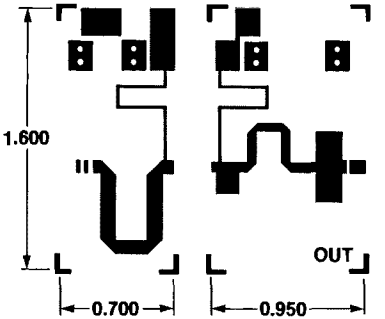
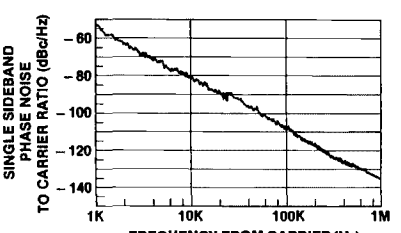


FIGURE 17

PHASE NOISE OF THE LOW Q MICROSTRIP 2.0 GHz OSCILLATOR USING THE HXTR-4103 (P_{osc} = 29.8 dBm)



PACKAGING CONSIDERATIONS FOR RF TRANSISTORS

by

Norman E. Dye

Motorola Semiconductors

INTRODUCTION

Parasitic reactances, material losses and for higher power devices thermal limitations combine to make package selection for RF transistors a technically challenging undertaking. It has been said the best RF package is NO package. And while this is understandable, it is not practical. Thus the trick is to design a package that protects the RF die, heat sinks it and makes connections to the "outside world" with minimal deleterious effects.

This paper will discuss thermal, electrical, mechanical and other considerations in the design of RF packages. Several existing packages will be described in discussing the evolution of RF packages. Finally, new approaches will be proposed to achieve packages with satisfactory characteristics at LOWER COST.

RF TRANSISTOR PACKAGE CHARACTERISTICS

Figure 1 is a summary of the primary characteristics of a package suitable for use with high power at high frequencies. Thermal and electrical requirements predominate; however, many other factors influence what can and can't be done in designing an acceptable RF package. These characteristics will be discussed in the following paragraphs.

THERMAL CONSIDERATIONS

The name of the thermal game with RF devices is to maintain die temperature below a prescribed temperature (150 degC to 200 deg C) during normal operation. For low power devices with the die mounted on the collector portion of the lead frame or on alumina oxide ceramic, this presents little difficulty for dissipations below 1/4 watt. Typical packages are shown in Figure 2. Use of a copper lead frame and modest heat sinking of the collector lead can increase the dissipation limitation to 3/4 watt. A wider, thicker collector lead results in the so-called PowerMacro package (Figure 3) which has a thermal rating of 1.5 watts.

However, where higher power dissipation is required, the RF die must be heat sunk through some medium which offers low thermal resistance while maintaining electrical isolation. The most practical material currently available offering low thermal resistance and simultaneously high electrical resistance is beryllium oxide (BeO). Figure 4 depicts the thermal properties of BeO compared with other materials. Figure 5 shows electrical resistivity of BeO along with several common insulators.

ELECTRICAL CONSIDERATIONS

Objectively, one wishes to make contact with the RF die while keeping parasitic capacitance and inductance along with conductivity losses at a minimum. Package design--location of external leads, thickness of BeO, path length from die to external lead connections and choice of plating materials allow the package designer to approach these desired results.

A key objective is to keep lead length from die to the external circuit as short as possible. Also leads (including current paths on the ceramic) must be sufficiently wide to prevent excess resistance or inductance. And most important the plating on both ceramic and leads must be low loss and sufficiently thick in skin depths to minimize series resistance to RF current flow.

OTHER CONSIDERATIONS

Other factors in addition to thermal and electrical must be considered in designing RF transistor packages. Primarily these can be grouped under "Reliability and Cost" although some may fall more conveniently under "Customer Convenience." In the latter category are items such as type of heat sink (stud or flange) and form factor (surface mount, machine insertable, stripline compatible, etc.)

Reliability, here, covers die attach, wire attach, hermeticity and lead solderability. Both die and wire attach are dependent on plating. High power die attach must have void free, low thermal resistance bonds (Silicon-Gold eutectic is the most common) to prevent thermal hot spots and these bonds can be achieved most readily with an adequate amount of smooth, pure gold (Au). Wire bonds are generally reliable whether Au on Au, Au on aluminum (Al), Al on Au or Au on copper (Cu) but if Au plating of the package is involved with Al wire, it is imperative that the plating be free of even the smallest amounts of Thallium (used sometimes in Au plating solutions to improve rate and smoothness of plating).

Hermetic packages, a representative sample of which is shown in Figure 6, have requirements contrary to those of good RF packages. The lead length through the hermetic seal is usually longer and more lossy than the length required for similar non-hermetic packages. Today, hermeticity is seldom warranted for commercial applications. Modern transistors are constructed with silicon nitride (SiN4) die passivation, Au top metal and Au wire which alleviates the need to keep moisture and foreign material from coming in contact with the die and wire bonds. However, if packages are subjected to contaminants such as those found in vapor phase soldering and subsequent flux removal solutions, gross leak hermeticity is important to prevent particles from getting inside the transistor where long term chemical action could result in premature device failure.

Lead solderability is generally thought to create no problems provided leads are covered with not less than 50 micro-inches of Au plating. But even Au can cause difficulties in soldering if sufficient time is used in soldering such that the Au plating is dissolved in the solder solution. Also, both silver (Ag) and Cu tarnish such that these material finishes are rendered useless unless the user is willing to remove the oxides just prior to solder attach (or use the parts with minimal shelf life).

Of the many "other" considerations in designing an RF package, perhaps the most important of all is COST. Metal ceramic packages represent 50% or more of the product cost for most RF transistors. The basic problem, then, is how to devise a package with suitable RF characteristics in which a transistor can be assembled without difficulty, which can be put to use at some time in the future, with high reliability, and yet be relatively low in cost.

What are the cost ingredients of RF packages? One can identify 3 major components as shown in Figure 7. These are materials (such as ceramic disc, metal heat sink and lead frame), brazing operations used to assemble the constituent pieces, and plating. Brazing is probably the least expensive of the three and since it is essential--without creating user problems in heat sinking (no heat sink on package) and/or soldering into a circuit (no leads on package)--it will not be discussed further.

Material costs particularly when using BeO can be a sizeable portion of the total package costs. Reduce the amount of BeO and you can reduce material costs. Finally there are plating costs. Since Au is a normal final plate for an RF package for the obvious reasons of good conductivity, inertness, etc., it became a prime target of cost reduction particularly when Au was selling for $600/oz. 1) Even today at $325/oz. Au adds significantly to RF package costs and efforts continue to eliminate it wherever possible.

EVOLUTION OF BASIC PACKAGE TYPES

The SOE Package

In the early 1960's as transistors began to deliver watts of power at frequencies greater than 50 MHz, a new RF power package evolved suitable for micro-strip circuit applications. It was called Stripline Opposed Emitter (SOE) after its planar lead construction with two opposing leads tied to the common element in grounded emitter amplifiers. A picture of the SOE is shown in Figure 8. The raised bridge - an integral part of the lead frame - permits both short base and emitter wires simultaneously thereby reducing parasitic reactances. Thickness of the BeO (typically 60 mils) resulted in a compromise between thermal resistance (thin BeO desired), electrical resistance (thick BeO desired), and mechanical considerations necessary for heat sink attach without fracture of the ceramic disc (thick BeO desired).

Variations of the basic SOE package have resulted in the dual emitter bond (DEB) package (Figure 9). The addition of a 2nd emitter bridge (flat) on the BeO surface allows parallel emitter wires which lowers emitter inductance leading to increased amplifier gain. By widening the flat emitter stripe, the semiconductor manufacturer can add a MOS capacitor thereby achieving the input matched package (CQ or J0) (Figure 10). Wiring the capacitor between base and emitter raises the input impedance, reduces input losses and reduces input Q. Matching inside the package close to the die is essential for higher power, higher frequency devices in which Zin and/or Zout of the die is less than 0.5 ohms. Without input matching, a device would exhibit excessive circuit losses as well as extremely narrow band characteristics.

The Isolated Collector Package

An attempt to achieve the lowest possible common element inductance resulted in the transistor die being isolated on a collector "island" completely surrounded by the common element metallization (Figure 11). Of course this requires the collector contact to be made via

1)First, Au was removed from the heat sink (flange or stud) where it served no useful purpose other than appearance. Next the Au was reduced in thickness (typically to 50 micro-inches) in all areas of the package except the die bond pad where it is essential to maintain >100 micro-inches of Au to achieve void free Si-Au eutectic bonds.

wires which can result in increased collector series inductance. Again provisions can be made for use of an input matching capacitor (Figure 12), or both input and output matching capacitors (Figure 13).

Common Emitter TO39 (CE-TO39)

Cost considerations led to the addition of BeO to a conventional TO39 package (see Figure 14) in a successful effort to reduce the cost of 1 to 4 watt driver transistors operating at frequencies through 500 MHz. Tying the emitter leads to the case and isolating electrically the collector results in high performance (>10 dB gain) amplifiers that cost in the vicinity of $1 to $2-- a substantial decrease in price from SOE packaged devices.

Common Emitter TO220 (CE-TO220)

Still the power levels above 4 watts even at frequencies as low as 50-100 MHz required the use of the expensive SOE package. This necessitated the modification of a low cost, higher power package (the TO220) such that satisfactory RF performance could be achieved at least through 175 MHz. Again the key was the use of BeO to isolate the collector and permit low inductance "grounding" of the emitter as shown in Figure 15.

Cost savings are not as substantial as in the case of TO39's. Although the basic TO220 package is lower in cost than a TO39, modifying the TO39 involves a relatively small amount of unpatterned BeO while the TO220 requires larger, patterned BeO and, generally, with "wraparound" metallization. The basic package costs of the CE-TO220 can be approximately half that of an SOE and if these savings can be maintained through subsequent assembly and final test *operations (not an easy feat to accomplish), the resulting transistor should have a sell price* $1 to $2 less than a comparable SOE packaged part.

Frequency and power limitations do exist in the TO220 package. Basically it is highly undesirable from the standpoint of parasitic lead inductance which results in the package essentially being impractical for use at power levels above 40 watts at 50 MHz, 30 watts at 200 MHz and 10 watts at 500 MHz.

NEW PACKAGE CONCEPTS

Achieving packages that still provide low thermal resistance, low parasitics, ways to heat sink and ways to access the terminals of the transistor all at LOWER COST is still the primary objective of modern day RF packaging efforts. *A novel approach at Motorola is to minimize use of* Au by using it only on the die bond pad of an essentially standard SOE package (Figure 16). Excellent electrical conductivity is still achieved by the use of a copper clad lead frame with the external leads tin plated after assembly. One major problem with this process is the necessity for package hermeticity during the lead plating operation. Also the design concept leaves the basic SOE package intact - which means the cost of patterned BeO and the cost of brazing remain essentially unchanged.

Reducing the BeO is the major thrust of another new RF package concept. Since BeO is only needed under the active transistor die, it can be reduced from a patterned disc or rectangle to a small unpatterned disc or rectangle that is substantially less costly to manufacture. One example of such a package is shown in Figure 17. Here the center disc is BeO while the outer ring is less expensive aluminum oxide (Al_2O_3). The lead frame includes a collector lead that bridges the gap between materials and covers the collector bond pad area. While the amount of BeO is minimized, other costs such as brazing and plating are left unchanged. And the extended collector lead necessitates use of a separate raised bridge (if desired).

A less expensive concept that utilizes a semiconductor manufacturer's main asset - the ability to process silicon - is shown in Figure 18. Two thick rectangles of intrinsic silicon are placed on either side of a rectangular block of unpatterned BeO. The three metallized but electrically insulating pieces are brazed to a copper flange along with two pieces of lead frame material. It is relatively simple (and inexpensive) to pattern the silicon rectangles to provide shorting bars on the sides adjacent to the BeO. Wiring, then, provides for collector and base contacts and dual emitter bonds.

SUMMARY

Packages suitable for use at RF frequencies must have low parasitics and low loss. For power transistors, the package must also have low thermal resistance from die to case. These requirements historically have resulted in RF power packages being a significant portion of the manufacturing cost of RF power transistors.

Various packages have been designed (CE-TO39, CE-TO220) in efforts to reduce package costs; however, their limitations with respect to power dissipation and parasitics make them unsuitable except in very restricted applications.

This paper has discussed the considerations necessary in RF package design and the evolution of a variety of packages suitable for use at radio frequencies. Finally, several alternate approaches to devising a LOW COST package suitable for use at both high power and high frequency have been proposed.

FIGURE 1

CHARACTERISTICS OF RF POWER PACKAGES

1. **GOOD THERMAL PROPERTIES**
2. **LOW INTERELECTRODE CAPACITANCE**
3. **LOW PARASITIC INDUCTANCE**
4. **HIGH ELECTRICAL CONDUCTIVITY**
5. **RELIABLE**
6. **LOW COST**
7. **FORM FACTOR SUITABLE FOR CUSTOMER APPLICATION**

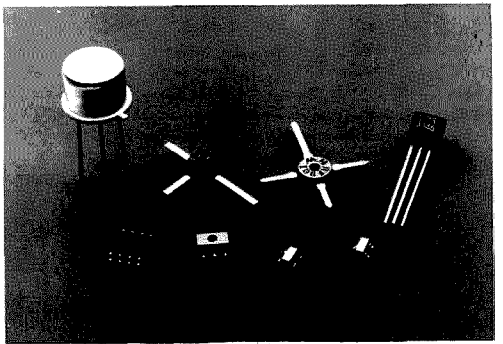


FIGURE 2–LOW POWER PACKAGES FOR RF

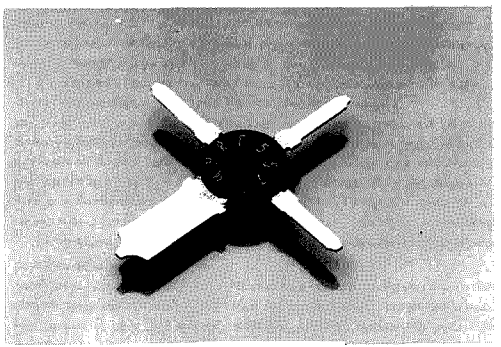


FIGURE 3–THE POWERMACRO PACKAGE

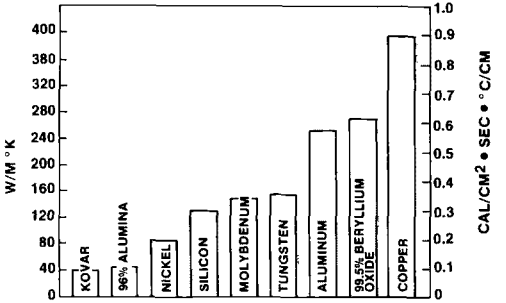


FIGURE 4–THERMAL PROPERTIES OF METALS/CERAMICS

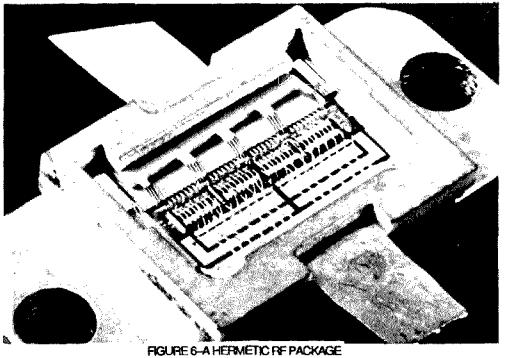


FIGURE 6–A HERMETIC RF PACKAGE

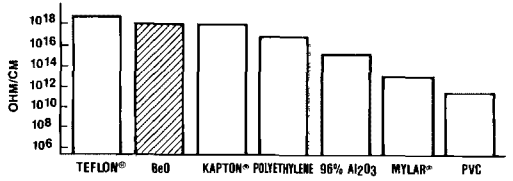


FIGURE 5–ELECTRICAL RESISTIVITY OF TYPICAL INSULATORS

X7129A

FIGURE 7

COST INGREDIENTS OF TYPICAL RF POWER PACKAGE.

MATERIAL		$0.40
BeO	$0.08	
METALLIZATION OF BeO	0.10	
FLANGE, NI PLATED	0.10	
LEAD FRAME, NI PLATED	0.12	
ASSEMBLY		0.15
FINAL PLATE		0.45
		$1.00

X7125

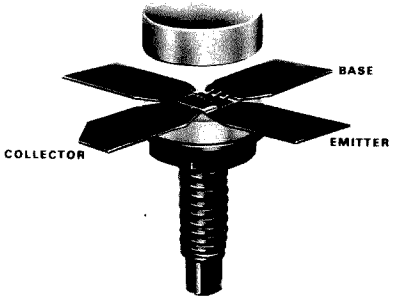


FIGURE 8–THE STRIPLINE OPPOSED EMITTER PACKAGE

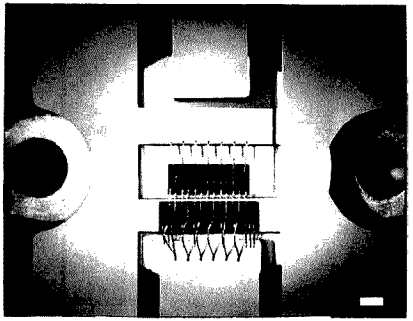


FIGURE 10–THE INPUT MATCHED PACKAGE

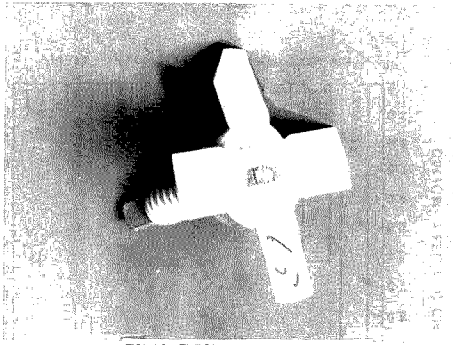


FIGURE 9–THE DUAL EMITTER BOND PACKAGE

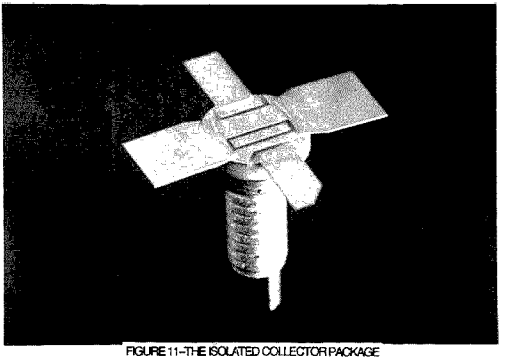


FIGURE 11–THE ISOLATED COLLECTOR PACKAGE

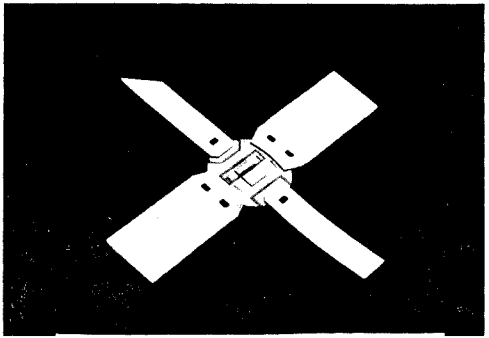


FIGURE 12–AN ISOLATED COLLECTOR PACKAGE WITH INTERNAL MATCHING

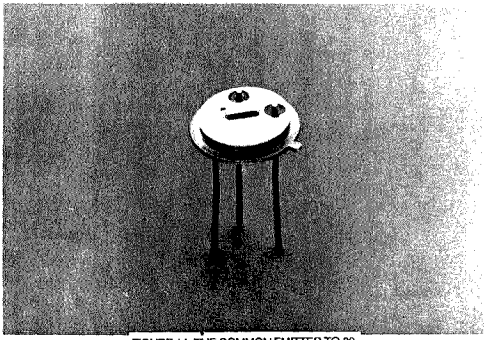


FIGURE 14–THE COMMON EMITTER TO-39

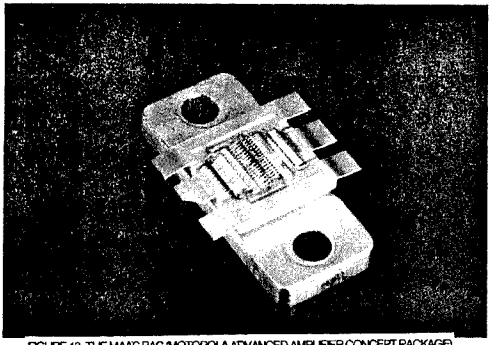


FIGURE 13–THE MAAC PAC (MOTOROLA ADVANCED AMPLIFIER CONCEPT PACKAGE)

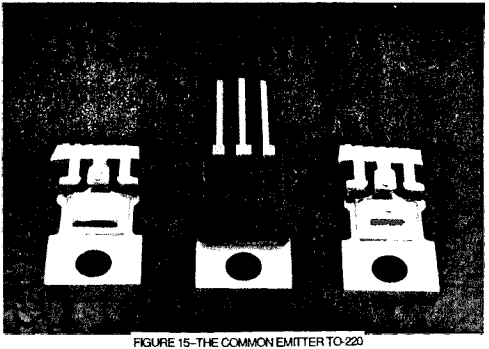


FIGURE 15–THE COMMON EMITTER TO-220

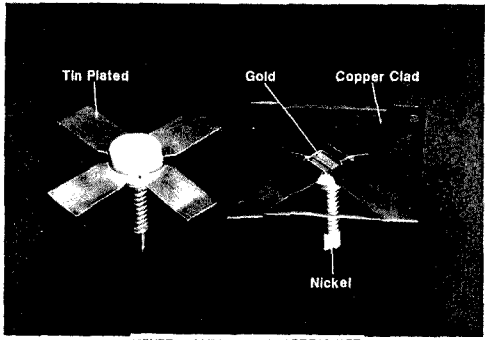


FIGURE 16–A MINIMUM GOLD SOE PACKAGE

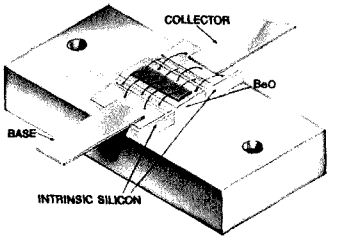


FIGURE 18–A NEW PACKAGE CONCEPT

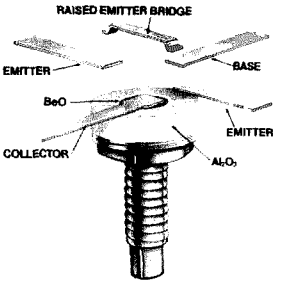


FIGURE 17–A MINIMUM BEO SOE PACKAGE CONCEPT

MICROSTRIP MINIATURE TRANSFER SWITCH

by

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ABSTRACT

A microstrip transfer PIN switch has been developed for the 675 MHz digital microwave system of Indian Telephone Industries Limited, Bangalore. It uses lumped elements to provide 90° electrical length between two diodes which is required to increase isolation. An isolation of more than 50 dB is obtained at two isolated ports in the 600 to 750 MHz frequency band with a minimum of 15 dB return loss at all the four ports. The maximum insertion loss obtained in the band is 0.8 dB. The switch is TTL compatible and has replaced the bulky, coaxial switch which used relays.

INTRODUCTION

Transfer switches are required to switch two transmission lines betaween the antenna and load Z_o. The configuration of a transfer switch using PIN diodes is shown in Fig.(1). When the control voltages V_{c1} and V_{c2} are positive and zero respectively, only the diodes D_1 and D_3 conduct and lines (1) and (2) get connected to the antenna and load Z_o respectively. When the control voltages V_{c1} and V_{c2} ae zero and positive respectively, only the diodes D_2 and D_4 conduct and line (1) gets connected to the load Z_o and line (2) gets connected to the antenna. First, a switch was developed with only one diode in each path and then a switch with two diodes in each path separated by an electrical length of 90° made of lumped elements was developed. The development of these switches will be discussed in the following sections.

Microstrip Transfer Switch with One Diode in Each Path:

The configuration of the microstrip transfer switch with one diode in each path is shown in Fig. (2). The switch was developed on 1/32" thick Teflon fiberglass substrate (ϵ_r=2.54) using HP 5082 - 3001 glass package PIN diodes. The high frequency chip capacitors were used for DC blocking. Air-core coil inductors were used for RF to DC isolation. The measured performance of the switch is shown in Fig. (3). The minimum return loss obtained is 22.0 dB. The isolation at port No.3 has decreased from 29.0 dB to 26.5 dB over the 600 to 750 MHz frequency band. The minimum isolation obtained at port No.4 is 34.5 dB. The isolation at port No. 3 is about 6 dB less than that of the Isolation at port No.4. This is because the two signals add in phase at port No.3. The maximum insertion loss obtained is 0.5 dB.

Microstrip Transfer Switch with Two Diodes in Each Path:

The isolation is expected to increase when two similar

diodes separated by a quarterwave transmission line are used in each path instead of one diode. At the frequency at which the electrical length between the diodes is exactly 90^0, the isolation will be double that offered by a single diode. The dimensions of the switch become too large if the distributed quarterwave lines are used because the length of a quarter wave line on 1/32" thick Teflon fiberglass (ϵ_r=2.54) is approx. 7.5 cm. The equivalent T- or π - section lumped element networks are very convenient in such applications.

The element values of the T-equivalent lumped circuit calculated using the equations:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}, \quad Z_0 = \sqrt{\frac{L}{C}}$$

where f_0 = 675 MHz, Z_0 = 50 Ω

are L = 11.789 nH, C = 4.715 pF

The air-core coil inductors were characterized by making them resonate in series with the chip capacitors. Johanson thin film variable capacitors were used as shunt capacitors. These capacitors were tuned so that a T-equivalent network consisting of L's and C offered a 90^0 electrical length at 675 MHz. The electrical lengths measured at the band edges (at 600 and 750 MHz) are approximately 77^0 and 105^0. The switch circuit is shown in Fig. (4). A photograph of the unit is shown in Fig.(6).

The measured performance of the switch is shown in Fig.(5). It can be seen that a minimum return loss of 15 dB is obtained over the required frequency band and is maximum ($\simeq$ 32 dB) around 700 MHz. The minimum isolation obtained is 50 dB. The maximum insertion loss is 0.8 dB. Almost similar results were obtained when the ports (2), (3) and (4) were taken as input ports. The increase in the insertion loss from 0.5 dB to 0.8 dB in the frequency band can be attributed to the lead inductances of the diodes. The computed results obtained taking the forward diode resistance as 1 ohm and the reverse junction capacitance as 0.2 pF are as follows: The return loss is more than 17 dB and isolation is more than 50 dB.

The microstrip transfer PIN switch with lumped elements has given good results over a frequency bandwidth of 22% (600 to 750 MHz). The switch being a planar circuit can be easily integrated with other subsystems.

ACKNOWLEDGEMENT

The authors wish to record their thanks to management of M/S Indian Telephone Industries Limited, Bangalore for kind permission to publish this paper.

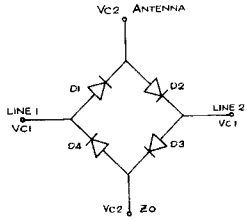


FIG. 1. TRANSFER SWITCH

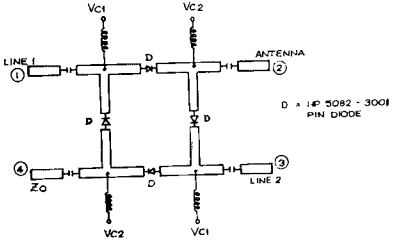
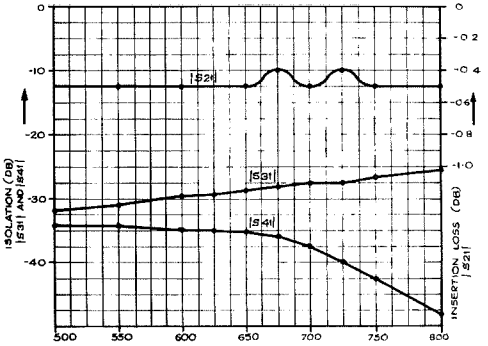
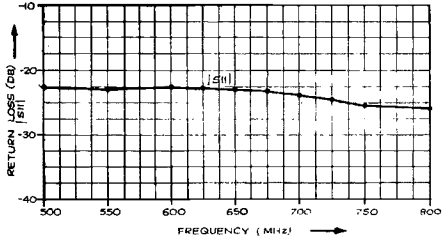


FIG. 2. MICROSTRIP TRANSFER SWITCH WITH ONE DIODE IN EACH PATH

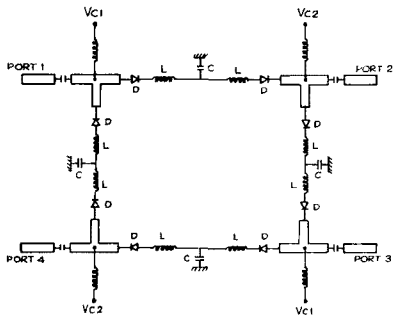


a) ISOLATION AND INSERTION LOSS



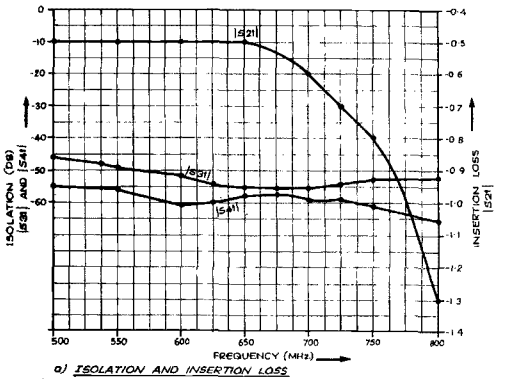
b) RETURN LOSS

FIG. 3. RESULTS OF THE MICROSTRIP TRANSFER SWITCH WITH ONE DIODE IN EACH PATH.

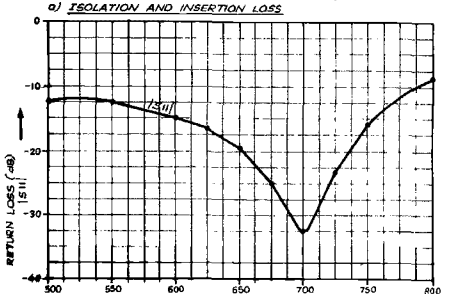


L = 11.79 nH
C = 4.715 PF
D = HP 5082 - 3001
PIN DIODE

FIG. 4. MICROSTRIP TRANSFER SWITCH WITH TWO DIODES IN EACH PATH



a) ISOLATION AND INSERTION LOSS



b) RETURN LOSS

FIG. 5. RESULTS OF THE MICROSTRIP TRANSFER SWITCH WITH TWO DIODES IN EACH PATH.

MATHEMATICS OF THE LINVILL STABILITY CRITERIA

by

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For the power transistor, the 'Y' parameters at various frequencies are known. The device input admittance and the output admittance are complex. The transistor may not be stable at some frequencies or loadings. The RF designer is interested in finding circuitry and loading which will produce stability. He looks first at the output. Finding this he then determines the input network. For the mathematics to be used the following circuit model will be used.

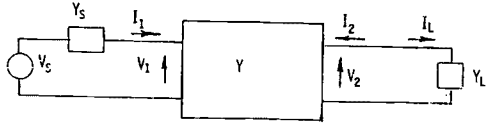


Figure 1, 'Y' Parameter Transistor Circuit

A technique the designer may use to select the the output circuit is the mathematics of Linvill. The output power from the device is described by a parabaloid of revolution. The power input to the device is described by an inclined surface, the input power plane. This inclined plane intersects the parabaloid of revolution. The slope and angles of orientation are dependent upon both device parameters and the output loading.

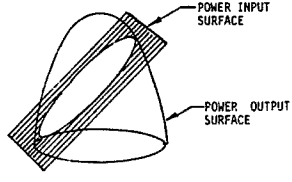


Figure 2, Power Input and Output Surfaces

The parabolic power surface of revolution rests on the LM plane. This LM plane is a Smith chart rotated 180 degrees. The axis of the paraboloid of revolution is perpendicular to the LM plane. The intersection of the LM plane and the paraboloid is a circle of unit radius.

The center of the circle is at L=1 and M=0. Recapping, P_o and P_{in} is represented in a three-dimensional coordinate system whose axes are L, M, and P (power). The LM plane represents the zero power output reference.

$$P_o = R_e \ (V_2 \ I_L^*)$$

$$P_o = \frac{L \ |Y_{21}|^2}{2 R_e Y_{22}} - \frac{(L^2 + M^2) \ |Y_{21}|^2}{4 R_e Y_{22}}$$

From the above equation the power is also zero if L = 2 and M = 0; or if L = 1 and M = 1. And also is if L = 1 and M = 1; and is if L = 1 and M = -1. The result of the intersection of the paraboloid and the LM plane is a circle of unit radius in the LM plane. The center of the circle is at L = 1, M = 0.

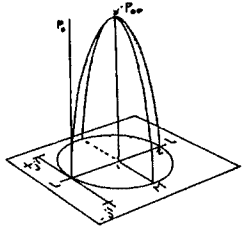


Figure 3, Sketch of Power Output as a Function of L and M.

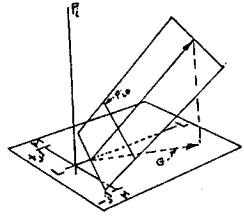


Figure 4, Sketch of Power Input as a Function of L and M.

Consider a property of the LM plane following from the fact,

$$V_2 = - \frac{y_{21}}{y_{22} + Y_L} = - \frac{y_{21}}{2R_e \ y_{22}} (L + jM)$$

and

$$Y_L + y_{22} = \frac{2 R_e \ y_{22}}{L + j M}$$

Any point in the LM plane represents an admittance whose value is related to $Y_L + y_{22}$. If y_{22} of the active device is known then the load admittance Y_L can be calculated. The expression for $Y_L + y_{22}$ can be rationalized to give real and imaginary parts. Using the Smith chart overlay, it should be remembered that any immittance chosen from it is a sum, L_L and y_{22}. In finding Y_L values, a conversion from the readings taken from the Smith chart must be done.

CONDUCTANCE READ FROM THE SMITH CHART

$$g_c = \frac{\mathrm{Re}\,(Y_L)}{g_{22}}$$

SUSCEPTANCE READ FROM THE SMITH CHART

$$b_c = \frac{\pm\,\mathrm{Im}\,(Y_L)}{g_{22}}$$

These results will be used later after the Linvill charts are plotted.

The following are equations that will be used to prepare tho Linvill chart.

GRADIENT LINE ANGLE, θ

$$\theta = \tan^{-1} \frac{I_m\,(y_{12}\,y_{21})}{-R_e\,(y_{12}\,y_{21})}$$

STABILITY FACTOR, C

(Less than one, unconditionally stable)

$$C = \frac{\left|y_{12}\;y_{21}\right|}{2\,g_{11}\,g_{22} - R_e\,(y_{12}\,y_{21})}$$

GAIN AT MAXIMUM POWER OUTPUT, G_{oo}

$$G_{oo} = \frac{C}{2}\left|\frac{y_{21}}{y_{12}}\right| \quad (\text{In dB} = 10 \log G_{oo})$$

MAXIMUM GAIN, G_{MAX}

(Available power gain)

$$G_{MAX} = K_g\,G_{oo}$$

$$K_g = 2\left[\frac{1 - \sqrt{1 - C^2}}{C^2}\right]$$

GAIN CIRCLE DATA

GAIN RATIO

$$g = \frac{G}{G_{oo}}$$

DISTANCE TO CENTER OF GAIN CIRCLE, FROM LINVILL CHART CENTER, ALONG GRADIENT LINE

$$d = -g\,\frac{C}{2}$$

RADIUS OF GAIN CIRCLE

(Radius of Linvill chart is unity)

$$r = \sqrt{1 - g + \frac{C_g^{\,2}}{2}}$$

CALCULATOR PROGRAM, HP 15c Linvill Gradient Line Angle. O

and Stability Factor, C

REG	VALUE	TRIAL NUMBERS
1	g_{11}	17.2
2	b_{11}	11.6
3	g_{12}	0
4	b_{12}	-0.64
5	g_{21}	32.2
6	b_{21}	-63.1
7	g_{22}	0.27
8	b_{22}	1.89
9	g_{result}	-40.38
.0	b_{result}	-20.6
.1	$y_{12}y_{21}$	45.338
.2	0	-27.03
.3	C	0.9127

LINE	KEYCODE	KEYS	VALUE
001	42,21,11	f LBL A	
002	45 3	RCL 3	g_{12}
003	45 4	RCL 4	b_{12}
004	42 25	f I	y_{12}
005	45 5	RCL 5	g_{21}
006	45 6	RCL 6	b_{21}
007	42 25	f I	y_{21}
008	20	x	$y_{12}y_{21}$

Gradient Line Angle and Stability Factor Program, continued

LINE	KEYCODE	KEYS	VALUE
009	44 9	STO 9	STORE g_r
010	42 30	f Re≷Im	
011	44 .0	STO .0	STORE b_r
012	42 30	f Re≷Im	
013	43 1	g →P	$\lvert y_{12}\,y_{21}\rvert$
014	44 .1	STO .1	
015	43, 5, 8	g CF 8	CLEAR COMPLEX MODE
016	45 .0	RCL .0	Im ($y_{12}\,y_{21}$)
017	45 9	RCL 9	Re ($y_{12}\,y_{21}$)
018	- 18	CHS	-Re ($y_{12}\,y_{21}$)
019	10	÷	Im ($y_{12}\,y_{21}$)/-Re ($y_{12}\,y_{21}$)
020	43 25	g $\tan^{-1}$	$\tan^{-1}$(Re($y_{12}\,y_{21}$)/-Re($y_{12}\,y_{21}$))
021	44 .2	STO .2	ϕ
022	2	2	2
023	45 1	RCL 1	g_{11}
024	20	x	$2g_{11}$
025	45 7	RCL 7	g_{22}
026	20	x	$2g_{11}\,g_{22}$
027	45 9	RCL 9	Re ($y_{12}\,y_{21}$)
028	30	-	$2\,g_{11}\,g_{22}$ - Re ($y_{12}\,y_{21}$)
029	45 .1	RCL .1	$\lvert y_{12}\,y_{21}\rvert$
030	34	x≷y	$2g_{11}\,g_{22}$ - Re ($y_{12}\,y_{21}$)
031	10	÷	$\lvert y_{12}\,y_{21}\rvert$/ ($2\,g_{11}\,g_{22}$ - Re ($y_{12}y_{21}$))
032	44 .3	STO .3	C
033		g RTN	PROGRAM END

The preceding complex arithmetic program calculates both the stability factor and the gradient line angle by the Linvill technique. The HP 15c has two parallel stacks for number manipulation. The first parallel stack contains the real part of the complex number; the second stack contains the imaginary part of the complex number. Once the complex numbers are loaded into the stack, the complex arithmetic follows as if you were carrying out ordinary arithmetic operations.

Between lines 002 and 007 the parameters for y_{12} and y_{21} are loaded into the stack. The complex product $y_{12}\ y_{21}$ is taken at line 008. The real and imaginary parts of this product are stored in registers 9 and .0 The real and imaginary parts of $y_{12}\ y_{21}$ are recalled, divided, and the gradient line angle, ϕ calculated. This is at lines 016 through 020. The factors for the calculation of the stability factor, C are recalled and operated on. This is in lines 022 through 031. Finally the result, C is stored in register .3

CALCULATOR PROGRAM FOR THE GAIN AT MAXIMUM POWER OUTPUT, P_{oo}

This program gives G_{oo} in dB. This is the power level of the gain circle that passes through the LM plane at L = 1 and M = 0, (the center of the Smith chart). The values of the transistor 'y' parameters must be in the memory stack; and program 'A' must have been run, so that 'C' is stored in reg .3

Maximum Power Output, P_{oo} program

LINE	KEYCODE	KEYS	VALUE
172	42,21,14	f LBL 0	
173	45 5	RCL 5	g_{21}
174	45 8	RCL 8	b_{21}
175	42 25	I	MOVE TO COMPLEX STACK
176	45 3	RCL 3	g_{12}
177	45 4	RCL 4	b_{12}
178	42 25	I	MOVE TO COMPLEX STACK
179	10	÷	y_{21}/y_{12}
180	43 1	→P	$\lvert y_{21}/y_{12}\rvert$
181	43, 5, 8	CF 8	CLEAR COMPLEX FUNCTION
182	45 .3	RCL .3	C
183	20	X	
184	2	2	
185	10	÷	$\frac{C}{2}\left\lvert\frac{y_{21}}{y_{12}}\right\rvert$

186	43 13	g LOG	
187	1	1	
188	0	0	
189	20	X	
190	43 32	RTN	G_{oo} in dB

TRANSISTOR 'y' PARAMETERS, FOR SAMPLE CALCULATION

y_{11} = 17.2 + j 11.6 m mhos

y_{12} = 0 - j 0.64 m mhos

y_{21} = 32.2 - j 63.1 m mhos

y_{22} = 0.27 + j 1.89 m mhos

GRADIENT LINE ANGLE

θ = -27.03 DEG

GAIN AT MAXIMUM POWER OUTPUT

G_{oo} = 17.03 dB

STABILITY FACTOR

C = 0.9127

MAXIMUM GAIN

G_{MAX} = 19.374 dB

SAMPLE CALCULATION OF MAXIMUM GAIN

$$K_g = 2\left[\frac{1 - \sqrt{1 - C^2}}{C^2}\right]$$

Where C + 0.9127

K_g = 1.41982

$G_{MAX} = K_g G_{oo}$

Where G = 50.5159

G_{MAX} = 1.41982 X 50.5159

G_{MAX} = 71.7234

$G_{MAX_{dB}}$ = 10 LOG 71.7234

$G_{MAX_{dB}}$ = 18.5566 dB

This gain point on the paraboloid of revolution is the point where the input plane, so oriented, just touches the paraboloid.

CALCULATION OF GAIN CIRCLE DATA

GAIN RATIO 'g'	GAIN RATIO IN dB 'g_{dB}'	DISTANCE TO CENTER 'd'	RADIUS OF GAIN CIRCLE 'r'
1.41982	1.522 dB	-0.6479	.00693
1.25893	1.0	-0.574546	.266783
1.0	0	-.456376	.456376
0.707	-1.5	-.322658	.630165

The distance is measured from the point L = 1, M = 0 (The center of the Smith chart). A measurement from this central point to the edge of the chart is 3.57 inches. The above values of distance and radius are in relation to unity. These must be converted by a ratio of one to 3.57 This is so that the distances may be made directly on the Smith chart. Sample calculation,

$$\frac{d_{in}}{3.57} = \frac{-.6479}{1} \quad ; \quad d_{inches} = 2.306 \text{ in}$$

DISTANCES IN INCHES FOR DIRECT TRANSFER TO THE SMITH CHART

GAIN RATIO	GAIN RATIO dB	$G_{OO}+g_{dB}$	DISTANCE TO CENTER OF GAIN CIRCLE IN INCHES	RADIUS OF GAIN CIRCLE IN INCHES
1.41982	1.522	18.55	-2.306 IN	0.02467
1.25893	1.0	18.03	-2.04538	0.949747
1.0	0	17.03	-1.62470	1.62470
0.707	-1.5	15.53	-1.14866	2.24339

Remember, the gradient line angle, -27.03; and using these above values of distance and radius, draw the Linvill chart.

LINVILL CHART

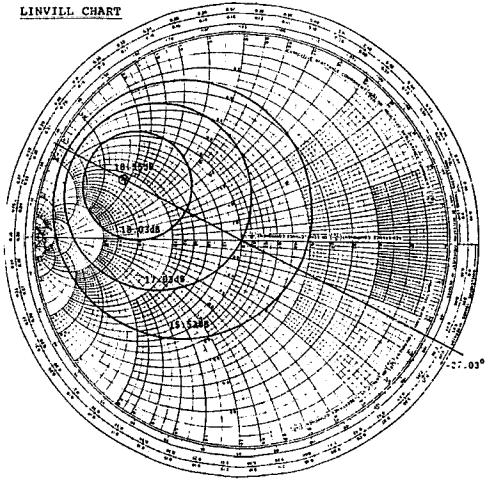


Figure 5, Linvill Chart

The Linvill chart has been drawn from the 'y' parameters. These parameters were selected for the sample calculation. The LM plane of the power output graph has a correspondence to a Smith chart rotated 180 degrees. Points on this chart have a relation to the output load to be selected for the transistor. This output load may be selected from any point in the LM plane. But for this demonstration select a LM point under the maximum gain point. A G_{MAX} of 18.55 dB is read. Reading from the Smith chart, the conductance is 2.2, and the susceptance is -2.2 These are related to the output load and the transistor reactance by the following,

$$G_L = 2.2 \times g_{22} = 2.2\ (0.27\ ) = 0.594 \text{ m mho}$$

$$B_L = -2.2 \times g_{22} - b_{22} = -2.2\ (\ 0.27\ ) - 1.89 = -2.484 \text{ m mho}$$

OUTPUT LOAD FOR G_{MAX}

$$Y_L = G_L + j\,B_L = 0.594 - j\ 2.48 \text{ m mho}$$

THE INPUT MATCHING CIRCUIT

Previously defined 'y' parameters, at 200 mHz

y_{11} = 17.2 + j 11.6 m mho

y_{12} = 0 - j 0.64 m mho

y_{21} = 32.2 - j 63.1 m mho

y_{22} = 0.27 + j 1.89 m mho

and Y_L has been selected, 0.594 - j 2.48

Substitute these values into the following equation,

$$y_{in} = y_{11} - \frac{y_{12}\, y_{21}}{y_{22} + Y_L}$$

(On the HP 15c, run GSB 1; Note y_{11} through y_{22} must be entered in registers 1 through 8. Y_L must be in reg .9 & .0)

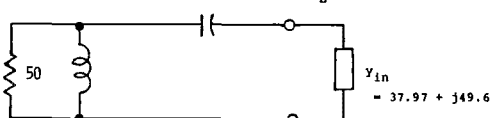


Figure 6, Input Matching Network

A matching circuit is developed by starting with the admittance Y_{in}, and working leftwards to obtain a 50 ohm termination. First the input admittance, 37.97 + j 49.6 m mho is not a normalized admittance. It must be divided through by a reciprocal 50 ohms. This is equivalent to a division by 20×10^{-3}. The normalized value is 1.898 + j 2.482 This normalized admittance can now be placed directly on the Smith chart. The normalized impedance and admittance coordinates Smith chart is best used here. The impedance values are on the orange lines; and the admittance values are on the green lines. Looking through from the green lines to the orange, transforms from admittance to impedance. Move counter-clockwise from -j 0.255, along a constant impedance circle, and arrive at -j 0.395 on the normalized 50 ohm circle. The difference of these two gives the normalized reactance the input impedance must first see. (-j 0.395 - (-j 0.255)) = -j0.14 It is normalized, so it must be multiplied by 50 to obtain the reactance.

$$\begin{array}{r} -j\ 0.14 \\ \times 50 \\ \hline -j\ 7.0 \end{array}$$

$$X_c = -7.0 = \frac{1}{2\pi fC} \; ; \quad C = \frac{1}{7.0\ (\ 2 \times 3.14 \times 200 \times 10^6)}$$

$$C = 113.68\ pF$$

The impedance of the circuit is at this point parallel to the input impedance. Therefore conversion is now made to admittance, the green lines.

We are at the point, 1 + j 2.05 admittance. Moving along the constant admittance circle to one, takes us in a negative admittance direction. Therefore the value is inductive. This distance is -j 2.05 Multiply by 20×10^{-3} (reciprocal 50 ohms).

$$2.05 \times 20 \times 10^{-3} = 41.0 \times 10^{-3} \text{ mho}$$

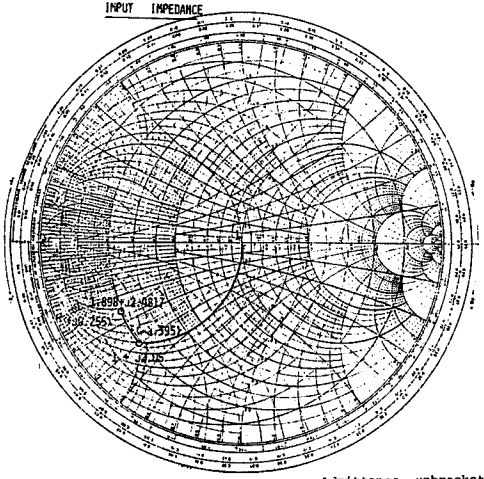
Take the reciprocal to get it into a reactance value (reciprocal of mho).

$$X_L = 24.39$$

$$X_L = 2\pi fL$$

$$L = \frac{24.39}{2 \times 3.14 \times 200 \times 10^6}$$

$$L = 0.0194089 \text{ micro henry}$$



Admittance, unbracketed

Impedance, bracketed

Figure 7, Input Impedances

CALCULATOR PROGRAM FOR INPUT IMPEDANCE

$$Y_{in} = Y_{11} - \frac{Y_{12}\,Y_{21}}{Y_{22} + Y_L}$$

(equation obtained when the 'y' parameter model was first defined.)

To run - GSB 1; (to go to a line GTO CHS 191)

(Note this program will eliminate any previously calculated values of ~~0~~ and C obtained in program 'A'.)

REG	PARAMETER	
1	Re Y_{11}	17.2
2	Im Y_{11}	11.6
3	Re Y_{12}	0
4	Im Y_{12}	-0.64
5	Re Y_{21}	32.2
6	Im Y_{21}	-63.1
7	Re Y_{22}	0.27
8	Im Y_{22}	1.69
9	Re Y_L	0.594
.0	Im Y_L	-2.48
.1	Re $(Y_{22} + Y_L)$	0.864
.2	Im $(Y_{22} + Y_L)$	-0.590
.3	Re Y_{IN}	37.96
.4	Im Y_{IN}	49.634

CALCULATOR PROGRAM,

FOR INPUT IMPEDANCE

(Continued)

191	42,21, 1	LBL 1		
192	45 7	RCL 7	g_{22}	0.27
193	45 8	RCL 8	b_{22}	1.89
194	42 25	f 1	y_{22}	0.27
195	45 9	RCL 9	G_{Y_L}	0.594
196	45 .0	RCL .0	B_{Y_L}	-2.48
197	42 25	f 1	Y_L	0.594
198	40	+	$Y_{22} + Y_L$	0.864
199	44 .1	STO .1	Re $(Y_{22}+Y_L)$	0.864
200	42 30	f Re≷Im		-0.59
201	44 .2	STO .2	Im $(Y_{22}+Y_L)$	-0.59
202	42 30	f Re≷Im	$Y_{22} + Y_L$	0.864
203	45 3	RCL 3	g_{12}	0
204	45 4	RCL 4	b_{12}	-0.64
205	42 25	f 1	y_{12}	0
206	45 5	RCL 5	g_{21}	32.2
207	45 6	RCL 6	b_{21}	-63.1
208	42 25	1	y_{21}	32.2
209	20	X	$Y_{12} Y_{21}$	-40.38 -320.606
210	45 .1	RCL .1	Re $(Y_{22} + Y_L)$	0.864
211	45 .2	RCL .2	Im $(Y_{22} + Y_L)$	-0.59
212	42 25	f 1	$Y_{22} + Y_L$	0.864
213	10	÷	$y_{12}y_{21}/(y_{22}+Y_L)$	-20.7-j38.0
214	45 1	RCL 1	g_{11}	17.2
215	45 2	RCL 2	b_{11}	11.6
216	42 25	f 1	y_{11}	17.2
217	34	X≷Y	$y_{12}y_{21}/(y_{22}+Y_L)$	-20.7-j38.0
218	30	-		37.9+j49.63
219	44 .3	STO .3	Re Y_{in}	37.968
220	42 30	f Re≷Im		49.634
221	44 .4	STO .4	Im Y_{in}	49.6340
222	42 30	f Re≷Im	Y_{in}	37.96+j49.634
223	43 32	RTN		

THE CIRCUIT

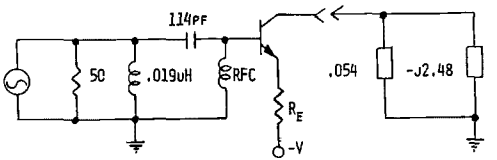


Figure 8, Transistor Matching Circuit

It is assumed that the output circuits can be developed with the normalized impedance and admittance Smith chart. This is the chart used to develop the input circuits.

PARAMETER CONVERSION

$$Y_{11} = \frac{(1 + s_{22})\ (1 - s_{11})\ + s_{12}\, s_{21}}{(1 + s_{11})\ (1 + s_{22})\ - s_{12}\, s_{21}}$$

$$Y_{12} = \frac{-2\, s_{12}}{(1 + s_{11})\ (1 + s_{22})\ - s_{12}\, s_{21}}$$

$$Y_{21} = \frac{-2\, s_{21}}{(1 + s_{11})\ (1 + s_{22})\ - s_{12}\, s_{21}}$$

$$Y_{22} = \frac{(1 + s_{11})\ (1 - s_{22})\ + s_{12}\, s_{21}}{(1 + s_{22})\ (1 + s_{11})\ - s_{12}\, s_{21}}$$

With these equations, parameters measured in 's' parameters can be converted to the admittance 'y' parameters.

CALCULATOR PROGRAM, HP15c, PARAMETER CONVERSION 's' TO 'y'

0	S_{11} R	.13548	.2395
1	S_{11} I	-.54337	.9606
2	S_{12} R	.0064279	.001730
3	S_{12} I	.00766043	-.001066
4	S_{21} R	-1.3339	-.06387
5	S_{21} I	3.6648	3.049
6	S_{22} R	.60211	.06957
7	S_{22} I	-.37624	.884
8	DEMO R	1.65	$(1+S_{11})(1+S_{22})-S_{12}S_{21}$ (R)
9	DEMO. I	-1.3	(I)
.0	$S_{12}S_{21}$ R	-36.648×10^{-3}	
.1	$S_{12}S_{21}$ I	$13,339 \times 10^{-3}$	

'a' TO 'y' CONVERSION, continued

071	42,21,15	LBL E	
072	45 2	RCL 2	
073	45 3	RCL 3	
074	42 25	f I	
075	45 4	RCL 4	
076	45 5	RCL 5	
077	42 25	f I	
078	20	X	
079	44 .0	STO .0	
080	42 30	f Re≷Im	
081	44 .1	STO .1	
082	1	1	
083	45 0	RCL 0	
084	45 1	RCL 1	
085	42 25	f I	
086	40	+	
087	1	1	
088	45 6	RCL 6	
089	45 7	RCL 7	
090	42 25	f I	
091	40	+	
092	20	X	
093	45 .0	RCL .0	
094	45 .1	RCL .1	
095	42 25	f I	
096	30	-	
097	44 8	STO 8	
098	42 30	f Re≷Im	
099	44 9	STO 9	
100	42 30	R f I	
101	1	1	
102	45 6	RCL 6	
103	45 7	RCL 7	
104	42 25	f I	S_{22}
105	40	+	$(1 + S_{22})$
106	1	1	
107	45 0	RCL 0	
108	45 1	RCL 1	
109	42 25	f I	
110	30	-	
111	20	X	
112	45 .0	RCL .0	$S_{12}S_{21}$
113	45 .1	RCL .1	
114	42 25	f I	
115	40	+	
116	45 8	RCL 8	
117	45 9	RCL 9	
118	42 25	f I	
119	10	÷	
120	44 .2	STO .2	
121	42 30	f Re≷Im	
122	44 .3	STO .3	
123	2	2	
124	16	CHS	
125	45 2	RCL 2	

'a' TO 'y' CONVERSION, continued

126	45 3	RCL 3
127	42 25	f I
128	20	X
129	45 8	RCL 8
130	45 9	RCL 9
131	42 25	I
132	10	÷
133	44 .0	STO .4
134	42 30	R I
135	44 .5	STO .5
136	2	2
137	16	CHS
138	45 4	RCL 4
139	45 5	RCL 5
140	42 25	I
141	20	X
142	45 8	RCL 8
143	45 9	RCL 9
144	42 25	I
145	10	÷
146	44 .6	STO .6
147	42 30	R I
148	44 .7	STO .7
149	1	1
150	45 0	RCL 0
151	45 1	RCL 1

152	42 25	I
153	40	+
154	1	1
155	45	RCL 6
156	45	7
157	42 25	I
158	30	−
159	20	X
160	45 .0	RCL .0
161	45 .1	RCL .1
162	42 25	I
163	40	+
164	45 8	RCL 8
165	45 9	RCL 9
166	42 25	I
167	10	÷
168	44 .8	STO .8
169	42 30	R I
170	44 .9	STO .9
171	43 32	RTN

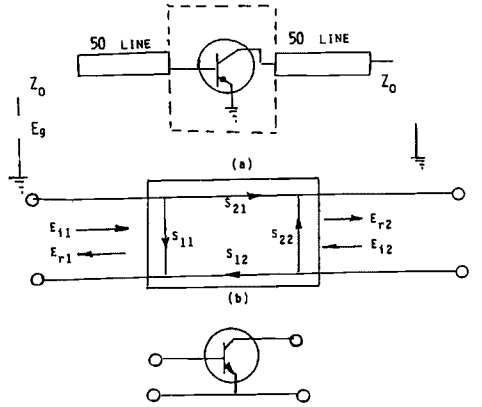


Figure 9, Block Diagram of a Typical 's' Parameter Measurement system

COMMON EMITTER

$s_{11} = s_{ie}$

$s_{21} = s_{fe}$

$s_{22} = s_{oe}$

$s_{12} = s_{re}$

$$s_{11} = \left.\frac{E_{r1}}{E_{i1}}\right|_{E_{i2}=0} \qquad s_{22} = \left.\frac{E_{r2}}{E_{i2}}\right|_{E_{i1}=0}$$

$$s_{21} = \left.\frac{E_{r2}}{E_{i1}}\right|_{E_{i1}=0} \qquad s_{12} = \left.\frac{E_{r1}}{E_{i2}}\right|_{E_{i1}=0}$$

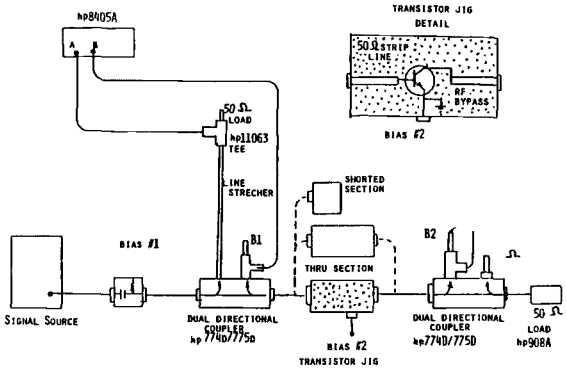


Figure 10, Block Diagram of a Typical 'a' Parameter Measurement System

REFERENCES:

1) "The Design of Tetrode Transistor Amplifiers" J. G. Linvill & L. G. Schimpf, Bell System Technical Journal, Vol 35, July 1956, pages 813-840

2) Application Note 77-1, Hewlett Packard, pages 2-4

Basic MODAMP™ MMIC Circuit Techniques

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Introduction and MODAMP™ MMIC Structure

This paper describes Avantek's MSA (Monolithic Silicon Amplifier) series MODAMP™ silicon bipolar Monolithic Microwave Integrated Circuits (MMICs), intended for use as general purpose 50 ohm gain blocks. Their single chip construction minimizes size and parasitics and maximizes uniformity. The wafer fabrication process uses nitride self-alignment for precise registration, ion implantation for precise *doping control*, and both *gold metallization* and *nitride* passivation for high reliability. A variety of geometries allow the designer to select for appropriate gain, power, noise, and frequency chacteristics. Packaging options, ranging from inexpensive plastics to high reliability, hermetically sealed ceramic microstrip.

The internal structure of the MODAMP™ MMIC is a Darlington connected pair of transistors with resistive feedback and a simple resistive biasing scheme. A general schematic is shown in Fig. 1. Since S_{11} and S_{22} are set primarily by resistive divider networks, they remain relatively constant over a wide frequency range. The use of both series feedback (R_E adjusting the emitter voltage of Q2) and shunt feedback (R_F adjusting the base voltage of Q1) helps desensitize the design to variations in active device parameters. A "bleeder" resistor attached to the emitter of Q1 decouples the quiescent bias point of Q1 from the β of Q2 (without this resistor the emitter *current of Q1 would necessarily equal the base current of* Q2). R_C also serves a feedback function. As the transistors draw more current, the voltage drop across R_C will decrease the collector voltages, tending to shut down the transistors.

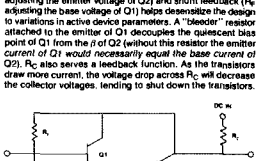


Figure 1. General MODAMP™ schematic.

Since device β (and, therefore, collector current, given a fixed bias) tends to increase with temperature, R_C also serves as a temperature compensating element. Note: On some MODAMP™ MMICs, R_C is an internal element whose value may be a selectable option; on others it must be added as an external component. MODAMP™ MMICs containing internal R_C's have dash suffixes beginning with "1", e.g., MSA-0236-11. Units without an internal collector resistor have dash suffixes beginning with "2" or have no dash suffix.

Since the internal resistive networks prematch both input and output to 50 ohms, MODAMP™ MMICs are particularly easy to design with. To design an amplifier, all that's needed is a 50 ohm microstrip line, blocking capacitors, and some very simple bias circuitry. Nonetheless, because MODAMP™ MMICs are high frequency devices, there are some basic construction rules that should be followed when using them.

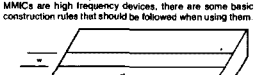


Figure 2. Microstrip structure.

Stripline Structures

Fig. 2 shows a typical microstrip structure. Line impedances are determined by strip width (w), board dielectric material (ϵ_r), and dielectric thickness (h). Since the impedances of the MODAMP™ MMICs are prematched to operate in a 50 ohm system, microstrip lines should be as close to 50 ohms *as possible to realize full specified performance. Dimensions* of 50 ohm line for some common board materials are shown in Table 1. Operation in systems with characteristic impedances other than 50 ohms is possible with somewhat reduced performance; in particular most MODAMP™ MMICs perform satisfactorily in 75 ohm systems without additional impedance matching.

Board Material Selection

A board material should be selected that is appropriate for the intended frequency of operation. Although G10 (epoxy-glass board) is an acceptable low cost choice for small signal, low frequency applications, incon sistencies in the dielectric (usually glass pockets) can cause problems at frequencies above 500 MHz, or with low impedance power stages built on the same board. PTFE woven-glass has much more consistent dielectric characteristics, and performs well to frequencies in excess of 2 GHz. It is also a fairly rugged material that can tolerate substantial rework, and is not particularly sensitive to heat or humidity.

Duroid is the favored material of many microwave designers because of its high dielectric consistency and low dielectric dissipation. Note that 50 ohm line on .015" RT/duroid-5870 is a particularly good match to the lead width of the 70 mil package, meaning minimal step discontinuity effects with this combination. RT/duroid is a somewhat fragile material—it crushes fairly easily, and glues do not adhere well to its substrate so thin metalization patterns are subject to lifting if abused with repeated rework. Some versions can also be quite hydroscopic, and can show substantial dielectric shifts with variations in humidity. Care should be taken when working with this material.

Table 1. Line widths for 50 ohm line for various board materials.

Board Material	ϵ	Thickness	w/h for 50Ω	w for 50Ω
RT/Duroid 5870[1]	2.3	.015"	2.90	.044"
PTFE-Woven Glass Fiber (Typ.)	2.55	.010"	2.55	.025"
		.031"	2.55	.079"
		.062"	2.55	.158"
Epoxy-Glass (G10)	4.8	.062"	1.75	.108"
Alumina/E10[2]	10.0	.025"	0.95	.024"
		.050"	0.95	.048"

[1] Trademark of Rogers Corp. for its PTFE nonwoven glass PC material. (RT is reinforced teflon and PTFE is polytetrafluoroethylene)
[2] E-10 and Epoxlam-10 are trademarks of 3M for its ceramic filled PTFE substrate

Table 2. Representative board material and thickness for various package options.

Package	04	20	35	70	85
Lead Width	.030"	.030"	.020"	.040"	.020"
Representative Board	G10 (.062")	PTFE (.031")	PTFE (.010")	5870 (.015")	G10 or PTFE (.062") (.010")

Alumina is an excellent high frequency material, but because it is a ceramic, it is expensive to process and requires etchants or a diamond scribe for line rework. It is the material of preference for hybrid circuits. Several manufacturers make soft board materials with dielectrics closely approximating those of alumina. These boards are also good choices for high frequency (> 1 GHz) applications.

All boards must be plated on both sides. For soft boards, 1 oz. Cu plating is the most common choice. When etching the circuit pattern, the entire bottom side plating should be left intact to provide the best possible ground plane.

Parasitics

During board layout, care should be taken to minimize all parasitics. Remember that extra lead length equals extra inductance added to the design. This is particularly important if the circuit is to be operated above 1 GHz. Transmission lines should, whenever possible, run flush to the package. For some package options this will require that a hole be made in the circuit board so that the MODAMP™ MMICs' leads are in the same plane as the transmission line. MODAMP™ MMICs should be mounted on the etched side of the board to minimize the inductance of "fed through" connections. Abrupt changes in transmission line width also create parasitic effects, called step discontinuities. Although the *complete* model for such a discontinuity can become quite complicated, the overall effect of the step from a MODAMP™ MMIC lead to a 50 ohm transmission line is typically .05 to .2 nH of extra series inductance. Tapering the transmission lines from 50 ohms down to the MODAMP™ MMIC lead width helps minimize this effect. Bends in transmission lines also create parasitic effects and should be avoided when possible; when they must be used, the corners should be chamfered to prevent the bends from acting as extra shunt capacitance. For more information on the properties of microstrip structures, see K.C. Gupta, et al, *Microstrip Lines and Slotlines*, Artech House, 1979. Dedham, MA.

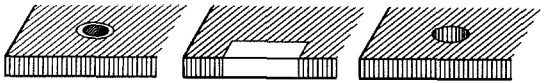
To illustrate how important parasitic effects can be, a "careful" design using a MSA-0204 on $^1/_{16}$" PTFE woven-glass was simulated using a computer program and analyzed from 500 MHz to 3 GHz. Both step discontinuities and parasitic inductances were included in the model. The blocking capacitor was assumed to be a 100 pF, 0.1 inch square ceramic chip with infinate Q and an associated parasitic inductance of .9 nH. The analysis was of the input circuit mismatch only; assuming losses due to output mismatch are of a similar magnitude, the total amplifier loss would be about double that shown. To help distinguish the effects of parasitic mismatch from those due to device impedances, the simulation was also made of both the network with parasitics terminated in a "perfect" (50 + j0 ohm) device and of a MSA-0204 operated in an ideal (parasiticless) system. Table 3 shows the results of the analysis. In this case, amplifier gain loss ranges from negligible (less than .1 dB) at 500 MHz to nearly .4 dB at 3 GHz. Remember that the results shown are for minimal realistic parasitics. If the layout is "sloppy," impedance mismatches in excess of 2:1 and consequent amplifier gain decreases of 1 dB or more can be expected.

Table 3. Parasitic effects on input impedance mismatch of MSA-0204.

Frequency	MSA-0204, No Parasitics		Parasitics Only		MSA-0204 + Parasitics	
MHz	VSWR	Loss, dB	VSWR	Loss, dB	VSWR	Loss, dB
500	1.09:1	0.0	1.01:1	0.0	1.18:1	.03
1000	1.23:1	.04	1.12:1	.01	1.39:1	.11
1500	1.29:1	.07	1.22:1	.04	1.46:1	.15
2000	1.29:1	.07	1.30:1	.07	1.45:1	.15
2500	1.26:1	.06	1.38:1	.11	1.45:1	.15
3000	1.26:1	.05	1.45:1	.15	1.53:1	.19

Grounding

Perhaps the second most important consideration in PC board layout (after impedance matching) is good RF grounding. Ground planes should be kept as large and as solid as possible. Return paths for high frequency circulating currents must be kept as short as possible, especially at the *"emitter's" of the MODAMP™ MMICs. If, for example, plated* through holes are used as ground returns, they should be placed directly under the ground leads of the MODAMP™ MMIC and be located as near as possible to the body of the package. This is because any additional path length here acts as series inductance, which translates into unwanted emitter resistance at operating frequencies. Gain, power compression, and high frequency rolloff will all be degraded if proper grounding techniques *are not used. Fig. 3 shows a variety* of ways of providing good return paths between topside ground connections and the bottom ground plane.



a. Wire "feed through" soldered in place in hole drilled through board

b. "Wrap around" of copper foil (may be used with slot in board)

c. Plated through hole (side walls of hole metalized).

Figure 3. Methods of realizing minimal length return paths to ground.

MODAMP™MMICs incorporating internal "collector" resistors (dash 1 option) help demonstrate how important good grounding is. These units give up one ground lead to allow the designer access to the internal resistor. As a consequence they sacrifice significant high frequency performance. The gain vs. frequency curves of the MSA-0270-12 (single ground lead) and the MSA-0270-22 (dual ground leads) shown in Fig. 4, demonstrate this performance tradeoff. Note the decrease in $f_{1\,dB}$ (the frequency at which the gain is 1 dB lower than the gain at 100 MHz) from around 1.6 GHz to below 1 GHz. Fig. 5 shows a further example of the effects of parasitic emitter inductance resulting from poor

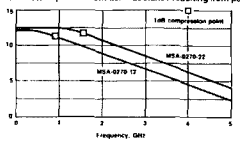


Figure 4. Typical gain vs. frequency for MSA-0270-12 and MSA-0270-22.

RF grounding. The device analyzed is the MSA-0135-21. Gain vs. frequency curves are shown for emitter inductances ranging from 0 to 4 nH.

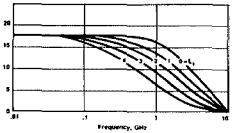


Figure 5. Gain vs. frequency as a function of emitter inductance (L_E) for the MSA-0135-21.

DC Blocking Capacitance

DC blocking capacitors must be used in both the RF input and the RF output lines to isolate the resistive bias circuitry of the MODAMP™ MMIC from the source and load resistances. These capacitors will also put limits on the *frequency response of the finished amplifier. Low frequency* response will be determined by the capacitor's value; it must be high enough to be a reasonable RF "short" at the lowest frequency of operation. High frequency response will be limited to the frequency at which the capacitor's associated parasitic inductance becomes resonant with the blocking capacitor ($1/(2\pi\sqrt{LC})$ Hz, where L = parasitic inductance in Henrys, and C = the capacitor value in Farads). Operation above this frequency often leads to highly unpredictable circuit behavior.

Fig. 6 shows typical effects of blocking capacitors on impedance match as a function of frequency, capacitance, and parasitic inductance. Note that low frequency match is determined by capacitor value, with the parasitic inductance having negligible influence; whereas at higher frequencies, the value of the parasitic inductor dominates the match, with the value of the capacitor becoming unimportant so long as it is large enough to be a low series impedance path. The ratio of capacitive reactance to parasitic resistance is called the Q of the capacitor. Blocking capacitors with high Qs should always be used to minimize insertion losses.

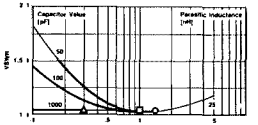


Figure 6a.

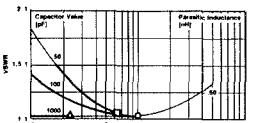


Figure 6b.

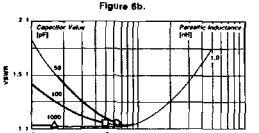


Figure 6c.

□ : resonant frequency, 25 nH parasitic inductance

o : resonant frequency, 0.5 nH parasitic inductance

Δ : resonant frequency, 1.0 nH parasitic inductance

Figure 6. Effects of DC blocking capacitors on VSWR as a function of frequency, capacitance and parasitic inductance.

Biasing

In order to deliver full performance, MODAMP™ MMICs must be biased correctly. The internal resistive networks determine individual transistor operating points; all the user needs to do is present the proper voltage at the DC input terminal. For the purpose of bias stability over temperature, the internal transistors should have their bias supplied through a collector resistor (labeled R_C in Fig. 1). This resistor works in two ways. First, it compensates for increases in device β with temperature by dropping the transistor's collector voltages whenever they try to draw more collector current. Coupled with this effect is the fact that the collector resistor will itself be changing in value over temperature.

Resistors with positive temperature coefficients such as the common carbon composite (+ .0001% per degree C) do an excellent job of compensating for the temperature drift of the negative coefficient on-chip resistors.

For bias stabilization over a temperature range of −10° to + 100°C, a drop of at least 1.5 volts across the collector resistor is necessary. The larger this voltage drop is, the more stable the bias will be. An interesting point is that for a fixed bias (constant quiescent current vs. temperature), the gain of the MODAMP™ MMIC will decrease as temperature increases. A voltage drop of about 2V across the collector resistor allows the bias swing over temperature to compensate for this gain change, yielding best gain flatness over temperature.

Table 4 shows an example of how selection of the bias stabilization resistor influences performance over temperature. These results come from device simulations using PSPICE and correlate well with observed performance of actual amplifiers. Note that with no stabilization resistor the user risks having the MODAMP™ MMIC self destruct at elevated temperatures. In general, bias current will increase as temperature increases (due to increases in device betas with temperature); gain may either increase or decrease depending on how well the bias shift compensates for the decreased gain at a constant bias at higher temperatures.

Table 4. Effects of R_C on performance over temperature.

MSA-0104		Operating Voltage = 5.07 V Nom.		
Voltage Drop, volts	Resistor Value, ohms	Temperature degrees C	Bias Current, mA	Power Gain @ 100 MHz, dB
0	0	−10	9.5	−0.5
		25	16.4	19.8
		100	"	"
1.5	82	−10	14.2	17.0
		25	17.3	19.3
		100	24.1	19.0
2.0	100	−10	16.3	18.5
		25	18.9	18.9
		100	24.6	19.0
7.0	412	−10	16.1	18.3
		25	16.9	18.1
		100	19.3	17.5

" Device destroyed due to excessive current draw

The value of the bias stabilization resistor R_C is given by:

$$R_C = \frac{V_{CC} - V_d}{I_d} \text{ ohms}$$

where V_{CC} = the power supply voltage applied to R_C (in volts)

V_d = the voltage at the DC input terminal of the MMIC (in volts)

I_d = the quiescent bias current drawn by the MMIC (in amps)

The recommended values of I_d and V_d can be found on the individual MODAMP™ MMIC data sheets, both in the *Electrical Specifications* table and above the listing of S-parameters

The dissipation of this resistor is given by:

$$P_{diss} = I_d^2 \times R_C \text{ watts}$$

The power rating of R_C must exceed P_{diss}; if necessary, resistors with lower power ratings may be paralleled to achieve the necessary dissipation capability. Some MODAMP™ MMICS are available with the collector resistor on the chip. This has obvious size and parts count advantages. The tradeoff is for high frequency performance (see the discussion of grounding above) and bias flexibility (only one supply voltage will be appropriate for a given internal resistor value). Also, the on-chip resistors have negative temperature coefficients, and will not hold the MODAMP™ MMIC's bias as constant over temperature as will an external carbon resistor.

Chokes and Bypass Capacitors

It is recommended that an RF choke (large value inductor) be used in series with the bias stabilization resistor. Although the choke is not generally needed to keep the RF out of the DC (the relatively high impedance of the bias stabilization resistor compared to a 50 ohm load is sufficient for this), it is needed to keep the stabilization resistor from appearing in parallel with the load circuit, and thus degrading the output match. A good rule of thumb is that the impedance of the choke at the lowest frequency of operation (given by $2\pi F L$) plus the value of the stabilization resistor should be at least 500 ohms. A 10 µH inductor works well as a choke at frequencies as low as 10 MHz; it can be either a molded inductor (for low cost applications) or a chip inductor (in cases where space is at a premium). At lower frequencies several turns of wire on a high permeability ferrite bead should be used. If the choke is omitted, the designer should expect a gain loss of between 0.5 and 1 dB and a decrease in $P_{1\ dB}$ of as much as 2 dB from the guaranteed performance due to load impedance mismatch.

A large value bypass capacitor (1 µF or so) should be used in conjunction with the choke to present a low impedance path to ground for any signal that does manage to get past the choke. This capacitor should be attached between the supply side of the RF choke and ground.

Typical Circuit Layouts

Fig. 7 shows a typical MODAMP™ MMIC circuit board layout that uses the above construction techniques. The layout is for 1/32" PTFE woven-glass board—a reasonable compromise between cost, durability, and electrical performance. Note that the transmission lines have no bends and are tapered near the package of the MODAMP™ MMIC to minimize step discontinuities. Twelve plated through holes, including two under the emitter leads, provide solid ground planes and minimal emitter parasitics for best high frequency performance. The gaps in the transmission line are appropriate for 50 mil ceramic chip capacitors, which have relatively low associated parasitic inductances—typically about 0.5 nH. The DC pad arrangement requires that a bias stabilization resistor be used, but makes the use of an RF choke optional. If the choke is not used, the stabilization resistor would be connected between the output 50 ohm line and the V_{supply} line, and the bypass capacitor would be attached between the V_{CC} line and ground. Spacing is appropriate for ¼ watt carbon resistors, molded inductors, and 1 µF electrolytic capacitors. The layout has been designed so that the section between the arrows in Fig. 7 can be repeated for multiple cascaded stages. Overall circuit dimensions are 1" × 1.5" for a single stage, with each additional stage adding 1" to the overall length. The size was chosen for convenience of assembly; a more compact layout providing a three stage cascade of MODAMP™ MMICs in the same space and using chip resistors and inductors as shown in Fig. 9. Fig. 8 shows a circuit layout analogous to that in Fig. 7 for a MODAMP™ MMIC with the internal bias stabilization resistor.

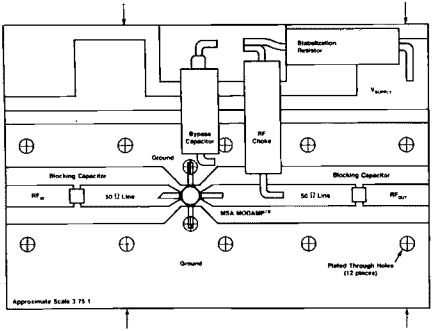


Figure 7. Typical MODAMP™ MMIC circuit (dual ground configuration).

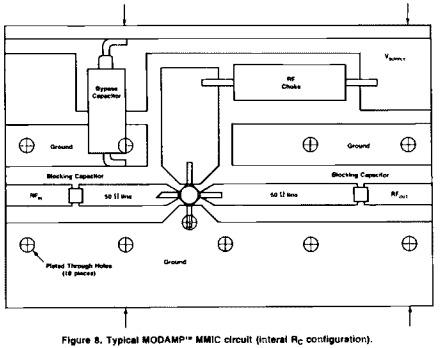


Figure 8. Typical MODAMP™ MMIC circuit (interal R_C configuration).

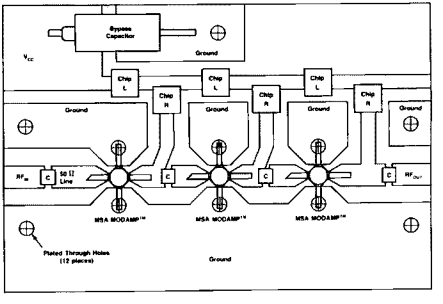


Figure 9. MODAMP™ MMIC circuit layout three stage cascade.

DESIGN OF DIELECTRICALLT STABILIZED OSCILLATORS USING FEEDBACK TECHNIQUES

by

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ABSTRACT

A simple model of a dielectric resonator FET oscillator stabilized with the resonator in the feedback path is presented. Based on this model a high efficiency, high Q DRO was developed In the 7 GHz frequency band. The oscillator has excellent frequency stability and noise performance. A mechanical frequency tunability of ± 50 MHz and power output of +18 dBm was achieved.

INTRODUCTION

Recent advances in the technology of temperature stable dielectric materials like Barium Tetratltanate and Zirconium - Tin Tetratltanate have inspired interest in techniques to dielectrically stabilize fundamental microwave oscillators.

Dielectric resonator oscillators (DROs) are highly compatible with modern microwave integrated circuitry. A sufficiently high output power, high frequency stability, small size and low cost are the features of a DRO. The resonator's high Q contributes to the DRO's excellent FM noise performance.

Oscillators stabilized by a dielectric resonator coupled to the output circuit one-half wave length away from the FET ("passive" injection locking) do not give as high loaded Qs and stability as feedback DROs (series or shunt) exhibit.

The development of fundamental microwave oscillators using a dielectric resonator for shunt feedback has been reported in recent articles. This technique has tended to be empirical in nature, often at the design stage itself. This paper presents a design approach which has been found to be both predictable and sufficiently accurate. Using an approximate feedback model, it was possible to calculate the lengths and Impedances of the feedback microstrip elements required to sustain oscillation, with the dielectric resonator completing the feedback loop. DROs for the 7 GHz and 13 GHz frequency bands were developed using this modeling technique. The test results of the 7 GHz DRO only have been included in this paper. The preliminary results obtained for the Ku band have been encouraging.

DESIGN

The basic schematic of an oscillator is shown in Figure 1. The condition for oscillation is given by

$$\Gamma_R S_{11}' = 1 \qquad \text{OR} \qquad \Gamma_L S_{22}' = 1$$

The two conditions being equivalent [2], we choose

$$|\Gamma_R||S_{11}'|\, e^{j(\theta_R + \theta_{S_{11}'})} = 1$$

The magnitude and phase conditions are given by

$$|\Gamma_R||S_{11}'| = 1 \quad \text{AND} \quad \theta_R + \theta_{S_{11}'} = 0$$

For oscillations to build up it is required that $|\Gamma_R||S_{11}'| > 1$. The microstrip resonator has low losses and hence it is sufficient if S11' can be made greater than unity at the input

of the two port network.

For the NEC GaAs FETs used in the 7 GHz and 13 GHz bands, /S 11/ is between 0.2 to 0.8. Shunt feedback is developed to make /S11'/ > 1 for the condition of oscillation to be met.

The characterization of the feedback network (Figure 2) proceeds as follows. For the chosen electrical length θ1 and impedance Z1, and from the measured S parameters of the device, the Y parameters (say [Y1]) of the combination of the device and output microstrip element are obtained. It is assumed that at resonance, the dielectric resonator is purely resistive (R). For modeling purposes it is also assumed that the dielectric resonator is placed at the end of microstrip element (θ2,Z2), θ2 away from gate of the FET. For the chosen θ2, Z2, and a value of R, the Y parameters (say [Y2]) of the combination of microstrip and dielectric resonator are calculated. Adding [Y1] and [Y2] gives the overall Y parameters of the feedback network with the active device. The new S parameters are derived from this.

The lengths of the microstrip elements θ1 and θ2 are chosen depending upon the mechanical configuration of the active device and the circuit topology. A simple computer program was developed to check oscillation conditions for different values of θ1, θ2, Z1, Z2 and R. The value of R is dependent on the coupling coefficients β1 and β2 between the dielectric resonator and microstrip lines. An optimum coupling is required as weak coupling results in lower output and a tendency to cease oscillations at higher temperatures, while very tight coupling effects the frequency stability. θ1, θ2, Z1 and Z2 are varied to get the condition of /S11'/ >1. A complex conjugate is presented at the gate to determine the frequency. Load matching at the output is optimized for a good RF power.

FABRICATION AND PERFORMANCE

The DRO was fabricated on Teflon (1/32") fibreglass board ($\varepsilon r \approx 2.54$). The biasing arrangement is as shown in Figure 3 with a chip capacitor on the output side for a DC block. The dielectric resonator is magnetically coupled in the TE 018 mode to the gate and drain microstrip lines. The resonator acts as a bandpass filter whose centre frequency can be tuned by varying the gap between the top lid and the dielectric. The exact positioning of the dielectric is critical and a purely empirical approach has been followed to obtain high frequency stability and a sufficiently high power output. The DRO was free from mode jumps and hysteresis. A chip resistor of 50 ohms terminating the gate circuitry was used to eliminate spurious oscillations.

The frequency stability of the DRO was within $\pm$400 kHz over $0^{o}C$ to $55^{o}C$ at a centre frequency of 7410 MHz. The frequency drift over temperature can be adjusted by proper choice of the resonator temperature coefficient. A resonator with a positive temperature coefficient of 6 ppm/^{o}C was used in the oscillator. The output power variation remained within $\pm$ 0.8 dB over the entire temperature range, as shown in Figure 4. Figure 5 shows the variation of frequency as a function of air gap thickness h.

Excess tuning causes sharp output power variation, a fall in loaded Q and mode separation problems. A tendency to mode jump is seen for very low values of h. Moreover close proximity of the tuning screw over the dielectric degrades temperature stability performance. The mechanical tuning range was limited to ± 50 MHz in keeping with practical considerations.

The use of a quartz spacer is recommended for improving the loaded Q [4]. The diameter to height ratio of the dielectric resonator has to be properly chosen for optimum mode separation or spurious oscillations at other modes are possible for an improper selection of D/H ratio. When the dielectric is coupled between the feedback microstrip lines, oscillation over a range of ± 50 MHz of dielectric resonant frequency is possible depending upon the position of the dielectric from the drain port and also on the tightness of coupling. The frequency of the oscillator is set for a slightly higher value than the resonant frequency of the dielectric. Sweep measurement results conducted for the resonator coupled between parallel microstrip lines gave loaded Q values ranging from 800 to around 1000 depending upon the closeness of the lines with the dielectric. It is imperative that the resonant frequency and Q measurement of the resonator be made using a box with the same mechanical dimensions as that of the oscillator. The same microstrip layout was used for fabricating oscillators with centre frequencies from 7.2 to 7.8 GHz. The thickness of the dielectric and its positioning alone had to be varied to construct the oscillators. Repeatability of the oscillators was excellent and final placing of the dielectric resonator was optimized rapidly.

EFFECT OF BIASING

At lower values of gate voltage the frequency pushing was less. In the configuration used the frequency dependence on gate voltage was considerable. A pushing figure of approximately 1 MHz/Vgs and 300 kHz/Vds was obtained. At higher values of gate voltages, pushing was 3 MHz/Vgs. The pushing figures for a free running oscillator constructed with the same device read 80 MHz/Vgs and 3 MHz/Vds.

The measured FM noise at 10 kHz from carrier was -97 dBc 1 Hz BW (Figure 7). A harmonic rejection of greater than -30 dBc and spurious rejection more than -60 dBc was obtained.

A dielectric resonator feedback GaAs FET oscillator has been developed which exhibits:

(1) A frequency stability of better than ± 2.5 ppm/°C.

(2) Mechanical tunability of ± 50 MHz of centre frequency.

(3) FM noise of better than -97 dBc at 10 kHz from carrier, 1 Hz BW.

(4) A stable power output over 0 to 50°C and over the tuning range.

ACKNOWLEDGMENT

Our thanks are due to A.K. Sekhar and Eswarappa for the many useful discussions we had with them. We also wish to thank K.R. Shantharam, M.K. Ramesh and H.R. Keshavamurthy for the assistance given in fabricating the DRO.

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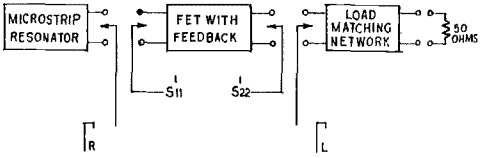

FIG.1 SCHEMATIC OF OSCILLATOR CIRCUIT

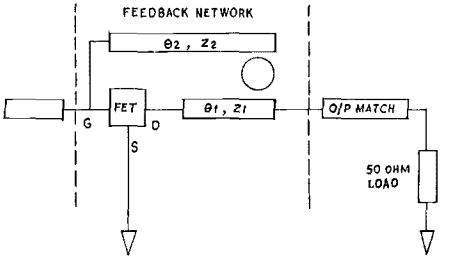

FIG.2 DESIGN MODEL

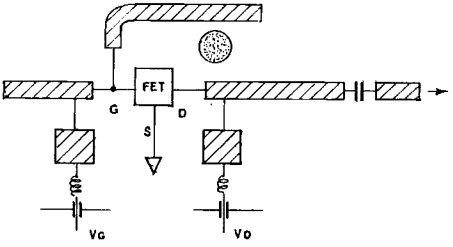

FIG.3 DRO TOPOLOGY

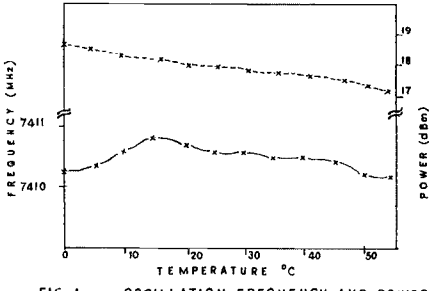

FIG. 4 OSCILLATION FREQUENCY AND POWER OUTPUT OVER 0 TO 50°C

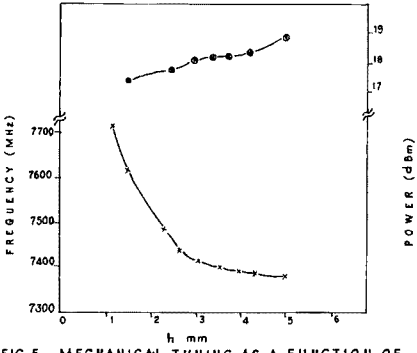

FIG.5. MECHANICAL TUNING AS A FUNCTION OF AIR GAP THICKNESS (h)

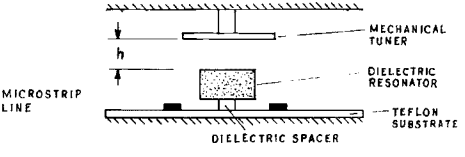

FIG-6 SIDE VIEW OF DIELECTRIC RESONATOR COUPLED BETWEEN FEEDBACK MICROSTRIP LINES

DOUBLE SIDEBAND DEMODULATED FM NOISE
PER 3.1 kHz BAND WIDTH
200 kHz rms DEVIATION = 0dB = 1mW

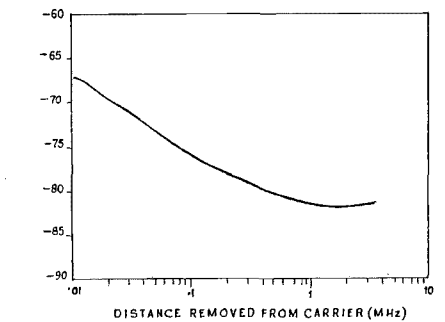

FIG. 7

IRON POWDER CORES FOR HIGH Q INDUCTORS

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SUBJECT: A brief overview will be given of the development of carbonyl iron powders. It will be shown how the magnetic properties of a given iron powder will effect inductor performance and, through example, how the physical size of a core along with its winding details interact to effect Q versus frequency characteristics.

INTRODUCTION: A circuit designer is often faced with a need for inductors and transformers. Regardless of whether it is decided to make or buy these components, it is valuable to have a practical understanding of the parameters that affect their performance.

In the last century the use of solid magnetic material for DC electromagnetics and later laminated magnetic materials for low frequency applications led to the need for materials that would operate efficiently at higher and higher frequencies. With the original thick laminations it was discovered that the apparent permeability or inductance decreased as frequency increased and, at the same time, losses became prohibitive. It was found that by using thin sheets of material insulated from one another that better results were obtained. This is primarily due to an effect known as eddy current shielding. As frequency increases the depth of magnetic penetration decreases for any given material. Thus by having thin sheets, effectively, more of the core body is utilized. This progression worked toward thinner laminations and grain oriented alloys to meet the higher frequency needs.

While the thin oriented laminations were useful for broadband audio transformers, they were unable to meet the need for selective circuits where high Q is required. While at low frequency the magnetic field in a coil is in its axial direction, at high frequency, each turn generates its own field concentric with the wire. These fields are coupled with fields from adjacent turns and are coupled to the core through axial fields rather than one central field. This type of field requires cores laminated in all directions in order to minimize losses and thus maintain reliable inductance and Q versus frequency. As a result, powdered iron cores were developed.

There are two basic classes of iron powders available; Hydrogen reduced irons and carbonyl irons. The hydrogen reduced irons have low resistance, and a relatively large particle size. This type of powder produces the highest permeabilities, (approaching 100), has low losses at low frequency, but the losses increase significantly at high frequency, producing very low Q at RF. Cores from this powder are commonly used for differential-mode chokes in line filters and DC output chokes in switching power supplies.

The carbonyl irons, on the other hand, have a particle which is formed by the decompositon of pentacarbonyliron vapor. This produces a spherical particle with an onion skin structure. The laminating affect of the onion skin produces a resistivity of the individual particles which is much higher than that of pure iron. This high resistance in conjunction with the very small particles size (3 to 5 microns) greatly enhances the high frequency performance. The permeability of carbonyl iron powders, and thus their inductance, can be manufactured to a very tight tolerance and they remain extremely stable with frequency, temperature, and applied signal level. All of these are important considerations in high Q selective circuits.

The distributed air-gap characteristic of the carbonyl iron powder produces a core with permeabilities ranging from 4 to 35. This feature in conjunction with the inherent high saturation point of iron makes it very difficult to saturate at high power RF. Normally, high power applications are limited by temperature rise due to core loss.

In the middle 1930's the first ferrites were investigated. The development of these materials produced higher permeabilities than that attainable with iron powder and, at the same time, they had reasonable losses. In many applications the higher permeability of the ferrite materials is a distinct advantage. However, with high frequency and high Q tuned circuits, high permeability is not nearly as important as attainable Q and good stability with varying environmental and electrical conditions.

Ferrites are typically manufactured to a +/-20% tolerance.

INDUCTANCE: The inductance per turn of a closed magnetic structure, like a toroidal core, is described by:

$$\frac{L}{n^2} = \frac{4\pi u A_e}{l}$$

where: L = inductance in (nH)

u = permeability

A_e = cross-sectional area (cm^2)

l = path length cm

n = number of turns

This illustrates that the inductance per turn of a core is directly related to its permeability and the ratio of its cross-section to its path length. Core manufacturers provide an inductance rating for their cores. There are 3 different descriptions commonly used: nh/t, mh/1000t, and uh/100t. Because the inductance varies, squared with turns, the three compare according to this example:

5nh/t = 50 uh/100 turns = 5mh/1000 turns

These ratings are used to calculate the required turns for a desired inductance as follows:

If Al is in nh/t,

$$\text{required turns} = \left[\frac{\text{desired L (nh)}}{\text{Al}}\right]^{\frac{1}{2}}$$

If Al in mh/1000 turns,

$$\text{required turns} = 1000\left[\frac{\text{desired L (mH)}}{\text{Al}}\right]^{\frac{1}{2}}$$

If rated in uh/100 turns:

$$\text{required turns} = 100\left[\frac{\text{desired L/uh}}{\text{Al}}\right]^{\frac{1}{2}}$$

For example, if 3uh is needed on a core with an inductance index (Al) of 49uh/100 turns then:

$$\text{required turns} = 100\left[\frac{3}{49}\right]^{\frac{1}{2}} = 24.7 \cong 25 \text{ turns}$$

Q CONSIDERATION: What are some of the considerations for producing high Q inductors? What is Q? In a simplified view Q = tan Φ = wL/R where Φ is the phase angle, wL is the inductive reactance and R is the effective series resistance. In the ideal inductor, the phase angle is 90 degrees and the Q is infinite. Likewise, an inductor with a Q of 1 has a phase angle of 45 degrees and thus its reactive and resistive elements are equal). A Q of 150 has a phase angle of 89.6 degrees.

The factors which make up the effective resistance are quite complex. They involve both the core and winding losses. The core losses vary with material, frequency, flux density, and core size. The winding losses involve wire resistance, turn-to-turn, and turn-to-core capacitive effects which are all frequency and size dependent. There are rigorous analyses of these inter-relationships available, but in general they are far too complex to be of much practical use when it comes to designing a high Q, high frequency inductor. The basic trends of these inter-relationships as they relate to frequency are shown in the following exapmles. The examples will use toroidal or donut-shaped cores, but the principles can be applied to other core shapes.

Optimum Q occurs when the combined core loss equals the total winding loss. It has been shown by Legg that, in general, the maximum attainable Q is directly related to the physical size of a core for any given material. It has also been shown that the frequency at which this maximum attainable Q occurs is, in general, inversely proportional to permeability, core size, and the square root of the core loss.

Figure 1 illustrates this basic relationship. For a given core material (carbonyl E, u = 10), recommended frequency range of .25 to 10 mHz), the physically large cores provide a higher peak Q than the physically small cores and the frequency at which

this peak occurs is indeed inversely proportional to the core size. That is to say, large cores reach their optimum at a lower frequency than the small cores.

Figure 2 illustrates that for the same physical size core, a T50, (which is a 1/2 o.d. toroidal core), that the frequency at which the peak Q occurs increases with decreasing permeability. Eddy current losses also are involved in determining this optimum frequency.

In this comparison, the inductance has been a variable in order to approach an optimized Q at an optimized frequency. Figure 3 shows a series of Q curves for the same size core and material, each with a different single layer winding. These curves show that the frequency at which the Q peaks, decreases as the number of turns, and thus the inductance, increases. It also shows that there is a point at which a peak-peak is obtained.

Another interesting comparison is to set the inductance at a fixed value and see how the core size, core material and required windings interact. Figure 4 shows this comparison. While these are not optimized coils, this example illustrates that even with a fixed inductance, larger cores produce higher Q at a lower frequency than the smaller cores.

Thusfar, the examples given have not considered the winding details, but have looked at the interaction of core size and material as it relates to Q and frequency. In the examples shown, the windings have all been a full single layer. The following examples illustrate the effects of different types of windings and their implications versus frequency.

WINDING CONSIDERATIONS: In arriving at the best winding for a given coil, there are two basic effects, which reduce Q, that need to be considered: resistive and capacitive.

The resistance of copper wire at very low frequency is the same as its DC resistance. The skin depth of an AC current is inversely proportional to the square root of the operating frequency. Thus the AC resistance of a conductor is proportional to $\sqrt{f}$. Because of this, the increased resistance due to skin effect will begin to come into play at higher frequencies for smaller wire and at relatively low frequency for large wire. As an example, #30 wire will begin to see increased resistance as low as 300 KHz and #40 wire is affected around 3 MHz. This resistance is further increased in wound coils due to the proximity effect of adjacent turns.

In order to help the AC resistance of a conductor approach its DC resistance at moderate frequency, Litz wire can be used. Litz wire is formed by a number of strands of small insulated wire connected in parallel at the ends and completely interwoven. The interweaving is essential in order for the various strands to equally share the current. There is a significant difference between true Litz wire and stranded wire.

Practical Litz wire is very effective at frequencies up to 1 MHz. As frequency increases, however, the benefits begin to disappear. At very high frequencies the reduced resistance due to the interwoven stranding is more than off-set by the capacitive build-up between the strands. Since most of the work in RF today is at frequencies above 1 MHz the use of Litz wire has become rather uncommon.

In a winding, the self- capacitance that is built up is a result of the turn- to-turn capacitance of adjacent wires as well as turn-to-core capacitance. The turn-to-turn capacitance is affected by the wire size, the number of turns, and the spacing and positioning of the turns. In general, capacitive affects on Q become increasingly important with frequency squared (f^2). For a toroidal coil, one of the most important factors in controlling capacitive built-up is to limit the winding to a single layer. Figure 5, from Welsby, shows how the self capacitance of a toroidal coil varies with the number of winding layers. It is seen that the addition of even a partial second layer dramatically increases the self-capacitance.

This capacitive effect is evident in figure 6. In this example all the coils are wound with #28 wire and essentially the same number of turns. Curve #1 is a single layer winding and has a peak Q of 244. Curve #2 is the result of adding only 2 turns on a second layer. The resulting Q is 7% lower. Curve #3 is a randomly wound coil and exhibits even lower Q. And the worst of the group is curve #4 which has 60 turns on the first layer and 40 turns on the second layer. In this example the capacitive effects have lowered the Q by over 25%.

Since the objective is to minimize both resistance, which implies larger conductors and thus multi-layers, and at the same time to minimize capacitance, which implies single layers with good spacing, it is valuable to keep in mind that the importance of resistance varies with $\sqrt{f}$ and the importance of capacitance varies with f^2. This indicates that at low frequencies resistance is the dominant factor and that at high frequencies capacitance is the most important factor.

Aside from the effect that coil capacitance has on Q, it also affects the self resonant frequency and apparent inductance of the coil. The greater the coil capacitance, the lower the self resonant frequency and the higher the apparent inductance.

These coils are also, often times, either dipped in a material to secure turns or are completely encapsulated. The dielectric characteristics of the material coming in contact with the winding can have a profound effect on the coil capacitance and, therefore, the Q, the apparent inductance and the self-resonant frequency. In order to minimize the shift that occors due to encapsulation, a material with a low dielectric constant must be used.

Another characteristic which effects the apparent inductance is leakage inductance. Leakage inductance acts in series with a coils self inductance. This is the result of uncoupled flux and becomes most apparent in high frequency, low inductance coils, particularly when the turns are not evenly distributed around the core. Here is an example using a T50-17 toroid (u = 4) wound with 10 turns, #20 wire:

In instances like this where it is possible to drastically change the positioning of the turns, and the permeability of the core material is low, very large differences are seen. In higher permeability materials this effect is much less. In a number of applications, toroidal coils are tuned by this means.

SUMMARY: Iron powder is a core material well suited for high Q stable inductors to be used in the 100 KHz to 200 MHz frequency range.

The following relationships regarding core material and size have been shown:

1. For a given material, larger cores produce a higher Q at a lower frequency.

2. For a given material and core size, Q peaks at a lower frequency as the turns are increased. There is a frequency and winding where Q is optimized.

3. For a given core size, the optimum value of Q is inversley proportional to the permeability.

It has also been shown that from the winding standpoint, in order to help optimize Q:

1. At low frequency (< 500 KHz) that the resistive losses are dominant and thus the use of Litz wire is advantageous.

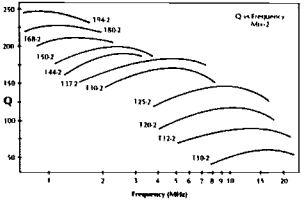
2. At frequencies above 1 MHz losses due to capacitive effects begin to dominate and that multilayering is very detrimental to Q. It can generally be stated that a full single layer will provide the best result.

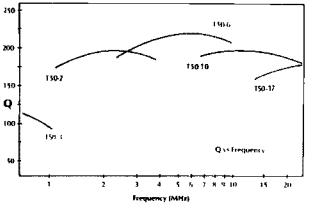
In order to help the design engineer in his efforts to build high Q inductors, Micrometals, Inc. has printed an extensive series of Q vs frequency curves for iron powder cores known as "The Q-Curve Book." In studying this information it can be seen that when high Q is required at a particular frequency and the physical size is limited by packaging requirements that, when possible, it is best to optimize the coil for Q and to adjust the value of the external resonating capacitors rather than to select the desired inductance and then sacrifice Q in order to achieve the inductance.

Another application for which iron powder is receiving increased attention is for use in very high frequency broadband matching applications. The extremely linear frequency response of iron powder even with 35 permeability material makes it useful for transformers above 50 MHz. The primary attraction of iron powder is its repeatability at the extremely high frequencies. Full characterization of these materials for broadband applications up to 1 GHz will be available in the future.

Carbonyl E 10 μo
MIX-2

Micrometals Part No.	Turns	Wire	L (uh)
T 93-2	100	#28	84
T 80-2	100	#28	55
T 68-2	100	#30	57
T 50-2	77	#30	29
T 44-2	66	#30	23
T 37-2	53	#30	11.5
T 30-2	47	#32	9.3
T 25-2	30	#30	3.0
T 20-2	30	#33	2.4
T 12-2	25	#36	1.3
T 10-2	25	#40	.9





PART NUMBER

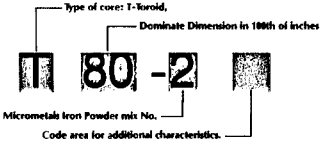

Type of core: T-Toroid,
Dominate Dimension in 100th of inches
T 80 -2
Micrometals Iron Powder mix No.
Code area for additional characteristics.

Figure 1

General Magnetic Properties

Mix #	Basic Iron Powder	Material Permeability (μo)	Temperature Stability (+)	Resonant Circuit Frequency Range[1] (MHz)	Color Code
1	Carbonyl C	20	280 ppm/°C	.15-2.0	Blue
2	Carbonyl E	10	95	.25-10	Red
3	Carbonyl HP	35	370	.02-1.0	Gray
6	Carbonyl SF	8.5	35	2.0-30	Yellow
7	Carbonyl TH	9.0	30	1.0-20	White
8	Carbonyl GQ4	35	255	.02-1.0	Orange
10	Carbonyl W	6.0	150	10-100	Black
12	Synthetic Oxide	4.0	170*	20-200	Green/White
15	Carbonyl GS6	25	190	.10-3.0	Red/White
17	Carbonyl	4.0	50	20-200	Blue/Yellow
22	Synthetic Oxide	4.0	410*	20-200	Green/Orange
0	Phenolic	1	0	50-250	Tan

[1]Frequency range indicated is for maximum Q. For wide-band applications where high Q is not required, the useful frequency range will typically extend 10 to 100 times higher.
*Non-linear

Figure 2

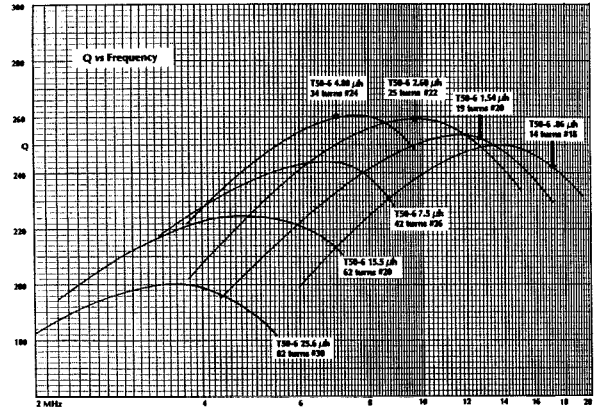


Figure 3

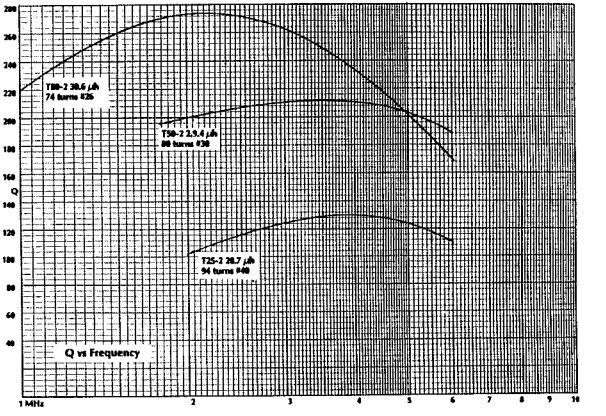


Figure 4

CAPACITANCE OF TOROIDAL WINDINGS AS A FUNCTION OF THE NUMBER OF LAYERS

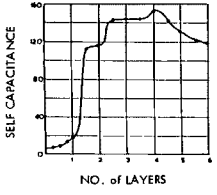


Figure 5

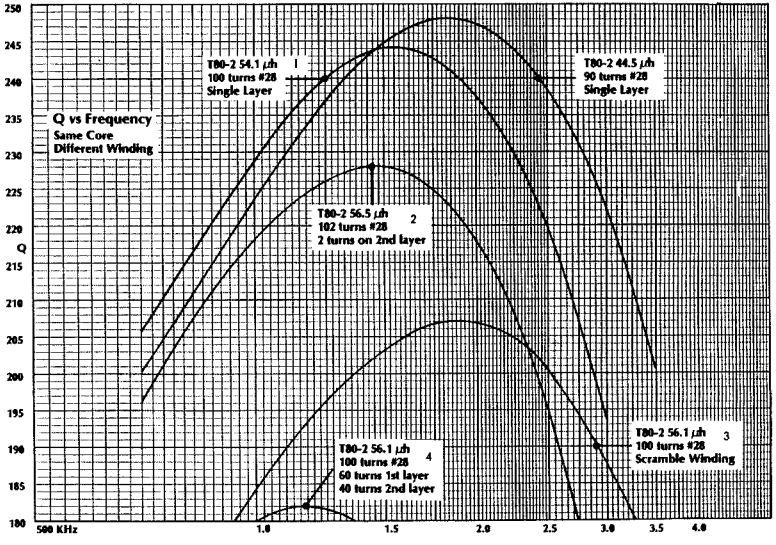


Figure 6

140 MHz Lumped Element 3dB Hybrid

by

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A 140 MHz, 3 dB hybrid was realized using lumped inductances and capacitances. At microwave frequencies 3 dB hybrids are realized using branched line hybrid couplers. Branched line hybrid consists of series and shunt $\lambda/4$ transmission lines. At 140 MHz the $\lambda/4$ transmission line will be about 53.5 cm long in air, and it would be impractical to fabricate branched line hybrids at these frequencies. The characteristics of transmission lines can be realized using lumped inductances and capacitances. It is thus possible to realize the branched line coupler in its equivalent form.

The commonly used single section branched line hybrid coupler is shown in Fig.1(a). The $\lambda/4$ transmission lines of this hybrid can be realized by the lumped element pi-network shown in Fig.1(b). The inductance L and the capacitance C of this network, in terms of the characteristic impedance Z_o and the centre frequency of operation f_o of the equivalent transmission line, are given by the following equations.

$$\sqrt{L/C} = Z_o \qquad \text{-------- (1)}$$

$$1/\sqrt{LC} = 2\pi f_o \qquad \text{------ (2)}$$

Using these equations the L and C values for the 50 Ω and $50/\sqrt{2}$ Ω charecteristic impedance $\lambda/4$ transmission line were calculated and the lumped element equivalent of the 140 MHz 3 dB two branched line hybrid is shown in Fig.2(a). This can be further simplified to the network in Fig.2(b).

Realization of the lumped element $\lambda/4$ transmission line:

A $\lambda/4$ transmission line was realized using aircore inductors and variable capacitors (Thintrim^R). The aircore inductors were measured by resonating them with a chip capacitor (at a series resonant frequency of 140 MHz). The series resonant circuit was loosely coupled to input and output microstrip lines with two 6.8 pF series capacitors. Thintrim^R variable capacitors were tuned to the appropriate value by resonating them with the measured aircore inductors in a similar way. To measure the insertion loss and insertion phase response of the lumped element pi-network, two equal length 50 ohms lines were used on the 31 mil thick Teflon fiberglass substrate. One microstrip line was used as the reference line to eliminate the ambiguities due to co-axial to microstrip transitions. Layout for this experiment is shown in Fig.3 (a). The series inductor L (56.84 nH) was connected by cutting the other microstrip line, and the capacitors C (22.736 pF) were grounded by through holes in patches P_1 and P_2. SMA connectors were used for the external

connections to the microstrip lines. HP 8505A network analyzer and 8503A S-parameters sets were used for measurements. Using an in-house circuit analysis package the theoretical response of the pi-network was calculated. The measured and theoretical insertion loss phase response for the lumped element $\lambda/4$ 50Ω transmission line is shown in Fig.4. There was a very close correlation between the measured and theoretical responses.

The realization of the lumped element branched line hybrid:

Since the lumped element pi-network design based on equations (1) and (2) had a satisfactory phase response, the branched line hybrid was realized as per Fig.2(b). The layout of the lumped element hybrid is shown in Fig.3(b). All the inductors and capacitors were tuned to proper values by the procedure outlined earlier. For this coupler the return loss and isolation maxima occured at different frequencies. The measured return loss and isolation characteristics are shown in Fig.5. Using the in-house "SCAT" circuit analysis program the lumped element hybrid circuit was analyzed. From the theoretical analysis it was found that it is possible to obtain the measured response when there is 10% increase in three of the inductor values, 8% decrease in the capacitor values and about 10% decrease in the value or L_1 (Fig.3b). This order of error in the measurement of L's and C's can be due to the following reasons:

1. Inaccuracy of the series resonant frequency measurement on the network analyzer.
2. Tolerance of chip capacitors used for measuring the aircore inductors.
3. The unaccounted loading of the series resonant circuit used for measuring L's and C's.

Based on the theoretical analysis, the 3 dB hybrid was tuned to get the response shown in Fig.6. it can be seen that this hybrid has a minimum return loss of about 14 dB, a minimum isolation of about 15 dB and a maximum coupling imbalance of 0.7 dB over 128 MHz to 144 MHz. Thus the lumped element 140 MHz 3 dB hybrid has a satisfactory performance over about 12% bandwidth. The difference in the theoretical and experimental results (fig.(6)) could be due to the fact that in theoretical modeling the finite Q's of the inductors and capacitors were not included. Though this coupler was realized with microstrip input and output lines and SMA connectors were used for our convenience, it can be realized on a PCB for integration with other circuits. Unline a Ruthroff transformer this coupler is compatible with planar technology and can be easily miniaturized using thick and thin film techniques. For a broader bandwidth, lumped element equivalent circuits for higher order branched line hybrids can be realized.

ACKNOWLEDGEMENT

The authors wish to record their thanks to management of M/S indian telephone industries Limited, Bangalore for kind permission to publish this paper.

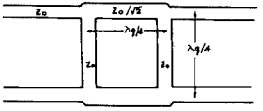

FIG. 1(a). SINGLE SECTION BRANCHED LINE COUPLER

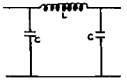

FIG. 1(b) TRANSMISSION LINE EQUIVALENT LUMPED ELEMENT NETWORK.

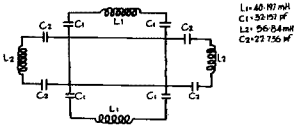

FIG. 2(a) L.C. ANALOGUE OF A BRANCHED LINE COUPLER

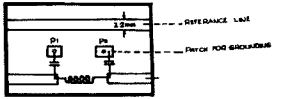

FIG. 3(a) LAYOUT FOR LUMPED ELEMENT λ/4 TRANSMISSION LINE MEASUREMENTS.

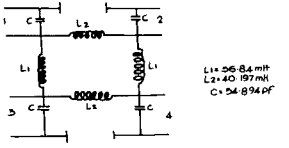

FIG. 2(b). SIMPLIFIED LUMPED ELEMENT BRANCHED LINE HYBRID.

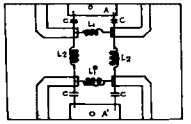

FIG. 3(b) LAYOUT OF THE LUMPED ELEMENT HYBRID.

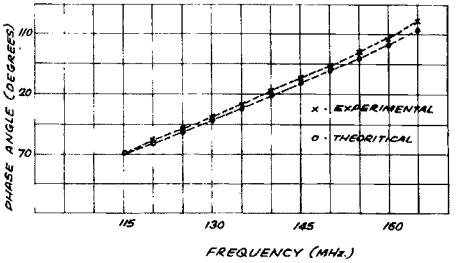

FIG. 4. THEORETICAL & EXPERIMENTAL VALUES OF INSERTION PHASE FOR λ/4 LINE.

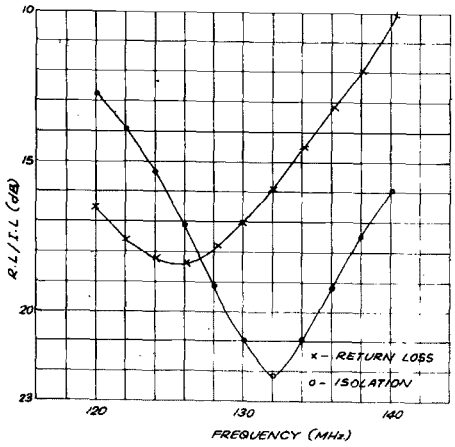

FIG. 5 UNTUNED COUPLER RESPONSE

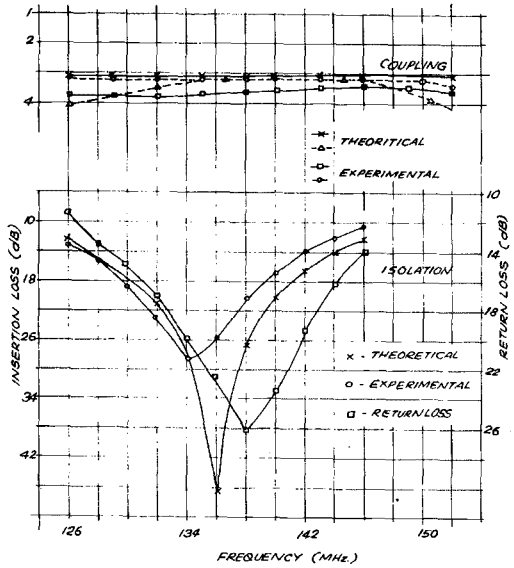

FIG. 6 TUNED HYBRID COUPLER RESPONSE

A COMMUTATION DOUBLE-BALANCED MIXER OF HIGH DYNAMIC RANGE

by

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INTRODUCTION

Dynamic range remains the principle goal of HF mixer design. The intermodulation performance and overload characteristics of a mixer are fundamental qualities used in the evaluation of a good design. Heretofore, most mixers sporting a high dynamic range have been either the passive diode-ring variety, or the active FET mixer.[1][2]

Common to both the diode and FET is their square-law characteristic so important in maintaining low distortion during mixing. However, equally important for high dynamic range is the ability to withstand overload that has been identified as a principle cause of distortion in mixing.[3] Some passive diode-ring mixer designs have resorted to paralleling of diodes to effect greater current handling, yet the penalty for this apparent improvement is the need for a massive increase in local-oscillator power.

This report examines a new FET mixer where commutation achieves high dynamic range without exacting the anticipated penalty of increased local-oscillator drive. Using the Siliconix Si8901, third-order intercept points upwards of +39 dBm (input) have been achieved with only +17 dBm of local-oscillator drive!

CONVERSION EFFICIENCY OF THE COMMUTATION MIXER

Unlike either the conventional diode-ring mixer or the active FET mixer, the commutation mixer relies on the switching action of the quad-FET elements to effect mixing action. Consequently, the commutation mixer is, in effect, no more than a pair of switches reversing the phase of the signal carrier at a rate determined by the local-oscillator frequency. Ideally, we would anticipate little noise contribution and, since the switching mixer, consisting of four "switches," has finite ON resistance, performance is similar to that of a switching attenuator. As a result, the conversion efficiency of the commutation mixer may be expressed as a loss.

This loss results from two related factors. First, is the r_{DS} of the MOSFET relative to the signal and IF impedances; second -- a more common and expected factor -- is the loss attributed to signal conversion to undesired frequencies. There are, however, ways to reduce the effects of undesired frequency generation by the use of filters.

The effect of r_{DS} of the MOSFETs may be determined from the analysis of the equivalent circuit shown in Figure 1, assuming that our local oscillator waveform is an idealized square-wave. It is not, but if we assume that it is, our analysis is greatly simplified; and for a commutation mixer, a high local-oscillator voltage begins to approach the ideal waveform of a square-wave.

Figure 1, showing switches rather than MOSFETs, also identifies the ON state resistance, r_{DS}, as well as the OFF-state resistance, r_{OFF}. The latter can be disregarded in this analysis as it is generally extremely high. On the other hand, the ON-state resistance, r_{DS}, together with the source and

load impedances (viz., signal and intermediate-frequency impedances) directly affects the conversion efficiency.

If we assume that our local-oscillator excitation is an idealized square-wave, the switching action may be represented by the Fourier series as,

$$\phi(x) = \frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2n-1)\,\omega t}{(2n-1)} \qquad \text{Eq. (1)}$$

The switching function, $\phi(t)$, shown in the derivative equivalent circuit of Figure 2, is derived from the magnitude of this Fourier series expansion as a power function by squaring the first term, viz., $(\frac{2}{\pi})^2$.

The available power that can be delivered from a generator of RMS open-circuit terminal voltage, V_{in}, and internal resistance, R_g, is,

$$P_{av} = \frac{V_{in}^2}{4R_g} \qquad \text{Eq. (2)}$$

or, in terms shown in Figure 3,

$$P_{av} = \frac{V_{in}^2}{\pi^2 R_g} \qquad \text{Eq. (3)}$$

The output power, deliverable to the intermediate-frequency port, is,

$$P_{out} = \frac{V_o^2}{R_L} \qquad \text{Eq. (4)}$$

To arrive at V_o, we first need to obtain the loop current, i_L, which from Figure 3, offers,

$$i_L = \frac{V_{in}}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad \text{Eq. (5)}$$

then,

$$V_o = \frac{V_{in} R_L}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad \text{Eq. (6)}$$

Combining Eqs. (4) and (6),

$$P_{out} = \frac{V_{in}^2 R_L}{\left[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}\right]^2} \qquad \text{Eq. (7)}$$

Conversion efficiency -- in the case for the commutation mixer, a loss -- may be calculated from the ratio of P_{av} and P_{out},

$$L_c = 10 \log \frac{P_{av}}{P_{out}} \quad dB \qquad \text{Eq. (8)}$$

Substituting Eq. (3) for P_{av}, and Eq. (7) for P_{out}, we obtain,

$$L_c = 10 \log \frac{\left[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}\right]^2}{\pi^2 R_L R_g} \quad dB \qquad \text{Eq. (9)}$$

The conversion loss represented by Eq. (9) is for a broadband double-balanced mixer with all ports matched to the characteristic line impedances. The ideal commutation mixer operating with resistive source and load impedances will result in having the image and all harmonic frequencies dissipated. For this case, the optimum conversion loss reduces to,

$$L_c = 10 \log \frac{4}{\pi^2} \quad dB \qquad \text{Eq. (10)}$$

or -3.92 dB.

However, a truly optimum mixer also demands that the MOSFETs exhibit an ON-state of zero Ohms, and, of course, an ideal square-wave excitation. Neither is possible in a practical sense.

Equation 9 can be examined for various values of source and load impedances as well as r_{DS} by graphical representation, as shown in Figure 4, re-

membering that a nominal 3.92 dB must be added to the values obtained from the graph.

To illustrate how seriously the ON-state of the MOSFETs affects performance, we need only to consider the Si8901 with a nominal r_{DS} (at V_{GS}=15V) of 23 ohms. With a 1:1 signal transformer (50 to 25-0-25Ω), Rg/r_{DS} = 1.1. Allowing a 4:1 IF output impedance to a 50 ohm preamplifier, the ratio R_L/r_{DS} approximates 4. From Figure 4 we read a conversion loss, L_c, of approximately 3.7 dB, to which we add 3.92 dB for a total loss of 7.62 dB. Additionally, we must also include the losses incurred by both the signal and IF transformers. The results compare favorably with measured data.

A careful study of Figure 4 reveals what appears as an anomalous characteristic. If we were to raise R_g/r_{DS} from 1.1 to 4.3 (by replacing the 1:1 transformer with a 1:4 to effect a signal-source impedance of 100-0-100Ω), we would see a dramatic improvement in conversion efficiency! The anomaly is that this suggests that a mismatched signal-input port improves performance.

Caruthers [4] first suggested that reactively terminating all harmonic and parasitic frequencies would reduce the conversion loss of a ring demodulator to zero. This, of course, would also require that the active mixing elements (MOSFETs in this case) have zero r_{DS}, in keeping with the data of Figure 4.

A double-balanced mixer is a 4-port, consisting of a signal, image, IF and local-oscillator port. Of these, the most difficult to terminate is the image-frequency port simply because, in theory it exists as a separate port, but in practice it shares the signal port. Any reactive termination would, therefore, be narrow-band irrespective of its proximity to the active mixing elements.

The performance of an image-termination filter offering a true reactance to the image frequency (100% reflective) may be deduced to a reasonable degree from Figure 4, if we first presume that the conversion loss between signal and IF compares with that between signal and image. The relationship is displayed in Figure 5 where we see the expected variation in amplitude proportional to conversion efficiency (inversely proportional to conversion loss).

Image-frequency filtering affects more than conversion efficiency. As the phase of the detuned-short position of the image-frequency filter is varied we are able to witness a cyclical variation in the intermodulation distortion as has been confirmed by measurement, shown in Figure 6. By comparing Figure 5 with Figure 6, we see that any improvement in conversion loss appears to offer a corresponding degradation in the intermodulation distortion.

INTERMODULATION DISTORTION

Unbalanced, single-balanced and double-balanced mixers are distinguished by their ability to selectively reject spurious frequency components, as defined in table I. The double-balanced mixer, by virtue of its symmetry, suppresses twice the number of spurious frequencies as does the single-balanced mixer.

In the ideal mixer, the input signal is translated to an intermediate-

frequency without distortion, viz., without imparing any of the contained information. Regrettably, the ideal mixer does not occur in practice. Because of certain nonlinearities within the switching elements as well as imperfect switching resulting in phase modulation, distortion results.

Identifying Intermodulation Distortion Products

The most damaging intermodulation distortion products (IMD) in receiver design are generally those attributed to odd-order, and, in particular, to those identified as the third-order IMD.

Any nonlinear device may be represented as a power series,

$$i_d = g_m e_g + \frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2 + \frac{1}{3!}\frac{\delta^2 g_m}{\delta V_G^2} e_g^3 + \cdots + \frac{1}{n!}\frac{\delta^{n-1} g_m}{\delta V_G^{n-1}} e_g^n \qquad \text{Eq. (11)}$$

which can be further broken into

TERM	OUTPUT	TRANSFER CHARACTERISTIC
$g_m e_g$	F1, F2	Linear
$\frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2$	2F1, 2F2 F1 ± F2	[Second-order Square-Law]
$\frac{1}{3!}\frac{\delta^2 g_m}{\delta^2 V_G} e_g^3$	3F1, 3F2 2F1 ± F2 2F2 ± F1	Third-Order

The second term is the desired intermediate-frequency we seek, all other higher-orders are undesirable, but, unfortunately, present to a varyign degree as illustrated in Figure 7.

There are both fixed-level IMD products and level-dependent IMD products.[5] The former are produced by the interaction between a fixed-level signal, such as the local oscillator and the variable-amplitude signal. The resulting frequencies may be identified,

$$n\phi_1 \pm \phi_2 \qquad \text{Eq. (12)}$$

where, n is an integer greater than 1.

Level-dependent IMD products result from the interaction of the harmonics of the local oscillator and those of the signal. The resulting frequencies may be identified,

$$n\phi_1 \pm m\phi_2 \qquad \text{Eq. (13)}$$

where, m and n are integers greater than 1.

For a mixer to generate IMD products at the intermediate frequency we must account for at least a two-step process. First, the generation of the harmonics of the signal and local oscillator; and, second, the mixing or conversion of these frequencies to the intermediate frequency. Consequently, the mixer may be modelled as a series connection of two nonlinear impedances, the first to generate the harmonic products, the second to mix or convert to the intermediate frequency. Although many harmonically-related products are possible, we will focus principally on odd-order IMD products.

If we allow two interfering signals, f_1 and f_2, to impinge upon the first nonlinear element of our mixer model, the result will be $2f_1 - f_2$ and $2f_2 - f_1$. These are identified as third-order intermodulation products (IMD_3). Other products are also generated taking the form $3f_1 - 2f_2$ and $3f_2 - 2f_1$, called fifth-order IMD products (IMD_5). Unlike the even-order products, odd order products lie close to the fundamental signals and, as a consequence, are

most susceptible of falling within the passband of the intermediate frequency and thus degrading the performance of the mixer.

A qualitative definition of linearity based upon intermodulation distortion performance is called the Intercept Point. By recognizing that,

the fundamental output (IF) response is directly proportional to the signal input level;

the second-order output response is proportional to the square of the signal input level; and,

the third-order output response is proportional to the cube of the signal input level,

then convergence occurs. The point of convergence is termed the Intercept Point. The higher the value of this intercept point, the better the dynamic range.

Intermodulation Distortion in the Commutation Mixer

Although the double-balanced mixer outperforms the single-balanced mixer as we saw in Table I, a more serious source of intermodulation products result when the local-oscillator excitation departs from the idealized square-wave.[6][7] This phenomenon is easily recognized by a careful examination of Figure 8, where a sinusoidal local-oscillator voltage reacts not only upon a varying transfer characteristic but also on a varying nonlinear, voltage-dependent capacitance (not shown in Figure 8). Although the effects of this sinusoidal transition are not easily derived, Ward [8] and Rafuse [9] have concluded that lowering R_g will provide improved intermodulation performance! This conflicts with low conversion loss, as we saw in Figure 4.[10]

Further examination of Figure 8 reveals that the sinusoidal local-oscillator excitation results in phase modulation. That is, as the sinusoidal wave goes through a complete cycle, the resulting gate voltage, acting upon the MOSFET's transfer characteristic, produces a resulting nonlinear waveform. Since all FETs have some offset -- a JFET has a cut-off voltage; a MOSFET has threshold voltage -- it is important, for symmetry as well as for balance, to offer some DC offset voltage to the gates. Optimum IMD performance demands that the switches operate in a 50% duty cycle; that is, the switches must be fully ON and fully OFF for equal time. Without some form of offset bias this would be extremely difficult unless we were to implement an idealized square-wave drive.

Walker [11] has derived an expression showing the predicted improvement in the relative level of two-tone third-order intermodulation products (IMD_3) as a function of the rise and fall times of the local-oscillator waveforms.

$$20\ Log \left[\frac{\left[t_r\, \omega_{LO}\, \frac{V_s}{V_c} \right]^2}{\pi} \right] \quad dB \qquad \text{Eq. (14)}$$

where, V_c is the peak-to-peak local-oscillator voltage,

V_s is the peak signal voltage,

t_r is the rise and fall time of V_c,

ω_{LO} is the local-oscillator frequency.

Equation 14 offers us several interesting aspects on performance. Since any reduction in the magnitude of V_s improves the IMD, we again discover that lowering R_g (which, in turn, decreases the magnitude of V_s) appears to bene-

fit performance. Second, the higher the local-oscillator voltage the better the IMD performance. Third, if we can provide the idealized square-wave drive we achieve infinite improvement in IMD performance!

An additional fault of sinusoidal local-oscillator excitation results whenever the wave approaches the zero-crossing at half-period intervals. As the voltage decays we find that any signal votlage may overload the MOSFETs causing intermodulation and crossmodulation distortion.[12] This can be easily visualized from Figure 9 where we see the classic i-e characteristics of the MOSFET at varying gate voltages. Only at substantial gate voltage do we witness reasonable linearity, and consequently, good dynamic range.

DYNAMIC RANGE OF THE COMMUTATION MIXER

As the two-tone Intercept Point increases in magnitude, we generally conclude a like improvement in dynamic range results. Yet, as we have concluded from earlier study, the intermodulation products appear to be a function of both the generator or source impedance as well as the ratio R_g/r_{DS} and R_L/r_{DS} (see Figure 4).

In any receiver performance can be quantified by the term Dynamic range. Dynamic range can be extended by improving the sensitivity to low-level signals and by increasing the power-handling ability without being overcome by interfering intermodulation products or the effects caused from desensitization.

There are rules to follow if we are to improve the low-level signal sensitivity. Ideally we would like a mixer to be transparent, acting only to manipulate the incoming signals for easy processing by subsequent equipment. The perfect mixer would have no conversion loss and a zero noise figure. However, in the preceeding analysis we discovered that optimum intermodulation performance occurred when the signal-input port is mismatched to the quad MOSFETs (Figure 4). It now becomes clear that a performance trade-off appears necessary. Either we seek low conversion loss and with it a lower noise figure, or we aim for the highest two-tone intercept point. Fortunately, as we seek the latter, our dynamic range will actually improve since a mismatched signal port has less effect upon the signal-to-noise performance of the mixer than does a matched signal port have upon the intermodulation distortion.

Convention has identified minimum sensitivity to be the weakest signal which will produce an output signal 10 dB over that of the noise in a prescribed bandwidth (usually 1 kHz), or

$$S_{EMS.} = 20\ Log\ \frac{V_S + V_N}{V_N} + 10\ dB \qquad \text{Eq. (15)}$$

Desensitation occurs whenever a nearby unwanted signal causes the compression of the desired signal. The effect appears as an increase in the mixer's conversion loss.

THE Si8901 AS A COMMUTATION MIXER

Because of package and parasitic constraints, the Si8901 appears best suited for performance in the HF to low VHF region. A surface-mounted version may extend performance to higher frequencies.

In our review of intermodulation distortion we recognized that to achieve

a high intercept point the local-oscillator drive must

approach the ideal square-wave;

ensure a 50% duty cycle; and,

offer sufficient amplitude to ensure a full ON and OFF switching condition, as well as to offer reduced r_{DS} when ON.

Furthermore, to maintain superior overall performance -- in conversion loss, dynamic range (noise figure) and intercept point -- some form of image frequency termination would be highly desirable even though, understandably, the mixer's bandwidth would be restricted. Consequently, the principal effort in the design of a high dynamic range commutation mixer is two-fold. First, and most crucial, is to achieve a gating or control voltage sufficient to ensure a positive and hard turn-ON as well as a complete turn-OFF of the mixing elements (MOSFETs). Second, and of lesser importance, is to properly terminate the parasitic and harmonic frequencies developed by the mixer.

Establishing the Gating Voltage

Local-oscillator injection to the conventional diode-ring, FET, or MOSFET double-balanced mixer is by the use of the broadband, transmission-line, transformer, [13] as shown in Figure 10. For the diode-ring mixer where switching is a function of loop current, or for active FET mixers that operate on the principle of transconductance and thus need little gate voltage, [14] the broadband transformer is adequate. If this approach is used for the commutation mixer, we would need extraordinarily high local-oscillator drive to ensure positive turn-ON. Rafuse [15] and Ward [16] used a minimum of 2 W to ensure mixing action; Lewis and Palmer [17] achieved high dynamic range using 5 Watts! The MOSFETs used in these early designs were p-channel, enhancement (2N4268) with moderately high threshold (6 V max.) and high input capacitance (6 pF max.). All of these early MOSFET double-balanced mixers relied on the conventional 50 to 100-0-100Ω transformer for local-oscillator injection to the gates.

A major goal is the conservation of power. This goal cannot be achieved using the conventional design. Simply increasing the turns ratio of the coupling transformer is thwarted by the reactive load presented by the gates.

The obvious solution is to use a resonant gate drive. The voltage appearing across the resonant tank -- and thus on the gates -- may be easily calculated,

$$V = |P \cdot Q \cdot X| \qquad \text{Eq. (16)}$$

P is the power delivered to the resonant tank circuit;

Q is the loaded Q of the tank circuit; and,

X is the reactance of the gate capacity.

Since the gate capacitance of the MOSFET is voltage dependent, the reactance of the gate becomes dependent upon the impressed excitation voltage. To allow this would severely degrade the IMD performance of the mixer. However, we can minimize the change in gate capacitance and remove its detrimental influence using a combination of substrate and gate bias, as shown in Figure 11. Not only does this show itself beneficial in this regard, but, as we saw in Figure 8, a gate bias is necessary to ensure the required 50% duty cycle. Furthermore, a negative substrate voltage ensures that each MOSFET on the monolithic substrate is electrically isolated and that each source-/drain-to-body

diode is sufficiently reverse biased to prevent half-wave conduction.

Implementing the resonant gate drive may take any of several forms. The resonant tank circuit may be merged with the oscillator, or it can be a varactor tuned Class B stage, [18] or, as in the present design, an independent resonant tank, shown in Figure 12.

To ensure symmetrical gate voltage in 180° anti-phase, if the local oscillator drive is asymmetrical, viz., fed by unbalanced coax, an unbalanced-to-balanced balun must be used (T1 in Figure 12), otherwise capacitive unbalance results with an attendant loss in mixer performance.

Table II offers an interesting comparison between a resonant-gate drive with a loaded tank Q of 14 and a conventional gate drive using a 50 to 100-Ω-100Ω transformer. The importance of a high tank Q is graphically portrayed in Figure 13. The full impact of a high gate voltage swing can be appreciated by using Equation 14. Here, as V_c (gate voltage) increases the intermodulation performance (IMD) also improves as we might intuitively expect. Calculated and measured results are shown in Figure 14 and demonstrate reasonable agreement. The difference may reflect problems encountered in measuring V_c as any probe will inadvertently load, or detune, the resonant tank even with the special care that was taken to compensate.

If we have the option to choose "high side" or "low side" injection -- viz., having the local-oscillator frequency above (high) or below (low) the signal frequency -- a closer inspection of Equation 14 should convince us to choose low-side injection.

Terminating Unwanted Frequencies

If our mixer is to be operated over a restricted frequency range where the local oscilator and signal frequencies can be manipulated, image-frequency filtering may be possible. Image-frequency filtering does affect performance. For high-side local-oscillator injection an elliptical-function low-pass filter, or for low-side injection a high-pass filter might offer worthwhile improvement. In either case, the filter offers a short-circuit reactance to the image frequency forcing the image to return once again for demodulation. The results of using a low-pass filter with the commutation mixer are known from our earlier examination of Figures 5 and 6.

The resonant-gate drive consisting of a high-Q tank offers adequate bypassing of the intermediate frequency and image frequency.

If the IF is narrow band, filtering may be possible by simply using a resonant LC network across the primary of the transformer. [19]

Design Techniques in Building the Commutation Mixer

The mixer was fabricated on a high-quality double-copper clad board (PCB) shown in Figure 15. An improvised socket held the Si8901. The signal and IF ports used Mini-Circuits, Inc., plastic T-case RF transformers. For the IF, the Mini-Circuits T4-1 (1:4); for the signal, the Mini-Circuits T1-1T (1:1) or T4-1 was used. The resonant tank was wound on a ¼-inch ceramic form with no slug. The unbalanced-to-balanced resonant tank drive used a T4-1. The schematic diagram, Figure 16, is for a commutation mixer with high-side injection, operating with an IF of 60 MHz.

The principle effort involved the design of the resonant-gate drive. This necessitated an accurate knowledge of the gate's total capacitive loading effect. To accomplish this a precision fixed capacitor (5 pF) was substituted for the Si8901 and at resonance it was a simple task to calculate the inductance of the resonant tank. Substituting the Si8901 made it again a simple task to determine the capacitive effect of the Si8901. Once known, a high-Q resonant tank can be quickly designed and implemented. To ensure good interport isolation, symmetry is important, so care is necessary in assembly to maintain mechanical symmetry, especially with the primary winding.

Performance of the Si8901 Commutation Mixer

The primary goal in developing a commutation double-balanced mixer is to achieve a high dynamic range. If this task can be accomplished with an attendant savings in power consumption, then the resulting mixer design should find wide application in HF receiver design.

The following tests were performed.

Conversion efficiency (loss)
Two-tone, 3rd-order Intercept Point
Compression level
Desensitization level
Noise Figure

Conversion loss and Intercept Point are directly dependent upon the magnitude of the local-oscillator power. The mixer's performance is offered in Figure 17, where the input intercept is plotted with conversion loss.

Both the compression and desensitization levels may appear to contradict reason. Heretofore, conventional diode-ring demodulators exhibiting compression and desensitization levels an order of magnitude below the local-oscillator power level. However, with a commutation MOSFET mixer, switching is not accomplished by the injection of loop current but by the application of gate voltage. At a local-oscillator power level of +17 dBm (50 mW), the 2 dB compression level and desensitization level was +30 dBm! The single-sideband HF noise figure of 7.95 dB was measured also at a local-oscillator power level of +17 dBm.

CONCLUSIONS

Achieving a high gate voltage to effect high-level switching by means of a resonant tank is not a handicap. Although one might at first label the mixer as narrow-band, in truth the mixer is wideband. For the majority of applications, the intermediate frequency is fixed, that is, narrow band. Consequently, to receive a wide spectrum of signal frequencies the local oscillator is tuned across a similar band. In modern technology this tuning can be accomplished by numerous methods. Likewise the resonant tank may take several forms. It can be part of the oscillator, or, as in Ref. (18), it can be a varactor-tuned driver electroncially tracking the local oscillator.

If the local-oscillator drive was processed to offer a more rectangular waveform, approaching the idealized square-wave, we might then anticipate even greater dynamic range as predicted by Equation 14.

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Single-Balanced	Double-Balanced
f_a	
$3f_a$	
$5f_a$	
$f1 \pm f2$	$f1 \pm f2$
$f1 \pm 3f2$	$f1 \pm 3f2$
$f1 \pm 5f2$	$f1 \pm 5f2$
$2f1 \pm f2$	
$2f1 \pm 3f2$	
$3f1 \pm f2$	$3f1 \pm f2$
$3f1 \pm 3f2$	$3f1 \pm 3f2$
$4f1 \pm f2$	
$5f1 \pm f2$	$5f1 \pm f2$

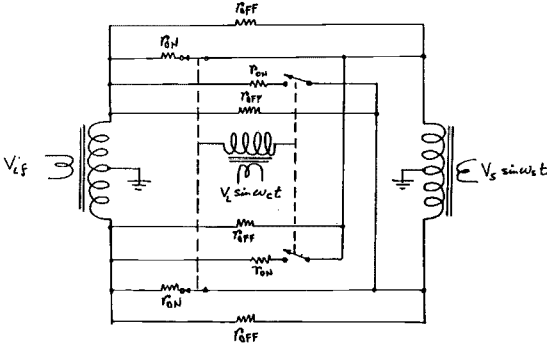
A Comparison of Modulation Products in Single and Double Balanced Mixers to the 6th Order

TABLE I

Power in (mW)	NR Gate Voltage (V)	Res Gate Voltage (V)
10	0.20	5.4
20	0.29	7.7
30	0.33	9.4
60	0.44	13.3

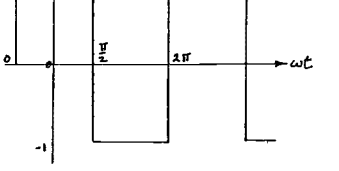
Comparison of a-c gate voltage versus local-oscillator drive between a non-resonant (NR) and resonant (Res) tank with a loaded Q of 14 (Freq. 150 MHz)

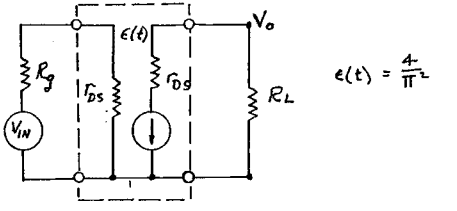
TABLE II



EQUIVALENT CIRCUIT OF COMMUTATION MIXER

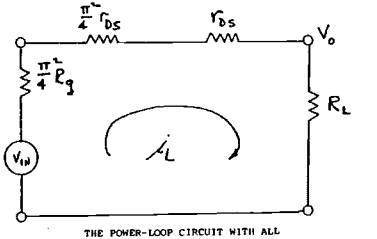
FIGURE 1





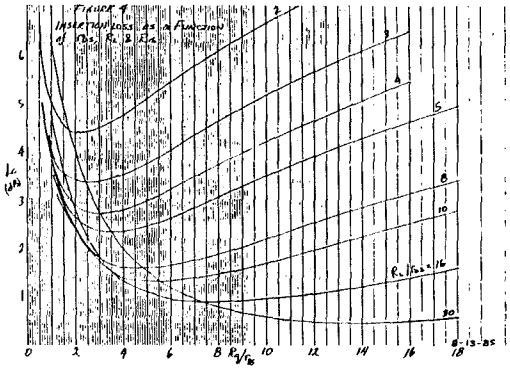
DERIVATIVE EQUIVALENT CIRCUIT

FIGURE 2



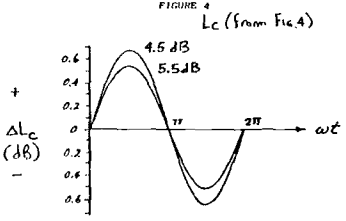
THE POWER-LOOP CIRCUIT WITH ALL ELEMENTS EQUIVALENT, BASED ON THE TRANSFER FUNCTION, $e(t) = 4/\pi^2$

FIGURE 3



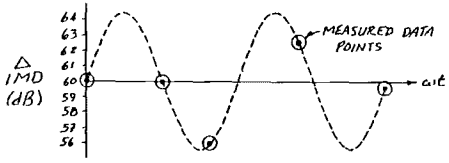
INSERTION LOSS AS A FUNCTION OF r_{DS}, R_L, & R_G

FIGURE 4



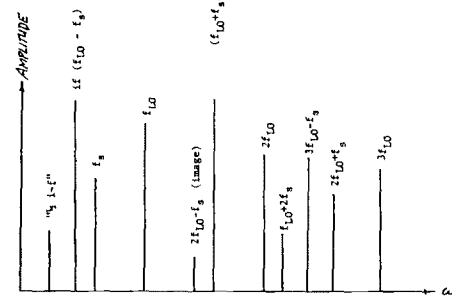
EFFECT OF IMAGE TERMINATION ON
CONVERSION LOSS

FIGURE 5



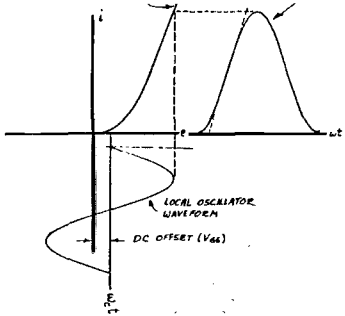
EFFECT OF IMAGE TERMINATION ON
3rd-ORDER DISTORTION

FIGURE 6



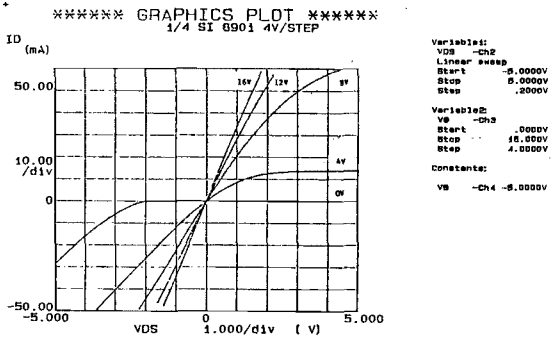
THE HARMONIC & SPURIOUS CONTENT
EXITING THE IF PORT OF THE
COMMUTATION MIXER

FIGURE 7



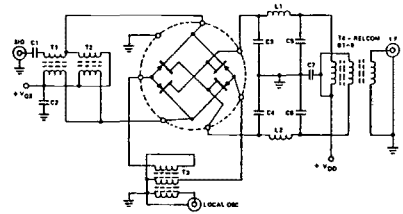
EFFECT OF SINUSOIDAL LOCAL OSCILLATOR WAVEFORM ON IF LINEARITY

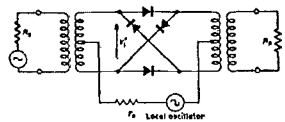
FIGURE 8



FIRST & THIRD QUADRANT I-E CHARACTERISTICS SHOWING EFFECTS OF GATE VOLTAGE LEADING TO LARGE SIGNAL OVERLOAD DISTORTION

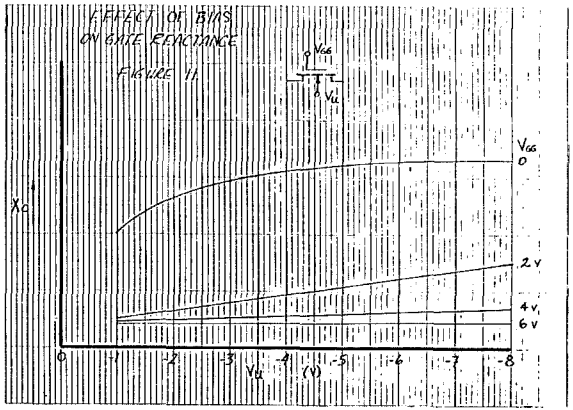
FIGURE 9



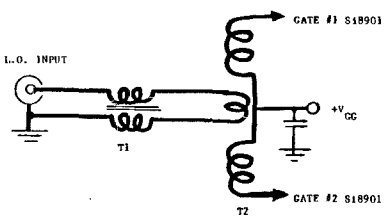


LOCAL OSCILLATOR DRIVE USING CONVENTIONAL BROADBAND TRANSFORMERS

FIGURE 10

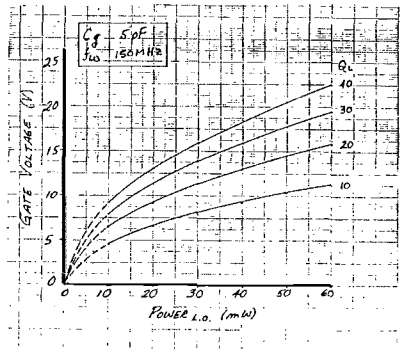


EFFECT OF BIAS AND SUBSTRATE VOLTAGE ON
GATE REACTANCE
FIGURE 11

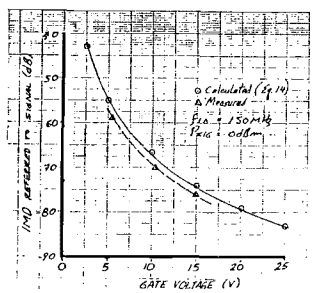


RESONANT-GATE DRIVE TRANSFORMER, T2, IS TUNED
TO RESONATE WITH C_{GG} OF S18901

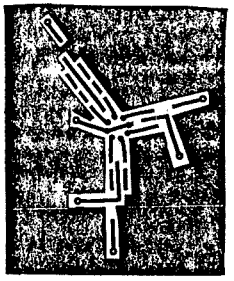
FIGURE 12



INFLUENCE OF LOADED Q ON GATE
VOLTAGE VERSUS L.O. POWER
FIGURE 13



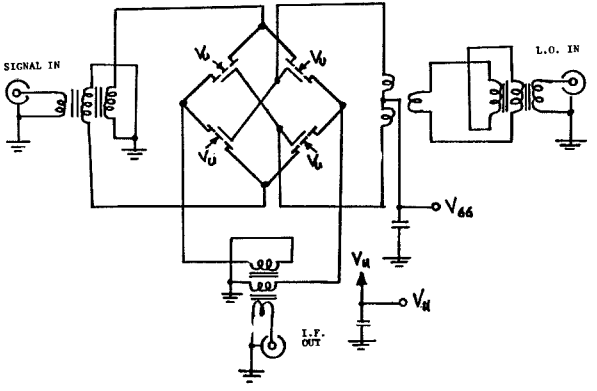
EFFECTS OF GATE VOLTAGE ON
INTERMODULATION DISTORTION
FIGURE 14



MASK LAYOUT — PRINTED CIRCUIT BOARD

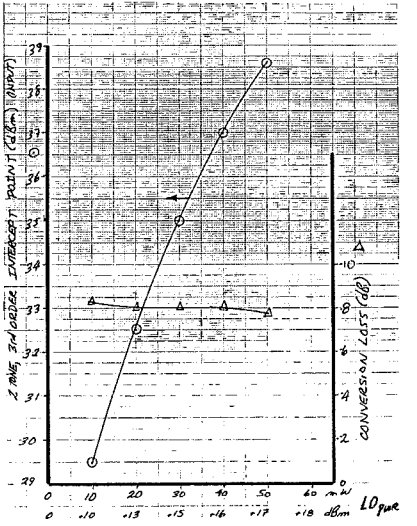
PROTOTYPE BALANCED MIXER

FIGURE I5



SCHEMATIC - COMMUTATION DOUBLE-BALANCED MIXER

FIGURE 16



INPUT INTERCEPT POINT & CONVERSION LOSS

FIGURE 17

MAXIMIZING CRYSTAL OSCILLATOR FREQUENCY STABILITY

by

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INTRODUCTION

Frequency stability is one of the central topics in the study of crystal oscillators, for the exceptional stability of quartz crystals is their fundamental advantage over other resonators. Both the long term and short term stability of crystal oscillators is important. Long term stability, characterized by terms such as "drift" or "ageing", is the systematic, non-random change in frequency with time, often expressed in terms of frequency change per day or per year. Short term stability is the random, noise-like behavior of the output frequency. In a measurement system based on a frequency counter (time domain), the short term stability is typically measured over gate times from milliseconds to seconds. The same random behavior of the frequency, but measured in a system based on a spectrum analyzer (frequency domain), is often specified in terms of the single-sideband level (relative to the carrier) of the angle modulation noise sidebands, at video frequencies from fractions of a Hertz to tens of Megahertz.

The studies which have been done on this topic fall into two groups: Studies of the crystal by itself, and analysis of crystal oscillator behavior. The former are often concerned with the theory of quartz resonators and with practical considerations concerning surface preparation, electrodes, cleanliness, new designs, etc. The latter include studies and experiments with the various oscillator configurations, such as the Colpitts, Clapp, Pierce, Butler, etc.

In the study of crystal oscillator stability, it is critical to examine the oscillator and circuit together. Particularly when considering short term stability, conclusions based on observations of the crystal alone can lead to erroneous results. In order to examine the crystal-circuit relationship in some detail, this study is confined to one particular oscillator configuration. However, insights obtained from the particular case will allow conclusions which are useful in the general. Exact equations for the crystal are used, and computer numerical methods are used to generate the various reactances and, even more important, the derivatives of these reactances.

For the purpose of analyzing the stabilizing effect of the crystal on the rest of the circuit, assume that the crystal is

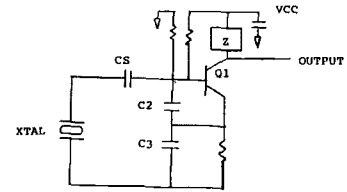
perfectly stable. In fact, certain *noisy processes are associated* with the crystal itself, and crystal frequency dependance on temperature and time is well known.

THE CIRCUIT

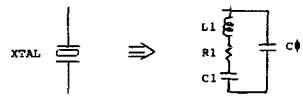
Figure 1a shows the circuit chosen for the analysis of the relationship between crystal , circuit, and frequency stability. The oscillator configuration is the popular Colpitts. Although the Colpitts is a grounded collector type of circuit, a small impedance in the collector provides a convenient signal output point and at frequencies of 10 MHz and lower this impedance has little effect on the oscillator base-emitter circuit.

THE CRYSTAL

Figure 1b shows the equivalent circuit of the frequency control crystal. The series circuit of C1, L1 and R1 represent the electrical equivalent circuit of the piezoelectric coupled mechanical resonance of the crystal. The reactances of C1 and L1 are orders of magnitude larger than that which would be obtained from electrical components, and the ratio of these reactances to R1, the loss term, or Q, is typically 60,000 to 1,000,000; again, three or more orders of magnitude larger than what can be obtained from electrical capacitors and inductors. C0 represents the parallel plate capacitor formed by the crystal electrodes. Typical values for a 10 MHz fundamental crystal are noted in the figure.



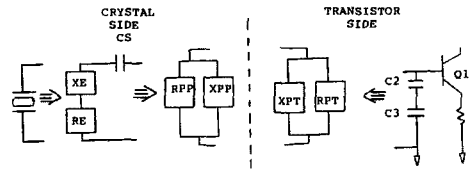
1.a.



1.b.

EXAMPLE

F1= $\frac{1}{2\pi\sqrt{L1C1}}$ = 10 MHZ
C1= .02 PICOFARADS
L1= 12.665 MILLIHENRY
R1= 20 OHMS
C0= 3.8 PICOFARADS



FOR STABLE OSCILLATION: XPP = -XPT; RPP = -RPT

1.c.

Figure 1a, b, c The Circuit

THEORY OF OSCILLATION

The crystal, capacitors CS, C2, and C3, plus the transistor reactances form a parallel resonant network at frequency F. The transistor provides gain, enough to offset the losses in the resonant circuit. It is useful for the present analysis to divide the circuit into the two parts shown in Figure 1c. The crystal, plus capacitor CS can be analyzed as a net inductive reactance XPP and parallel resistance, RPP. The transistor and C2 plus C3 are analyzed as a single parallel capacitive reactance and a parallel negative resistance, resulting from transistor gain. The circuit oscillates at a frequency where the positive (inductive) reactance of the crystal "side" equals the negative (capacitive) transistor "side". At turn-on, the negative resistance RPT developed by the transistor (connected to the complete tuned circuit) is of a lower value than the positive loss factor RPP. The net resistance is therefore negative, and oscillation begins. The amplitude of the oscillation builds to the point where some amplitude dependant gain factor, such as transistor saturation, lowers the gain and raises the effective negative resistance to exactly equal RPP, the condition necessary for steady state oscillation.

This establishes the conditions for the analysis. The following sections show that over the very narrow frequency range of inductive reactance of the crystal, the capacitive reactance of XPT is essentially constant and therefore oscillation occurs at the "intersection" of the value of XPT and the rapidly changing XPP. The stability of oscillation depends on this relationship.

THE REACTANCE CURVE

Figure 2 shows graphically* the steep rise of the parallel reactance and resistance curves due to the crystal, plotted as a function of frequency. As mentioned above, over the narrow frequency range depicted (.2%), the capacitive reactance of XPT is essentially constant. Therefore, the capacitance associated with the XPT value can be assigned to the right hand vertical scale. If, for example, we choose C2=C3=40 pF, then CT=20 pF, and the frequency of oscillation will be at point B.

The pertinent question is where we would choose to operate for best stability, but two forbidden regions must be discussed first. Practical circuit considertions including parasitic reactances and active device capacitances limit the maximum reactance of operation. In Figure 3, the boundary above which it is impractical to operate is arbitrarily chosen as 8,000 ohms, or 2 pF.

The exact values are unimportant because this is not the region of optimum stability. The other boundary, which is important, is determined by RPP, the equivalent parallel resistance.

* Equations in Appendix

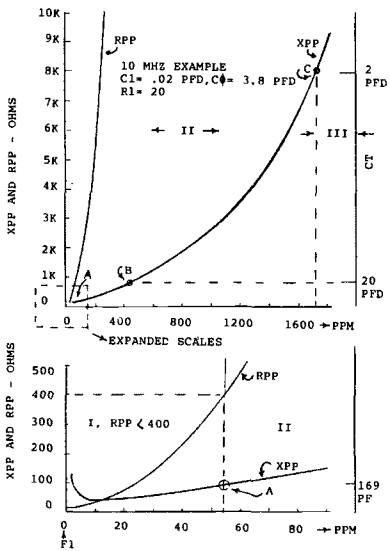


Figure 2, XPP, RPP

As discussed above (Theory of Oscillation), negative resistance is the model chosen to represent the gain relation between the transistor and the circuit. This resistance depends on the transistor characteristics and the values and ratio of C2 and C3. At present, it is important only to note that a minimum value of RPT (maximum gain), exists for any circuit value choice. Clearly, the circuit will not oscillate if RPP on the crystal side is less than RPT generated on the transistor side, so a boundary exists.

In the example, 400 ohms has been chosen as the boundary, so the circuit must operate somewhere between point A and point C. Where shall the greatest stability be obtained? If the crystal side only is considered, one might be tempted to choose point C, since the derivative of XPP with respect to frequency is highest at this point. To resolve the question, one must examine the transistor side in greater detail and determine the form of the unstable reactance.

THE TRANSISTOR SIDE

Recall from Figure 1 that the transistor side is defined as containing the capacitors C2 and C3 and the transistor itself. The admittance of this side will have real and imaginary parts as shown in that figure. The real part will be a negative

Since RPT depends on C2, C3 and C2/C3, the boundary between I and II is actually a curved line.

conductance of value 1/RPT and the imaginary a positive susceptance B=1/XCT parallel (the defining equations are shown in the Appendix.)

It is beyond the scope of this paper to quantitatively model and analyze the various long and short term instabilities on this side of the circuit. Rather, some systematic and random processess will be postulated, and the form of the circuit reactance instabilities will be shown. Armed with these models we can join the left and right sides of the circuit to describe the parameter that determines frequency stability.

CASE 1

The first model assumes that C parallel has a tolerance on its average value which varies this value with time, temperature, or other systematic function. In this case

$$C = CT * (1 + e) \qquad (1.6.1)$$

Where e represents the delta change from nominal (temperature, tolerance, etc.). The incremental reactance change, DX, due to e is then:

$$DX = 1/(2\pi FCT) - 1/(2\pi FCT(1+e)) \qquad (1.6.2)$$

$$DX = (1-(1-e))/(2\pi FCT) \qquad (1.6.3)$$

$$DX = e/(2\pi FCT) = XT * e \qquad (1.6.4)$$

CASE 2

Assume that the parallel capacitor CT has a fixed, stable part in parallel with a small variable capacitor CV which represents all of the instability or noisy portion of the circuit.

$$DX = XT - XT*XCV/(XT+XCV) \qquad (1.6.5)$$

$$DX = (XT)^2/(XT+XCV) \qquad (1.6.6)$$

For XCV >> XN:

$$DX = (XT^2/XCV) = (XT)^2*(2\pi FCV \qquad (1.6.7)$$

CASE 3

Assume that the current generator gm * Ib has a quadrature noise component $\overline{in}\ \angle 90^\circ$

The noise current into the base is derived in appendix B as:

$$\overline{iin} = \overline{in}/(1+X2/X3+gm*X2) \qquad (1.6.8)$$

Assuming gm * X2 >> (1 + X2/X3):

$$\text{then } |\overline{iin}| \doteq \overline{in}/(gm * X2) \qquad (1.6.9)$$

The "noisy reactance", XN, which would cause this current to flow is:

$$XN = gm * X2 * es / \overline{in} \qquad (1.6.10)$$

Where es is the oscillator voltage at the base. Then

$$DX = XT - XT*XN / (XT+XN) \qquad (1.6.11)$$

$$= (XT)^2 / (XT+XN) \qquad (1.6.12)$$

for XN >> XT

$$DX = (XT)^2 * \overline{in} / (es * gm * X2) \qquad (1.6.13)$$

for X2 = K * XT (1.6.14)

(1.6.13)

$$DX = XT^2 * \overline{in} / (K * es * gm) \qquad (1.6.15)$$

Summarizing the three cases

(1) $DX = (XT) * e$ (1.6.16)

(2) $DX = (XT)^2 * (2\pi F) * CV$ (1.6.17)

(3) $DX = (XT) * \overline{in} / es * gm * K$ (1.6.18)

Now we turn back to the complete circuit to find the form of delta frequency, DF.

DELTA FREQUENCY

The reactance curve of Eq. A6 plotted in figure 2 has a slope of DX/DF ohms per PPM. If one assumes an "operating" point of XT, then the frequency instability at that point will be:

$DF = [1/DX/DF] * DX$ (1.7.1)

Going back to the three cases developed in section 1.6, and substituting XPP=XPT=XT (condition of resonance),

$DF = [1/((DX/DF) * (1/XPP))] * e$ (1.7.2)

$DF = [1/((DX/DF) * [1/(XPP)^2))] * (2\pi F) * CV$ (1.7.3)

$DF = (1/((DX/DF) * [1/XPP))] * \overline{in}/(gm*es*K)$ (1.7.4)

These are the functions which yield the value of DF, the frequency instability of the total circuit, for the three cases of the preceding section. The quantities to the right of the brackets are constants determined by the degree of instability on the transistor side. The two functions in the brackets (one and three are the same) are determined by the crystal, the capacitor CS, and the value of the XT, the parallel reactance. In order to minimize delta frequency, we wish to maximize the inverse of these, which are,

I $(DX/DF)*1/XPP$ (1.7.5)

II $(DX/DF)*1/(XPP)^2$ (1.7.6)

These functions will be called the fractional reactance slope. Type I and Type II, to emphasize the fact tht it is the *fractional slope* which determines stability, not the absolute slope. In Figure 3, the fractional reactance slope functions and the reactance slopes have been plotted for a number of example cases, including the 10 MHz crystal of Figure 2, 5 MHz third overtone, and a 60 MHz third overtone. The functions are maximum at the lower boundary. The intuitively attractive steep slope at point "C" in Figure 2 is now shown to be deceptive because of the role of fractional slope in stability.

The effect of R1 and Q now becomes clear. The fractional reactance slope depends on XC1 of the crystal, so for all other factors equal, one always wants to maximize that. But best stability is found at the lowest reactance, and that occurs at a value determined by RPP which depends on R1, the crystal series

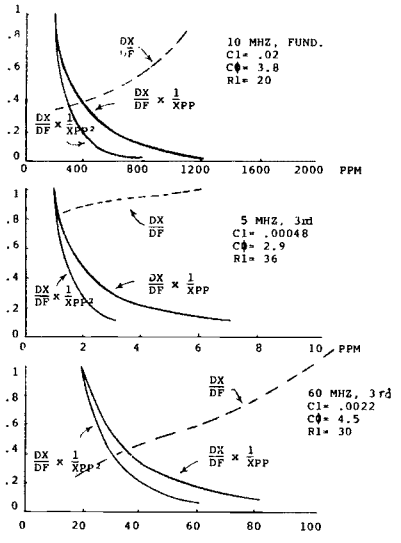


Figure 3. Relative Slopes

resistance. The crystal resistance determines stability indirectly by restricting the "operating" point of the circuit.

SERIES CAPACITANCE

Can one improve frequency stability by putting a capacitor in series with the crystal? The intuitive answer to this recurring question goes as follows (refer to Figure 2). The slope, DX/DF, increases with frequency but the fractional reactance slope decreases with frequency. At points A and B then,

Table 1.8.1

	PPM	RPP	XPP	DX/DF	TYPE I DX/(DF*XPP)	TYPE II $DX/(DF*XPP^2)$
A	55	402	94	1.58	1.68E-2	1.79E-4
B	440	25K	841	2.29	2.7E-3	3.2E-6

so better stability is obtained at A. If one adds a capacitor of reactance -747 ohms in series with the crystal, the entire curve is shifted in the negative direction. Is not now the reactance at F = 440 PPM equal to 841 minus 747 or 94? And since the curve is simply shifted, have we not now the DX/DF of point B but at the reactance of point A? Table 1.8.2 shows the results of adding a 21.3 pFd capacitor.

TABLE 1.8.2

	PPM	RPP	XPP	DX/DF	TYPE I DX/(DF*XPP)	TYPE II DX/(DF*XPP)
C	436	227	94	2.04	2.17E-2	2.31E-4
D	444.4	402	112	2.14	1.91E-2	1.71E-4

Several things have happened. At XPP equal 94 ohms, point C, RPP now equals 277 ohms, so this point violates the lower boundry of 400 ohms. Adjusting XCT to 112 ohms (changing CT), point D, gives RPP equal 402 ohms. DX/DF is now 2.14 so the fractional reactance slope (I) is 1.91E-2. The stability has been improved by about 14 percent for type I instabilities, compared to point A. But the type II fractional reactance slope is decreased by about 5 percent. So the answer for this particular example depends on the exact nature of the circuit instabilities. Note that this example assumes a perfect capacitor for CS. If CS were a varactor diode it is apparent that as the value decreases it is possible to move to a point where RPP is too low for oscillation. In VCXO designs then, the margin for oscillation should be adjusted at minimum capacity.

CONCLUSION

For several models of transistor and circuit instabilities it is seen that frequency stability is maximized when the fractional reactance slopes, Type I and Type II, are maximum. For a number of crystal examples these functions are maximum at the lowest parallel reactance. The minimum reactance point depends on the value of RPT, the parallel negative resistance. The effect of a capacitor in series with the crystal on stability depends on the exact nature of the circuit instabilities.

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APPENDIX A, EQUATIONS

CRYSTAL

$$X1 = XL1 + XC1 \;;\quad F1 = 1/2\pi\sqrt{(L1 + C1)^{.5}} \tag{A1}$$

$$= j2\pi F / ((2\pi F1)^2 * C1) - j/(2\pi F * C1) \tag{A2}$$

$$XO = -j / 2\pi F * CO \tag{A3}$$

CRYSTAL SERIES EQUIVALENT

$$XE = XO*((R1^2 + X1*(XO + X1))/(R1^2 + (XO + X1)^2) \tag{A4}$$

$$RE = R1/((R1/XO)^2 + ((XO + X1)/XO)^2) \tag{A5}$$

PARALLEL: XPP and RPP from RE and XE + XCS

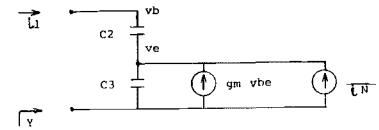
$$XPP = (RE^2 + (XE + XCS)^2)/(XE + XCS) \tag{A6}$$

$$RPP = (RE^2 + (XE + XCS)^2)/RE \tag{A7}$$

DERIVATIVES: COMPUTER CALCULATED INCREMENT

$$DXPP = XPP @ F - XPP @ (F\text{-}freq.\ increment) \tag{A8}$$

APPENDIX B, TRANSISTOR MODEL



$$i1 = vb*1/(1 + x2/x3 + gm*x2) + \overline{in}/(1+x2/x3 + gm*x3) \tag{B1}$$

$$Y = i1/vb = 1/RPT + 1/XCT \tag{B2}$$

$$RPT = gm*x2*x3 + (x2 + x3)^2/gm*x2*x3 \tag{B3}$$

$$XCT = ((x2 + x3)^2) - (gm*x2*x3)^2))/(x2 + x3) \tag{B4}$$

$$\dot{XCT} = x2 + x3 \tag{B5}$$

$$\overline{\dot{in}} = \overline{in}/(1 + x2/x3 + gm*x2) \tag{B6}$$

$$\overline{\dot{in}} = \overline{in}/gm*x2 \tag{B7}$$

$$\dot{XN} = es/in = gm*x2*es \tag{B8}$$

DIELECTRIC RESONATOR FILTERS FOR UHF AND MICROWAVE APPLICATIONS

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ABSTRACT

Simplified design methods for dielectric resonator bandpass and bandstop microwave filters are discussed. Two typical cases of dielectric resonator operation in the filter circuit, single- and dual-mode, are considered. Some practical filter realizations suitable for UHF and microwave applications are also described.

1. INTRODUCTION

Considerable advances have been made over the last decade in technology of low-loss and temperature stable ceramic materials suitable in a high-frequency filter applications. Low-loss (or high Q), large dielectric constant, and low frequency-temperature coefficient are the most significant features of temperature compensated ceramic materials that make them very attractive for filter applications at UHF and microwave frequencies [1].

Typically, these filters employ a cylindrical or rectangular shaped dielectric resonator as a basic element in the bandstop, bandpass, and directional filter realizations. A dielectric resonator filter operation is based on a specific mode of dielectric resonator at which the coupling between resonators and distributed transmission medium can be realized and practically controlled in order to obtain the desired filter characteristics. Depending upon applications and frequency range the dielectric resonator filters use a rectangular waveguide, cylindrical waveguide, coaxial line, or microstrip line for transmission medium [2]. Typically, at the UHF frequencies the TEM coaxial transmission lines containing the dielectric ring resonator are most often used for the bandpass filter realizations [3]. At microwave and millimeter wave frequencies the waveguide or microstrip line are mainly used as transmission media since their fundamental propagation modes are compatible with the $TE_{01\delta}$ mode of dielectric resonator [1], [2].

The objective of this paper is to present a brief outline of dielectric resonator filter design methods and to discuss some practical design considerations related to bandpass and bandstop filter realizations.

2. PRACTICAL DESIGN OF SINGLE-MODE DIELECTRIC RESONATOR FILTERS

Band-pass and band-stop filter design procedures are based on the low-pass prototype element model and a low-pass to band-pass or band-stop frequency mapping as described in [4]. All subsequent steps of the design procedure are outlined in Figure 1. It can be seen from Figure 1 that both maximally flat (or Butterworth) and equi-ripple (or Tchebyscheff) responses can be obtained following the design procedure outlined. It also follows that for the determination of a filter components, the dielectric resonator parameters required for a given circuit topology, such as the external Q's, Q_{ex}, and coupling coefficient k_i must be determined first. The Q_{ex}'s and k's values related to the physical dimensions of the filter can be obtained either analytically or expermintally or by combination of these two techniques.

With the reference to the band-pass filter equivalent circuit shown in Figure 2 the external Q, Q_{ex} and coupling coefficientds K_i's are functionally related to the circuit elements as follows [4]

$$Q_{ex1} = X_1/(K_{01}^2/R_1) = g_0\, g_1\, \omega_1'/W \qquad (1a)$$

$$Q_{ex_n} = X_n/(K_n^2,\ n+1/R_n) = g_n\, g_{n+1}\, \omega_1'/W \qquad (1b)$$

and

$$K_{i,\,i+1} = K_{i,\,i+1}\, 1/\sqrt{X_i,\ X_{i+1}} = W/\omega_1'\ \sqrt{g_i\, g_{i+1}} \qquad (2)$$

where $W = (\omega_2 - \omega_1)/\omega_o$ is the fractional bandwidth

ω_o is the center frequency of B-P filter

ω_i is the edge frequency of L-P prototype filter

$g_0, g_1, \ldots g_i, g_{i+1}, \ldots g_n, g_{n+1}$ are the elements of a L-P prototype filter.

It is essential, however, for a proper design to have the Q_{ex}'s and k's parameter values expressed in terms of the filter physical structure and dielectric resonator parameters.

In the most common case of the $TE_{01\delta}$ operation mode of cylindrical dielectric resonator being integrated with the waveguide or microstripline, approximate equations for the resonant frequency f_o, and unloaded Q factor, Q_o have been derived and practically verified in various designs [5], [6], [7].

However, there is no approximate expression available for a coupling coefficient, k, nor for resonator-to-resonator, nor transmission line-to-resonator coupling arrangements. Therefore, the best way in practice is to determine k from the external Q factor measurements for a pratical circuit structure, as any attempt to determine the coupling coefficient k value from analysis inevitably leads to rather complex algebra requiring the use of a computer to get the final solution.

If the Q_{ex} is obtained from measurements and the unloaded, Q, Q_o is for example determined analytically, then the coupling factor k can be obtained from

$$k = Q_o/Q_{ex} \tag{3}$$

Considering a typical filter structure of the form shown in Figure 3 (a) and (b) the unloaded Q factor can be calculated using [5]:

$$Q_o = \frac{\varepsilon_r a + \varepsilon_g b_a d_g + b_a d_a}{\varepsilon_r a \tan \sigma_r + \varepsilon_g b_a d_g \tan \sigma_g + R\lambda_o^2 d_r/2s^2} \tag{4}$$

Where the meaning of constants in (4) can be explained with the reference to Figure 3 as follows:

$$a = t + \sin(\gamma_r t)/\gamma_r$$

$$b_g = [\cos(\gamma_r t/2)/\sinh(\gamma_g s)]^2$$

$$b_a = [\cos(\gamma_r t/2)/\sinh(\gamma_a d)]^2$$

$$d_g = \sinh(2\gamma_g s)/2\gamma_g - s$$

$$d_a = \sinh(2\gamma_a d)/2\gamma_a - d$$

$$d_r = \sqrt{b_g b_a}\left[\frac{\gamma_g \sinh(\gamma_a d)}{\sinh(\gamma_g s)} + \frac{\gamma_a \sinh(\gamma_g s)}{\sinh(\gamma_a d)}\right]$$

where

$$\gamma_r = \left[\left(\frac{\omega_o}{c}\right)^2 \varepsilon_r - \left(\frac{u}{R}\right)^2\right]^{\frac{1}{2}} \tag{5a}$$

$$\gamma_g = \left[\left(\frac{2.405}{R}\right)^2 - \left(\frac{\omega_o}{c}\right)^2 \varepsilon_g\right]^{\frac{1}{2}} \tag{5b}$$

$$\gamma_a = \left[\left(\frac{2.405}{R}\right)^2 - \left(\frac{\omega_o}{c}\right)^2 \varepsilon_o\right]^{\frac{1}{2}} \tag{5c}$$

where the parameter u in (5a) can be approximated as follows:

$$u = 2.32 + \sqrt{0.033 R^2 \left(\frac{\omega_o}{c}\right)^2 - 0.185} \tag{6}$$

under the assumption that $\varepsilon_r \gg 1$, which holds for most dielectric resonators.

In order to assure that the filter circuit shown in Figure 3 is a bandpass type, which means that the RF power flow through the circuit relies on the presence of the $TE_{01\delta}$ mode of dielectric resonators, the metallic enclosure must act as a waveguide under cut-off conditions at the filter operated frequency. Otherwise, the circuit will operate as the bandstop filter with the signal power absorbtion at the frequency corresponding to the dominant $TE_{01\delta}$ mode (or possibly on some other adjacent hybrid modes).

In either case the resonant frequency of the circuit including the dielectric resonator operated in the $TE_{\delta lm}$ mode may be determined using the transmission line equivalent circuit model introduced in [5] and [6]. For example, the frequency, f_o, of the structure shown in Figure 3(b) basically depends on the dielectric resonator parameters such as D - diameter, L - height, and dielectric permittivity ε_r being also a function of the circuit parameters described by the following two equations:

$$\gamma_r L = \tan^{-1}\left(\frac{\gamma_a}{\gamma_r}\coth(d\,\gamma_a)\right) + \tan^{-1}\left(\frac{\gamma_s}{\gamma_r}\coth(s\gamma_s)\right) \qquad (7)$$

and

$$\frac{J_1(u)}{u\,J_o(u)} = -\frac{K_1(W)}{W\,K_o(W)} \qquad (8)$$

where J_o and J_1 are Bessel functions of the first kind of nth order, while K_n is the modified Hankel function of the nth order. The γ_a, γ_r, and γ_s propagation parameters are defined by (5), with the u given by (6).

The following approximation can be used to simplify Eq. (2) [7]:

$$\frac{J_1(x)}{x\,J_o(x)} \approx \frac{0.23}{(x-2.405)^{1.5}} \quad \text{for} \quad 2.405 < x < 3.83$$

$$\therefore \quad \approx \frac{0.08}{(x-5.52)^{1.3}} \quad \text{for} \quad 5.52 < x < 7.02$$

$$\text{etc} \qquad (9)$$

and

$$\frac{K_1(x)}{x\,K_o(x)} \approx \frac{2.06}{x^{1.3}} \qquad (10)$$

with

$$W = \sqrt{\left(\frac{\omega_o}{c}\right)^2 R^2 \varepsilon_r - u^2} \qquad (11)$$

Equations (7) to (11) can be used to determine the f_o value when the circuit's and dielectric resonator's parameters are known, or if the f_o is given to find the dielectric resonator parameters (the height L, for example) incorporated with a given circuit structure. In either case the calculations are carried out using a standard iteration method which leads to solution. Therefore, it is customary to asume an initial value for the dielectric resonator diameter D which would reduce the computation time, for example , an initial value for D can be determined from the following equation:

$$D = 2.405\,\frac{c}{\omega_o}\left[\varepsilon_r^{-\frac{1}{2}} + \varepsilon_a^{-\frac{1}{2}}\right] \qquad (12)$$

The resonant frequencies determined from measurements and the analysis using Eq. (7) - (11) for different values of a distance d are shown in Figure 4. The agreement between the

results obtained is very good. It can be observed from Figure 4 that the resonant frequency, f_o is sensitive to the change of distance, d, which in practical filter realizations can be used for frequency tuning. The unloaded Q factor, Q_o for the resonator incorporated in the structure shown in Figure 4 was 3000 determined from measurements and 2200 using Eq (4), both at frequency 10GHz.

The band-pass filter for operation at 10 GHz center frequency has been designed using two identical dielectric resonators (with the parameters shown in Figure 4) to obtain maximally flat (Butterworth) transfer characteristic with the 3 dB bandwidth of 50 MHz. The filter was made in the form shown in Figure 3. With the 50 ohm terminations the filter has an external Q factor, $Q_{ex} = 380$.

The low pass filter prototype elements used in computation were: $g_o = g_3 = 1$ and $g_1 = g_2 = \sqrt{2}$, and the coupling coefficient k_{12} between resonators was approximately equal to 3.5×10^{-3}, corresponding to the spacing 1 between resonators of 4.2 mm. The distance d between the top wall of the resonator metallic enclosure and the upper surface of each resonator has been set at 0.5 mm. A good agreement between the designed and measured characteristics of the filter has been obtained. The filter insertion loss within the pass-band determined experimentally was 1.7 dB at 10 GHz.

An example of another band-pass or band-stop filter realization is shown in Figure 5. This filter realization employes axially coupled cylindrical resonators suspended in the circular waveguide which is furnished with two coaxial couplings. Each resonator has a small centre hole to accommodate the coaxial arrangement of the filter structure. The hole diameter, d_i must be much smaller in comparison with the diameter of dielectric resonator, D to assure almost undisturbed propagation of the $TE_{01\delta}$ mode. It has been found that the presence of a small hole in the centre of dielectric resonator helps to better separate the HE modes from the operational $TE_{01\delta}$ mode [8]. The input/output coaxial coupling probes are usually adjusted experimentally for an optimal coupling condition.

The coupling coefficient, k between resonators may be determined using the following formula, provided that $d_i \ll D$;

$$k = \frac{F}{2\pi d_e^4} \sum_{n \geq 1} \frac{U_{on}^2}{A_n^2} B_n \frac{e^{-\alpha_{on} s}}{\alpha_{on}} \qquad (13)$$

where

$F = 15.2 \frac{D^4 L}{\lambda_o^2} \epsilon_r \text{ (cm)}^3$ with the assumption that,

$0.25 < L/D < 0.7$

λ_o is the free space wavelength corresponding to the resonant frequency f_o.

$A_n = 1 - (U_{on} D/2 p_{01} d_e)^2$ is the resonator/circuit parameter

U_{on} are the roots of Bessel function: $J_1(u) = 0$, i.e.,

$U_{01} = 3.832$, $U_{02} = 7.016$, etc.

with $n = 1$ for $s > 0.6$

and $n = 2$ for $0.16 < s < 0.6$

$s = 1 + L$ is the center-to-center spacing between resonators.

$p_{01} = 2.405$ is the first root of Bessel function: $J_0(u) = 0$

$\alpha_{on} = \frac{2\pi}{\lambda_{on}} \left[1 - (\lambda_{on}/\lambda)^2\right]^{\frac{1}{2}}$ is the attenuation constant

of TE_{on} mods ($\lambda_{01} = 1.64\, d_e$, $\lambda_{02} = 0.896\, d_e$, etc)

$B_n = J_o^2 (U_{on} D/2 d_e)/J_o^2 (U_{on})$ is the ratio of a squared Bessel functions (zero order).

Equation (13) is typically solved for the s value with the values of coupling coefficients k's constrained by the low-pass filter prototype parameters and the remaining circuit parameters intially pre-determined (including dielectric resonators). The dielectric resonator parameters; D, L, d_i and ϵ_r, should be computed first based on the resonant frequency, f_o, required for the filter in both band-pass and band-stop designs.

3. PRACTICAL DESIGN OF DUAL MODE DIELECTRIC RESONATOR FILTERS

The dual-mode dielectric resonator BP filter is a fairly new development in the microwave filter technology [9]. It is based on a dual- mode cavity approach which proved to be a very successful for the elliptic-type transfer characteristic realizations. The implementation of dielectric resonators into a classical dual- mode cavity filter leads to its weight and size reduction. A typical section of a dual-mode filter loaded by a cylindrical dielectric resonator is shown in Figure 6. The HE_{11} hybrid mode of dielectric resonator is employed in the filter operation. To design microwave cavity filters with dielectric resonators, determination of two basic factors; the resonant frequency of the cavity and coupling coefficients between

individual cavities or input/output coupling ports is necessary. With reference to the cavity shown in Figure 6 the resonant frequency, f_o, can be obtained by solving the following two equations [9].

$$\beta \tan(\beta L/2) \tanh(\Upsilon_o s) - \hat{\Upsilon}_o = 0 \qquad (14)$$

where $S = (T - L)/2$, and

$$\hat{\Upsilon} = \left[(1.841/B)^2 - k_o^2\right]^{\frac{1}{2}}$$

and

$$\left(\frac{\varepsilon_r}{p} A_1 J' + \frac{b_2}{h} J\right)\left(\frac{b_1}{h} J' + \frac{a_2}{h} J\right) - \frac{\beta^2}{k_o^2 z^2} a_1 b_1 J^2 \left(\frac{1}{p^2} + \frac{1}{h^2}\right)^2 = 0 \qquad (15)$$

where
$a_1 = K_b I_a - I_b K_a$
$a_2 = K_b' I_a - I_b' K_a$
$b_1 = K_b' I_a - I_b' K_a$
$b_2 = K_b' I_a - I_b' K_a'$
$J = J_1(hR)$
$I_a = I_1(pR)$, $I_b = I_1(pB)$
$K_a = K_1(pR)$, $K_b = K_1(pB)$

where $K_1(x)$ is modified Hankel function
$I_1(x)$ is modified Bessel function

with the primes denoting a differentiation in respect to argument and

$$h = (\varepsilon_r k_o^2 - \beta^2)^{\frac{1}{2}}$$
$$p = (\beta^2 - k_o^2)^{\frac{1}{2}}$$
$$\beta = \pi/L$$
$$k_o = \omega\sqrt{\mu_o \varepsilon_o} = 2\pi/\lambda_o$$

where λ_o is the free space wavelength corresponding to the resonant frequency f_o.

The coupling coefficient, k, between the cavity sections of the form shown in Figure 6 can be determined from the following equation.

$$k = \frac{\mu_o}{\varepsilon_o} M \frac{\left|\bar{H}_t\right|^2}{\int |\bar{E}|^2 dV} = 0.4082\, M \frac{(1.841/B)^2 \Upsilon_o^3}{k_o^2 \left[\sinh(\Upsilon T) - \Upsilon_o T\right]} \qquad (16)$$

where M is the magnetic polarizability of the coupling aperture.

Equation (16) can serve only as a good estimate of the coupling coefficient value, since in practice some adjustments of the coupling slot length, l, and its width, w, are necessary. A

fine tuning of the resonant frequency in each filter section shown in Figure 6 can be achieved by using metallic screw-tuners mounted on the cylindrical wall of the filter. A 4-pole, elliptical-type band-pass filter for operation at the center frequency of 4.2 GHz using the filter modules shown in Figure 6 has been recently reported [9]. This filter is currently used for the satellite communication applications.

4. CERAMIC MATERIAL COMPOSITIONS USED FOR DIELECTRIC RESONATORS

The first number in the parentheses corresponds to materials dielectric permittivity and the second one to the temperature coefficient of resonant frequency in ppm/°C.

- $Ba\ (Zn_{1/3}Nb_{2/3})O_3$ } $(38, \pm 4)$
- $Ba\ (Zn_{1/3}Ta_{2/3})O_3$ }
- $Ba\ Ti_4\ O_9$ (38, +18)
- $Ba_2\ Ti_9\ O_{20}$ (40, +2)
- (Zr, Sn) TiO_4 (~35, 20)
- (Ca, Sr)(Ba,Zr)O_3 (~30, 50)

Typical values of Q's for the dielectric resonators using above ceramics are in the range of 5000-10000 at 10 GHz.

5. CONCLUSION

Design aspects of the bandpass and bandstop filters using dielectric resonators for microwave and UHF applications have been discussed. Some practical filter realizations have been presented. Due to their relatively small size and light weight, they are ideally suited for operation in the space technology applications. These filters also offer excellent temperature stability and can be developed at a low cost.

It has been also shown that both types of filters discussed in the paper can be designed using standard filter synthesis method.

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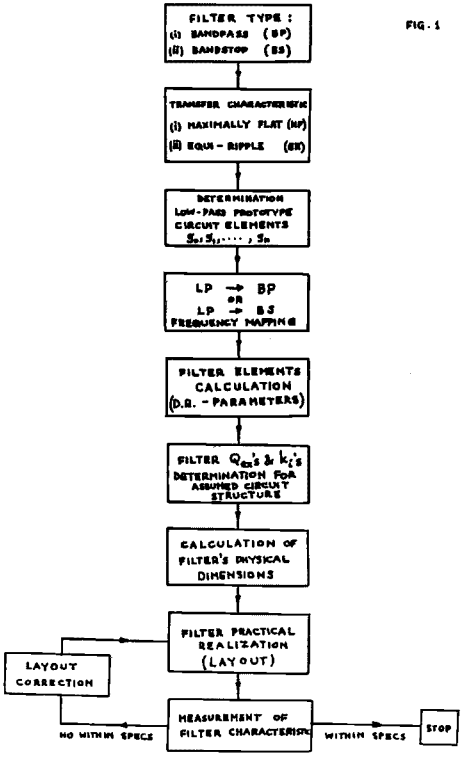

FIG. 1

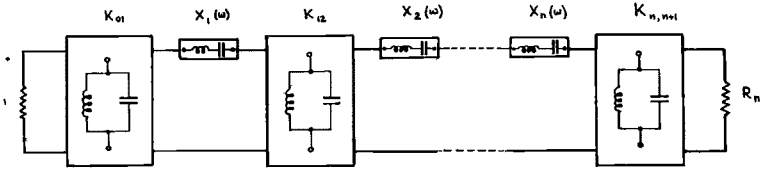

FIG. 2

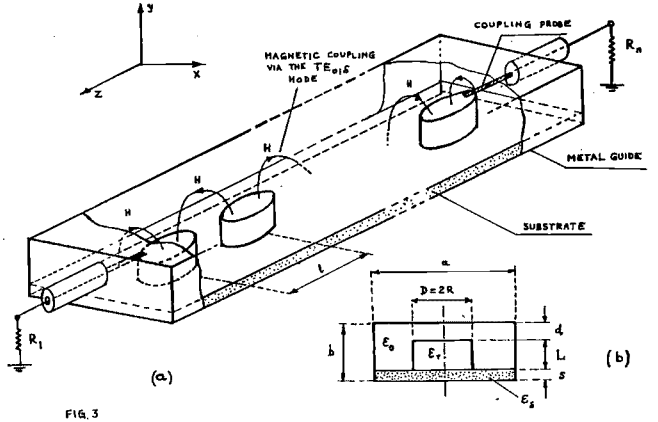

FIG. 3

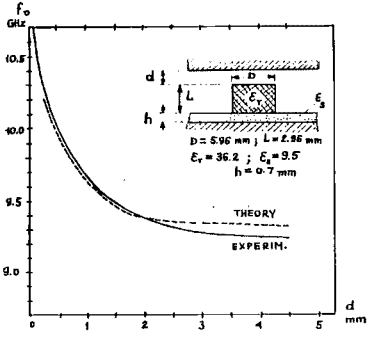

FIG. 4

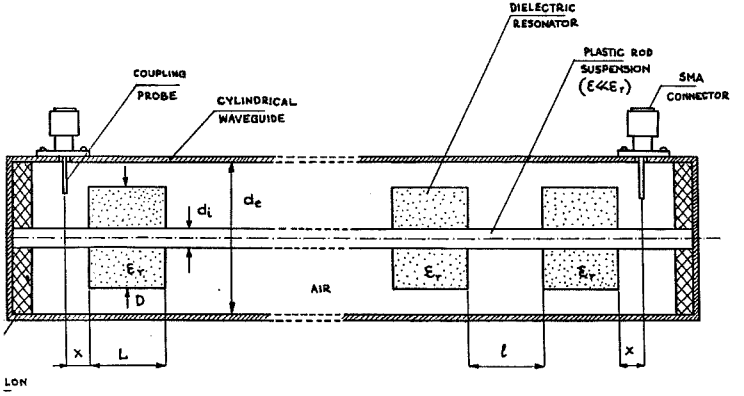
DIELECTRIC RESONATOR
PLASTIC ROD SUSPENSION ($\varepsilon \ll \varepsilon_r$)
SMA CONNECTOR
COUPLING PROBE
CYLINDRICAL WAVEGUIDE
d_i
d_e
ε_r
D
AIR
X
L
l
x
LON

FIG. 5

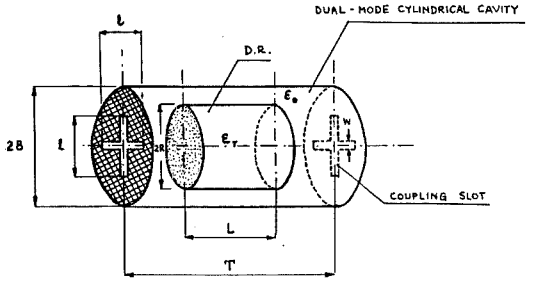
DUAL - MODE CYLINDRICAL CAVITY
l
D.R.
ε_o
2B
ε_r
W
COUPLING SLOT
L
T

FIG. 6

UNDERSTANDING RF TRANSISTOR DATA SHEET PARAMETERS

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INTRODUCTION

Data sheets often are the sole source of information about the capability and characteristics of a product. This is particularly true of RF transistors that are used throughout the world. Thus it is important that the user and the manufacturer of a product speak a common language, i.e., what the semiconductor manufacturer says about a transistor is understood fully by the circuit designer.

This paper reviews RF transistor parameters from maximum ratings to functional characteristics. Comments are made about critical specifications, about how values are determined and what are their significance. A brief description of the procedures used to obtain impedance data and thermal data is set forth. The importance of test circuits is elaborated. Finally, comments are made about possible tradeoffs in device specifications and their importance to the circuit design engineer.

DC SPECIFICATIONS

Basically RF transistors are characterized by two types of parameters: DC and functional. The "DC" specs consist (by definition) of breakdown voltages, leakage currents, hFE (DC beta) and capacitances, while the functional specs cover gain, ruggedness, noise figure, Zin and Zout. Thermal characteristics do not fall cleanly into either category since thermal resistance and power dissipation can be either DC or AC. Thus, we will treat the spec of thermal resistance as a special specification and give it its own heading called "thermal characteristics." Figure 1 is one page of a typical RF power data sheet showing DC and Functional specs.

Breakdown voltages are largely determined by material resistivity and junction depths (Figure 2). Each junction voltage - collector/base and emitter/base - is generally specified at a current level that is well within the safe operating limits of a reverse biased junction. The specifications are conventional and generally standard throughout the semiconductor industry.

Leakage currents (defined as reverse biased junction currents that occur prior to avalanche breakdown) are likely to be more varied in their specification and also more informative. Many transistors do not have leakage currents specified because they can result in excessive (and frequently unnecessary) wafer/die yield losses. Leakage currents arise as a result of material defects, mask imperfections and/or undesired impurities that enter during wafer processing. Some sources of leakage currents are potential reliability problems; most are not. Leakage currents can be material related such as stacking faults and dislocations or they can be "pipes" created by mask defects and/or processing inadequacies. These sources result in leakage currents that are constant with time and if initially acceptable for a particular application will remain so. They do not pose long term reliability problems. On the other hand, leakage currents created by channels induced by mobile ionic contaminants in the oxide (primarily sodium) tend to change with time and can lead to increases in leakage current that render the device useless for a specific application. Distinguishing between sources of leakage current can be difficult which is one reason devices for application in military environments require HTRB (high temperature reverse bias) and burn in testing. However, even for commercial applications where battery drain is critical or where bias considerations dictate limitations, it is essential that a leakage current limit be included in any complete device specification.

DC parameters such as hFE and Cob (output capacitance) need little comment. Typically, for RF devices hFE is relatively unimportant because the functional parameter of gain at the desired frequency of operation is specified. Note, though, that DC beta is related to AC beta (Figure 3). Functional gain will track DC beta particularly at lower RF frequencies. Generally RF device manufacturers do not like to have tight limits placed on hFE. Primarily the reasons that justify this position are:

a) Lack of correlation with RF performance
b) Difficulty in control in wafer processing
c) Other device manufacturing constraints dictated by functional performance specs which preclude specific limits for hFE.

A good rule of thumb for hFE is to set a maximum to minimum ratio of not less than 3 with the minimum hFE value determined by an acceptable margin in functional gain.

Output capacitance is an excellent measure of comparison of device size (base area) provided the majority of output capacitance is created by the base-collector junction and not parasitic capacitance arising from bond pads and other top metal of the die. Remember that junction capacitance will vary with voltage (Figure 4) while parasitic capacitance will not vary. Also, in comparing devices, one should note the voltage at which a given capacitance is specified. No

industry standard exists. The preferred voltage at Motorola is the transistor Vcc rating, i.e., 12.5 volts for 12.5 volt transistors and 28 volts for 28 volt transistors, etc.

MAXIMUM RATINGS and THERMAL CHARACTERISTICS

Maximum ratings (shown for a typical RF power transistor in Figure 5) tend to be the most frequently misunderstood group of device specifications. Ratings for maximum junction voltages are straight forward and simply reflect the minimum values set forth in the DC specs for breakdown voltages. If the device in question meets the specified minimum breakdown voltages, then voltages less than the minimum will not cause junctions to reach reverse bias breakdown with the potentially destructive current levels that can result.

A maximum rating for power dissipation (Pd) is closely entwined with thermal resistance (θjc). Actually maximum Pd is in reality a fictitious number - a kind of figure of merit - because it is based on the assumption that case temperature is maintained at 25 degC. However, providing everyone arrives at the value in a similar manner, the rating of maximum Pd is a useful tool with which to compare devices.

The rating begins with a determination of thermal resistance - die to case. Knowing θjc and assuming a maximum die temperature, one can easily determine maximum Pd (based on the previously stated case temperature of 25 degC). Measuring θjc is normally done by monitoring case temperature (Tc) of the device while it operates at or near rated output power (Po) in an RF circuit. The die temperature (Tj) is measured simultaneously using an infra-red microscope (see Figure 6) which has a spot size resolution as small as 1 mil in diameter. Normally several readings are taken over the surface of the die and an average value is used to specify Tj.

It is true that temperatures over a die will vary typically 10-20 degC. A poorly designed die (improper ballasting) could result in hot spot (worst case) temperatures that vary 40-50 degC. Likewise, poor die bonds (see Figure 7) can result in hot spots but these are not normal characteristics of a properly designed and assembled transistor die.

By measuring Tc and Tj along with Po and Pin - both DC and RF - one can calculate θjc from the formula

$$\theta_{jc} = \frac{T_j - T_c}{P_{in} - P_o}$$

Typical values for an RF power transistor might be Tj=130 degC; Tc=50 degC; VCC=12.5 V; Ic=12 A; Pin (RF)=10 W; Po (RF)=80 W. Thus

$$\theta_{jc} = \frac{130 - 50}{10 + (12.5 \times 12) - 80} = \frac{80}{50} = 1\ ^{\circ}C/W$$

Several reasons dictate a conservative value be placed on θjc. First, thermal resistance increases with temperature (and we realize Tc=25 degC is NOT realistic). Second, Tj is not a worst case number. And, third, by using a conservative value of θjc, a realistic value is determined for maximum Pd. Generally Motorola's practice is to publish θjc numbers approximately 25% higher than that determined by the measurements described in the preceding paragraphs, or for the case illustrated, a value of θjc=1.25 degC/W.

Now a few words are in order about die temperature. Reliability considerations dictate a safe value for an all Au (gold) system (die top metal and wire) to be 200 degC. (1) Once Tj max is determined along with a value for θjc, maximum Pd is simply

$$P_D(max) = \frac{T_J(max) - 25\ ^{\circ}C}{\theta_{jc}}$$

Specifying maximum Pd for Tc=25 degC leads to the necessity to derate maximum Pd for any value of Tc above 25 degC. The derating factor is simply the reciprocal of θjc!

Maximum collector current (Ic) is probably the most subjective maximum rating on RF transistor data sheets. It can, and is, determined in a number of ways each leading to different maximum values. Actually three possible current limitations can exist in RF transistors. One is package related; one is wire related; and a third is die related. Most older, lower frequency transistors are wire and/or package limited which is why these parts generally have Ic max determined by the current handling capability of the emitter wires or by dividing maximum Pd by collector voltage (or by BVCEO for added safety). Most higher voltage parts (28V and 50V) tend to be wire limited and when operated at lower voltage can safely handle sizeable amounts of current. Lower voltage parts (7.5V and 12.5V), however, tend to be package limited and should have Ic max determined by power dissipation considerations.

(1)For a more thorough discussion of die temperature, θjc and reliability the reader is referred to "Thermal Rating of RF Power Transistors" by Robert Johnsen, Motorola Appl. Note #790

Most modern, high frequency transistors are die limited because of high current densities resulting from very small current carrying conductors and these densities can lead to metal migration and premature failure. The determination of Ic max for these types of transistors results from use of Black's equation for metal migration which determines a mean time between failures (MTBF) based on current density, temperature and type of metal. At Motorola, MTBF is generally set at >7 years and maximum die temperature at 200 degC. For plastic packaged transistors, maximum Tj is set at 150 degC. The resulting current density along with a knowledge of the die geometry and top metal thickness allows the determination of Ic max.

It is up to the transistor manufacturer to specify an Ic max based on which of three limitations (die, wire, package) is paramount. Note however the limitation depends to some extent on application. It is recommended that the circuit design engineer consult the semiconductor manufacturer for additional information if Ic max is of any concern in his specific use of the transistor.

Storage temperature is another maximum rating that is frequently not given the attention it deserves. A range of -55 degC to 200 degC has become more or less an industry standard. And for the single metal, hermetic packaged type of device the upper limit of 200 degC creates no reliability problems. However, a lower high temperature limitation exists for plastic encapsulated or epoxy sealed devices. These should not be subjected to temperatures above 150 degC to prevent deterioration of the plastic material.

FUNCTIONAL CHARACTERISTICS

Functional characteristics of an RF transistor are by necessity tied to a specific test circuit (an example is shown in Figure 8). Without specifying a circuit, the functional parameters of gain, reflected power, efficiency - even ruggedness - hold little meaning. Furthermore, most test circuits used by RF transistor manufacturers today (even those used to characterize devices) are designed mechanically to allow for easy insertion and removal of the device under test (D.U.T.). This mechanical restriction sometimes limits achievable device performance which explains why performance by users frequently exceeds that indicated in data sheet curves. On the other hand, a circuit used to characterize a device is usually narrow band and tunable. This results in higher gain than attainable in a broadband circuit. Unless otherwise stated, it can be assumed that characterization data such as Po vs frequency is generated on a point-by-point basis by tuning a narrow band circuit across a band of frequencies and, thus, represents what can be achieved at a specific frequency of interest provided the circuit presents optimum source and load impedances to the D.U.T.

Broadband, fixed tuned test circuits are the most desirable for testing functional performance of an RF transistor. Fixed tuned is particularly important in assuring everyone - the manufacturer and the user - of product consistency, i.e., that devices made tomorrow will be identical to devices made today.

Tunable, narrow band circuits have led to the necessity for device users and device manufacturers to resort to the use of "correlation units" to assure product consistency over a period of time. Fixed tuned circuits minimize (if not eliminate) the requirement for correlation and in so doing tend to compensate for the increased constraints they place on the device manufacturer. On the other hand, manufacturers like tunable test circuits because their use allows adjustments that can compensate for variations in die fabrication and/or device assembly. Unfortunately gain is normally less in a broadband circuit than it is in a narrow band circuit and this fact frequently forces transistor manufacturers to use narrow band circuits to make their product have sufficient attraction when compared with other similar devices made by competition. This is called "specsmanship." A good compromise for the transistor manufacturer is to use narrow band circuits with all tuning adjustments "locked" in place. In comparing functional parameters of two or more devices, then, the data sheet reader should be careful to observe the test circuit in which specific parameter limits are guaranteed.

For RF power transistors, the parameter of ruggedness takes on considerable importance. Ruggedness is the characteristic of a transistor to withstand extreme mismatch conditions in operation (which causes large amounts of output power to be "dumped" back into the transistor) without altering its performance capability or reliability. Many circuit environments particularly portable and mobile radios have limited control over the impedance presented to the power amplifier by an antenna, at least for some duration of time. In portables, the antenna may be placed against a metal surface; in mobiles perhaps the antenna is broken off or inadvertently disconnected from the radio. Today's RF power transistor must be able to survive such load mismatches without any effect on subsequent operation. A truly realistic possibility for mobile radio transistors (although not a normal situation) is the condition whereby an RF power device "sees" a worst case load mismatch (an open circuit, any phase angle) along with maximum Vcc AND greater than normal input drive - all at the same time. Thus the ultimate test for

ruggedness is to subject a transistor to a test wherein Pin (RF) is increased up to 50% above that value necessary to create rated Po; Vcc is increased about 25% (12.5 V to 16 V for mobile transistors) AND then the load reflection coefficient is set at a magnitude of unity while its phase angle is varied through all possible values from 0 degrees to 360 degrees. Many 12 volt (land mobile) transistors are routinely given this test at Motorola Semiconductors by means of a test station similar to the one shown in Figure 9.

Ruggedness tests come in many forms (or guises). Many older devices (and even some newer ones) simply have NO ruggedness spec. Others are said to be "capable of" withstanding load mismatches. Still others are guaranteed to withstand load mismatches of 2:1 VSWR to∞:1VSWR at rated output power. A few truly rugged transistors are guaranteed to withstand 30:1 VSWR at all phase angles (for all practical purposes 30:1 VSWR is the same as∞:1 VSWR) with both over voltage and over drive. Once again it is up to the user to match his circuit requirements against device specifications.

Then as if the whole subject of ruggedness is not sufficiently confusing, the semiconductor manufacturer slips in the ultimate "muddy the water" condition in stating what constitutes passing the ruggedness test. The words generally say that after the ruggedness test the D.U.T. "shall have no degradation in output power." A better phrase would be "no measurable change in output power." *But even this is not the* best. *Unfortunately the D.U.T. can be "damaged" by the* ruggedness test and still have "no degradation in output power." Today's RF power transistors consist of up to 1K or more small transistors connected in parallel. Emitter resistors are placed in series with groups of these transistors in order to better control power sharing throughout the transistor die. It is well known by semiconductor manufacturers that a high percentage of an RF power transistor die (say up to 25-30%) can be destroyed with the transistor still able to deliver rated power at rated gain, at least for some period of time. If a ruggedness test destroys a high percentage of cells in a transistor, then it is likely that a 2nd ruggedness test (by the manufacturer or by the user while in his circuit) would result in additional damage leading to premature device failure.

A more scientific measurement of "passing" or "failing" a ruggedness test is called Δ Vre - the change in emitter resistance before and after the ruggedness test. Vre is determined to a large extent by the net value of emitter resistance in the transistor die. Thus if cells are destroyed, emitter resistance will change with a resultant change in Vre. Changes as small as 1% are readily detectable with 5% or less normally considered an acceptable limit. Today's most sophisticated device specifications for RF power transistors use this criteria to determine "success" or "failure" in ruggedness testing.

Data sheets for low power RF transistors show such special characteristics as noise figure (NF), maximum available gain (GUmax) and scattering (S) parameters. "S" parameters are normally taken with the D.U.T. in a standard commercial fixture using a network analyzer such as the one shown in Figure 10. Typically these are given as functions of frequency and Ic. The measurements are routine and need no further comment.

NF and GNF likewise use commercial equipment such as the Eaton 4012 gain-noise analyzer or the HP8970A Noise Figure Meter. NF of a transistor will vary with input match and as a result is generally measured in a test fixture with input tuning. Usually data is given with a circuit tuned initially for lowest possible NF and then for a standard 50 ohm input. Measuring NF at 50 ohms Zin is more repeatable albeit not normally as low in value. The 50 ohm measurement is preferred for production testing because it requires no tuning and can be done with automated test equipment and for this reason is frequently the value specified on data sheets. Likewise, gain is normally specified for best NF conditions and for 50 ohms Zin.

RF power transistors are typically characterized by impedance parameters rather than small signal "S" parameters. Both Zin and Zout of a device are determined in a similar way, i.e., *place the D.U.T. in a circuit* and tune both input and output circuit elements to achieve maximum Po at the desired frequency of interest. At maximum output power, D.U.T. impedances will be the conjugate of the input and output network impedances. Thus, terminate the input and output ports of the test circuit, remove the device and measure Z looking from the device, first, toward the input to obtain the conjugate of Zin and, second, toward the output to obtain ZOL which is normally given as the load required to achieve maximum Po.

A network analyzer is used in the actual measurement process to determine the complex reflection coefficient of the circuit using, typically, the edge of the package as a plane of reference. A typical measurement setup is shown in Figure 11. Figure 12 shows the special fixture used to obtain the short circuit reference while Figure 13 illustrates the adapter which allows the circuit impedance to be measured from the edge of the package.

The entire impedance measuring process is somewhat laborious and time consuming since it must be repeated for each frequency of interest. Note that the frequency range permitted for characterization is that over which the circuit will tune. For other frequencies, additional test circuits must be designed and constructed, which explains why it is sometimes difficult to get a

semiconductor manufacturer to supply impedance data for special conditions of operation such as different frequencies, different power levels or different operating voltages.

TRADEOFFS IN SPECIFICATIONS

Gain and ruggedness are the most obvious device parameters for compromise in RF power specifications. Devices with high gain - at least high with respect to their figure of merit (emitter periphery/base area) - tend to be fragile, i.e., not rugged. By using higher resistivity material, material with a thicker epitaxial layer and/or increased values of emitter resistance, ruggedness can be enhanced at the expense of gain. Likewise to get higher gain, the user may be asked to accept lower collector/base breakdown voltages (BVCBO orBVCES and BVCEO) in order to reduce collector resistivity and thereby increase gain.

Transistors specified for operation at a high frequency can be used at a lower frequency to obtain increased gain but almost always such devices at the lower frequency of operation will be fragile. Again for RF power transistors, the user should be wary of unnecessarily specifying tight limits on hFE particularly when functional gain is a test parameter. Also tight leakage current specifications lead to high costs as a result of yield losses and, except where essential such as low power and power devices with bias, should be candidates as tradeoffs for better prices.

SUMMARY

Understanding data sheet specifications and what they mean can be a major asset to the circuit designer as he goes about selecting and using an RF transistor for his specific application. This paper has emphasized some unique data sheet parameters of RF transistors and has explained what these mean from the semiconductor manufacturer's point-of-view. It is hoped this effort will help the circuit engineer make his selection and use of transistors more efficient and effective.

The RF transistor is an unusually complex semiconductor device and difficult to fully characterize. Not all information about RF transistor characteristics has been explained in this paper. Nor can all be covered in a data sheet. The circuit design engineer should contact the device manufacturer for more detailed information whenever it is appropriate. Most if not all current manufacturers of RF transistors have extensive applications support for the express purpose of assisting the circuit designer whenever and wherever assistance is needed.

FIGURES

1. A PAGE FROM MRF646 DATA SHEET (2ND PAGE)
2. GRAPH OF BV VS DOPING LEVEL AND JUNCTION DEPTH
3. BETA VS FREQUENCY CURVE
4. CAPACITANCE VS REVERSE BIAS VOLTAGE CURVE
5. A PAGE FROM MRF646 DATA SHEET (FRONT PAGE)
6. PHOTO OF INFRA RED MICROSCOPE SETUP
7. X-RAY PHOTO OF DIE BONDED TO BEO
8. PHOTO OF RF TEST CIRCUIT (MRF 646)
9. PHOTO OF FINAL TEST STATION
10. PHOTO OF NETWORK ANALYZER
11. PHOTO OF IMPEDANCE MEASUREMENT SETUP
12. PHOTO OF SPECIAL REFERENCE FIXTURE
13. PHOTO OF SPECIAL IMPEDANCE ADAPTER

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector Emitter Breakdown Voltage (I_C = 20 mAdc, I_B = 0)	BV_{CEO}	18	-	-	Vdc
Collector Emitter Breakdown Voltage (I_C = 30 mAdc, V_{BE} = 0)	BV_{CES}	36	-	-	Vdc
Emitter Base Breakdown Voltage (I_E = 5.0 mAdc, I_C = 0)	BV_{EBO}	4.0	-	-	Vdc
Collector Cutoff Current (V_{CE} = 15 Vdc, V_{BE} = 0, T_C = 25°C)	I_{CES}	-	-	5.0	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 0.4 Adc, V_{CE} = 5.0 Vdc)	h_{FE}	40	70	100	
DYNAMIC CHARACTERISTICS					
Output Capacitance (V_{CB} = 12.5 Vdc, I_E = 0, f = 1.0 MHz)	C_{ob}		90	125	pF
FUNCTIONAL TESTS					
Common Emitter Amplifier Power Gain (V_{CC} = 12.5 Vdc, P_{out} = 45 W, I_C(Max) = 5.8 Adc, f = 470 MHz)	G_{pe}	4.8	5.4	-	dB
Input Power (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	P_{in}	-	1.3	1.5	Watts
Collector Efficiency (V_{CC} = 12.5 Vdc, P_{out} = 45 W, I_C (Max) = 5.8 Adc, f = 470 MHz)	η	55	60		%
Load Mismatch Stress (V_{CC} = 15 Vdc, P_{in} = Note 1, f = 470 MHz, VSWR = 20:1, All Phase Angles)	ψ *	No Degradation in Output Power			
Series Equivalent Input Impedance (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	Z_{in}		1.6 + j4.0		Ohms
Series Equivalent Output Impedance (V_{CC} = 12.5 Vdc, P_{out} = 45 W, f = 470 MHz)	Z_{OL} **		1.3 + j2.8		Ohms

Notes

1. P_{in} = 150% of Drive Requirement for 45 W output at 12.5 V.

* ψ = Mismatch stress factor (the maximum condition established to verify the device resistance to load mismatch failure). The mismatch stress test is accomplished in the standard test fixture (Figure 11) terminated in a 20:1 minimum load mismatch at all phase angles.

** Z_{OL} Conjugate of the load impedance into which the device output operates at a given output power, v, and frequency.

FIGURE 1–TYPICAL DC AND FUNCTIONAL SPECIFICATIONS

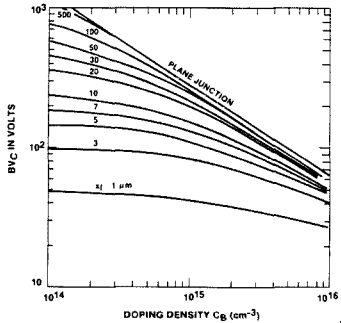

FIGURE 2–THE EFFECT OF CURVATURE AND RESISTIVITY ON BREAKDOWN VOLTAGE

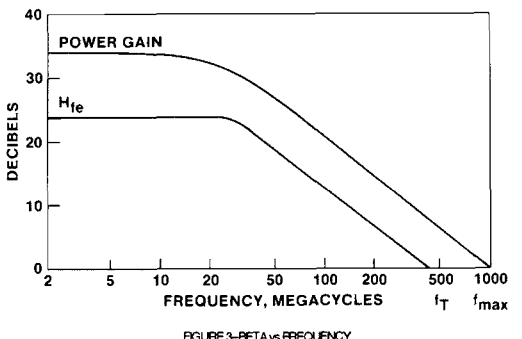

FIGURE 3–BETA vs FREQUENCY

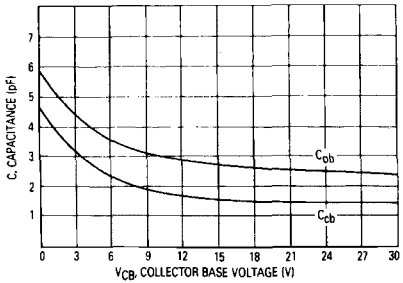

FIGURE 4–JUNCTION CAPACITANCE vs VOLTAGE

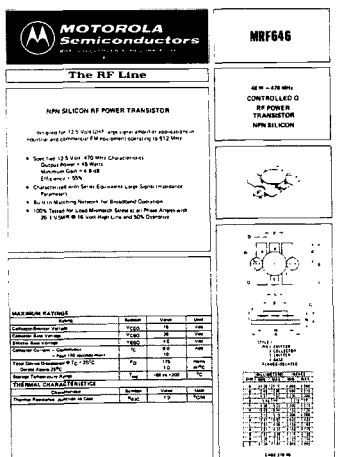

FIGURE 5–TYPICAL MAXIMUM RATINGS OF AN RF POWER TRANSISTOR

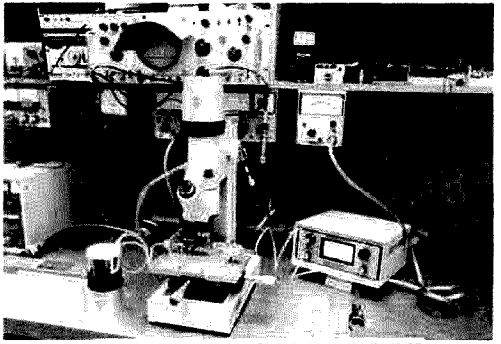

FIGURE 6–EQUIPMENT USED TO MEASURE DIE TEMPERATURE

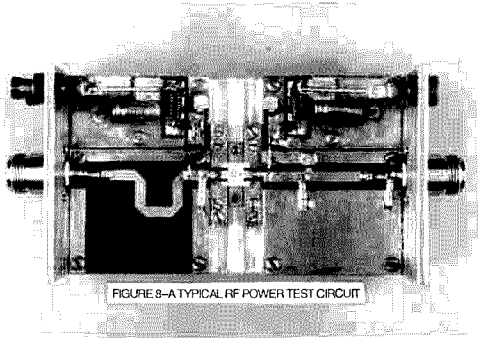

FIGURE 8–A TYPICAL RF POWER TEST CIRCUIT

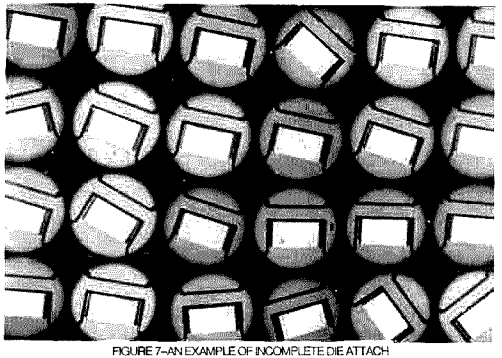

FIGURE 7–AN EXAMPLE OF INCOMPLETE DIE ATTACH

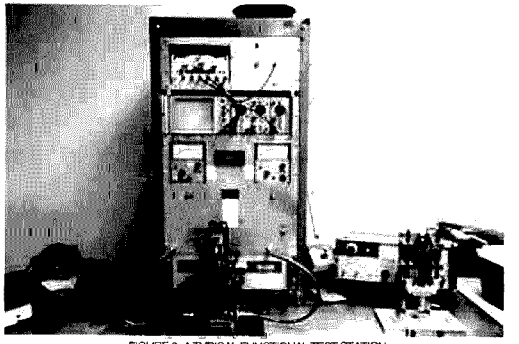

FIGURE 9–A TYPICAL FUNCTIONAL TEST STATION

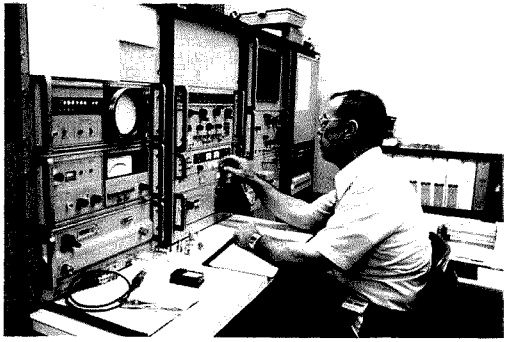

FIGURE 10–THE HP AUTOMATIC NETWORK ANALYZER

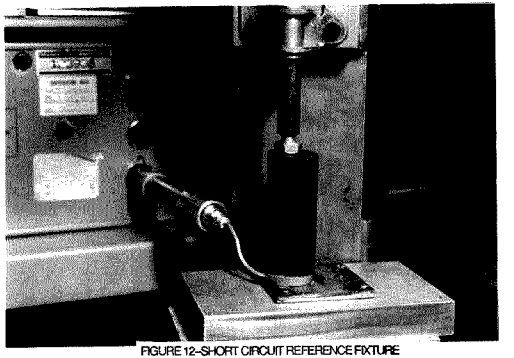

FIGURE 12–SHORT CIRCUIT REFERENCE FIXTURE

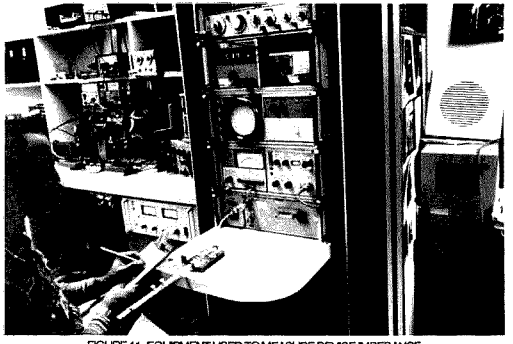

FIGURE 11–EQUIPMENT USED TO MEASURE DEVICE IMPEDANCE

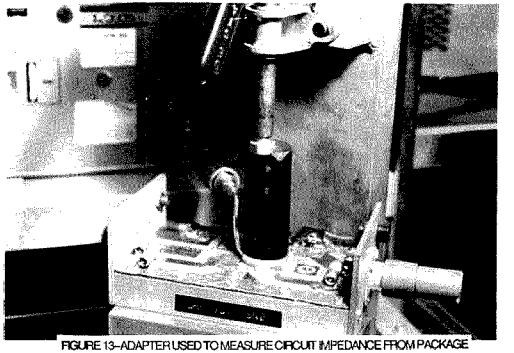

FIGURE 13–ADAPTER USED TO MEASURE CIRCUIT IMPEDANCE FROM PACKAGE

PIN Diode Attenuators and Vector Modulators at Intermediate Frequencies

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The PIN Diode

A PIN diode differs from an ordinary detector or switching diode in that it has an extra layer of undoped or intrinsic semiconductor sandwiched between the P and N doped layers normally found. When the device is reverse or zero biased this I layer is devoid of charge carriers and the diode has a very high AC resistance. With forward bias, carriers are injected into the I layer, the diode conducts and the AC resistance drops.

The key difference between the PIN diode and the ordinary PN diode is that the minority carriers in the I layer have a significant lifetime, and when this lifetime exceeds the period of an RF signal the normal rectification effects begin to be suppressed because the charges transferred in an RF cycle are less than the charge stored in the device.

When a PIN diode is used for switching a signal the forward bias current in the "on" state need not be as high as the peak RF current and the reverse voltage in the "off" state need not be as high as the peak RF voltage. This is a distinct advantage over the PN diode with no carrier storage but it is the behaviour of the PIN diode at intermediate bias states that makes it especially useful.

For small signals at RF frequencies the PIN diode appears essentially as a pure resistor. The exact resistance depends on the device construction but it is roughly inversely proportional to the bias current. Typically, a bias range of 1 μA to 10 mA might give RF resistances of 10K to 1 Ohms.

The quality of this resistance, ie., its linearity and lack of distortion products, can be very good indeed if the diode is used under the right conditions [1]. In practical terms this usually means ensuring that the minority carrier lifetime is at least 10 times the signal period and keeping to power levels of less than 0 dBm.

PIN diodes are available from several manufacturers and in a variety of packages, eg. for waveguide or stripline mounting, but for general purposes the most useful is the familiar in-line wire lead glass package. Figure 1 shows the resistance characteristics of varous Hewlett Packard diodes [2]. Note that the 3080 and 3081 types show less linear control curves. They are, though, particularly useful devices as they have long carrier lifetimes, typically 1.3 μs and 2 μs respectively.

Matched Variable Attenuators

A simple attenuator can be made with a single series or shunt variable impedance element. This, however, is only a matched device at zero attenuation and is not necessarily suitable for the majority of applications. At microwave frequencies it is common to convert unmatched

circuits to matched by the use of quadrature hybrid couplers (Figure 2a), which are readily printable in stripline.

At lower frequencies hybrids are costly components and other matching techniques can be used. The bridged-tee, Figure 2b, and the pi, Figure 2c, attenuators are well known circuits capable of giving variable, matched attenuation over a wide bandwidth if the elements are controlled properly. The bridged-tee requires one less active element but the pi configuration is normally preferred for its higher maximum attenuation with typical components.

Practical Pi Attenuator Design

The series and parallel resistances, Rs and Rp, in the pi attenuator must be controlled simultaneously to ensure a good match as the circuit gain, G, is varied. The required resistances are given by

$$Rp = Z\left[\frac{1+G}{1-G}\right] \qquad Rs = \frac{Z}{2}\left(\frac{1}{G} - G\right)$$

and these equations can be used, together with published device data, to calculate the PIN diode bias currents required at various attenuation settings. Because of the nature of the diode characteristics, this procedure is bound to result in control curves that are extremely difficult to realise in practice. It also sheds little light on the performance deterioration to be expected when the curves are not followed exactly.

At this point, many workers might turn to an extensive computer simulation; this author, however, believes that this is a case where better and quicker results can be obtained from a simple set of measurements.

Figure 3 shows the circuit of a PIN diode pi attenuator in which the series and parallel bias currents, Is and Ip, can be varied independently. If this is connected to a network analyser capable of measuring return loss, $|S_{11}|$, and transmission, $|S_{21}|$, curves of constant return loss and attenuation can easily be plotted. A representative set is shown in Figure 4.

For a given specification on return loss, there is a certain operating area into which the pattern of bias currents must be fitted. The easiset control pattern appears as a straight line on the plot; this can be generated from a single supply with one control line as shown in Figure 5a.

In the case illustrated, though, 20 dB return loss has been chosen as the target and inspection shows that, within this restriction, a straight line control locus can only give a limited attenuation range. It is clear, though, that a locus of two straight lines, as drawn, will cover the full range. Two circuits for generating such a locus are given in Figure 5b and 5c. Both give the same pattern of bias currents but the control voltage vs. attenuation responses are different; one is better suited to percentage gain control, the other to dB attenuation systems.

The calculation of component values for these driver circuits is straightforward and will not be detailed here. For the case in question, the attenuator was to be driven from a D to A converter and it was desired to keep the fractional gain change per LSB as constant as possible over the whole attenuation range.

Figure 6 shows the final circuitused; a batch of eight of these were construted for signal levelling purposes in a phased arrary system.

Figure 7 shows typical performance at 70 MHz. The control characteristic is reasonably linear; certainly the slope variations are small enough for 8 bit digital control to give consistently small step sizes of 0.5% or less. In this application the attenuator was to be used in a closed loop operation so absolute linearity or accuracy of the control was not a requirement; if this had not been the case, some further software linearisation could have been applied.

At low attenuations the input match worsens slightly. This is partly due to compromises made in the bias driver design and partly to stray reactances incurred by the layout and the connecting sockets.

The foregoing example shows how a wideband signal attenuator can be made with a minimum of components. Only one control line is needed and the driver circuit to achieve both a good match and reasonably linear control simultaneously is simple in the extreme.

Vector Modulators

In many applications, phase as well as amplitude control of a signal path is required. This might occur, for instance, in certain modulation systems, phased array processing or adaptive cancellation systems.

Standard phase shifter circuits employ switched line lengths, switched loaded lines etc., Figure 8. Variable reactance devices, such as varactors, can also be used but are limited to only small phase shifts. Switched systems can be cascaded to give phase shifters capable of covering the full 360 degrees in given step sizes. A disadvantage is that the phase settings are quantised and fine resolution demands many stages, which increases the insertion loss and potential inaccuracies. It should be noted that these systems are strictly delay inserters rather than pure phase shifters and wideband operation is not generally possible. Nevertheless, the use of cascaded phase shifters in conjunction with an attenuator does give full four quadrant control of the transmission characteristic. The controls are polar, ie., r and θ, or separate gain and phase adjustments.

In many cases it is more appropriate to combine the gain and phase control mechanisms into a single complex attenuator, or vector modulator. The basic scheme is shown in Figure 9. Full control of the transmission vector is possible but the controls in this case are cartesian, ie., x and y, or I and Q. If all four quadrants are to be covered bi-phase attenuators are required; these have a gain range of -1 to 1 rather than just 0 to 1. There is a 3 dB minimum theoretical loss through such a modulator; this, however, occurs only at certain phase settings, at others the minimum loss is 6 dB.

Despite this, the vector modulator is useful when fine or continuous adjustment is needed. It compares favourably with, for instance, a 6 or 8 bit phase shifter that may have up to 1 dB loss per bit.

Simple attenuators can be converted to bi-phase by the addition of a phase inverter, Figure 10a, or by offsetting half the signal, Figure 10b. The latter method offers easier control but has an inherent 6 dB loss; in the first arrangement it may be difficult to achieve zero transmission.

A better circuit is the hybrid coupler attenuator, versions of which appear in Figure 11. The input power is split between the two variable terminating resistances and the reflections from these terminations

cancel at the input port and add at the output. The depth of cancellation, and hence the input match, depends on the quality of the hybrid and how well the resistances track each other. Zero transmission, apart from hybrid leakage, occurs when the resistances are 50 Ohms; above or below this value transmission increases, with a phase reversal between the two regimes.

With PIN diodes as the variable elements the transmission vs. bias current response is parabolic rather than linear. Also, because of circuit imperfections and temperature effects, repeatable fine control around the zero transmission point may prove difficult. This type of attenuator is best suited to closed loop systems or those with regular calibration.

Any of these bi-phase attenuators can be used to make a four quadrant vector modulator but the hybrid attenuator, with single line control and low minimum loss, is probably the best, Figure 12. The bandwidth of such a circuit is determined by the quadrature hybrids used. It is interesting to note that the coupling network arrangement for this is exactly that found in the six-port network that is used for signal comparison and measurement [3]. This type of vector modulator has been used successfully at 750 MHz by the Independent Broadcasting Authority in Britain [4]. A version using a microwave printed stripline network has also been investigated at University College London and shown to give useful results over nearly an octave bandwidth.

A new variation is that shown in Figure 13; this is a method of extending a single bi-phase attenuator to give control of the quadrature transmission as well. No extra quadrature hybrids are required but with phase shifts provided by line lengths the bandwidth is limited. In the circuit shown the biasing arrangement is simplified by allowing the currents to flow to ground through the power dividers. Most bought in components of this type allow this but care must be taken to ensure that the currents do not saturate any ferrite devices inside.

This circuit, the Reflective Delay Line modulator, has been tried at UCL using commercial couplers at 70 MHz. The PIN diodes used were all HP 3080 types but were not specifically matched. Full cartesian control of the transmission vector was demonstrated; there were no missing sectors or regions of the coverage and because leakage in the couplers can be compensated by adjusting one or the other bias control the zero transmission point can always be accessed. The input return loss varied slightly with control settings but was about 20 dB over the whole range.

A further possibility would be to replace the quadrature hybrid with a 180 degree one and a quarter wave line; this would give an extremely economical four quadrant vector modulator.

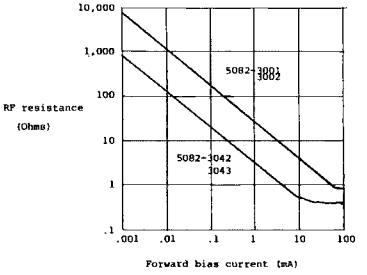
References

[1] "Rectification effects in PIN attenuators", Hewlett Packard Application Note 957-3.

[2] "Diode and Transistor Designer's Catalog", Hewlett Packard Data Book.

[3] A. L. Cullen, "The 6-port and the microprocessor in microwave measurements", Proc. European Microwave Conference 1980, pp74-82.

[4] H. J. O'Neill and B. V. W. Isaacs, "An adaptive cross-polar cancellation system for satellite communications employing dual polarisation frequency re-use", IEE Radio Spectrum Contraverbosity Techniques Conference, 1980, pp 137-141.



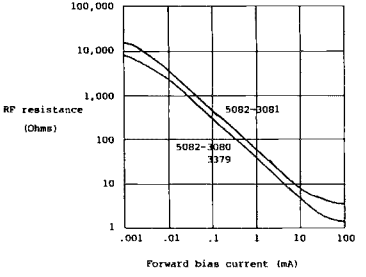


Figure 1: PIN diode RF resistances vs. current [2]

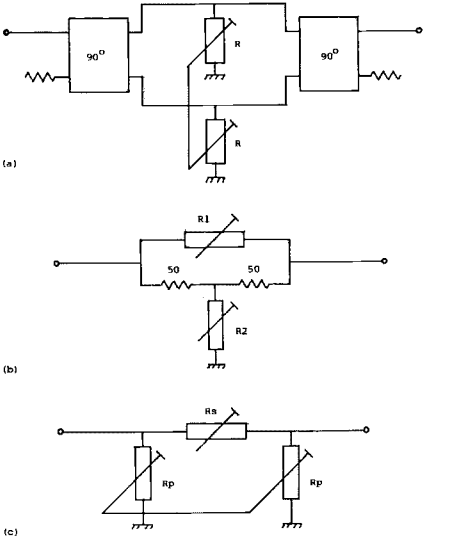


Figure 2: Attenuator configurations

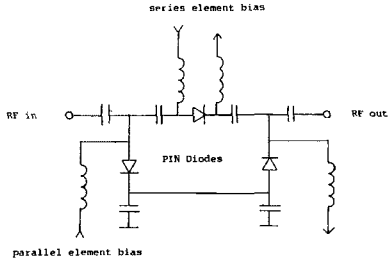


Figure 3: Pi Attenuator test circuit

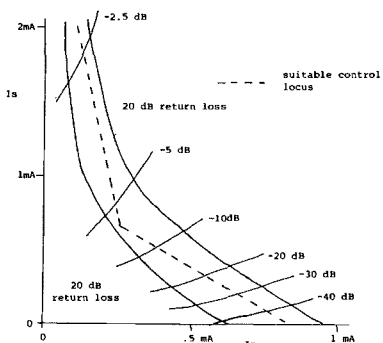


Figure 4: Lines of constant return loss and attenuation

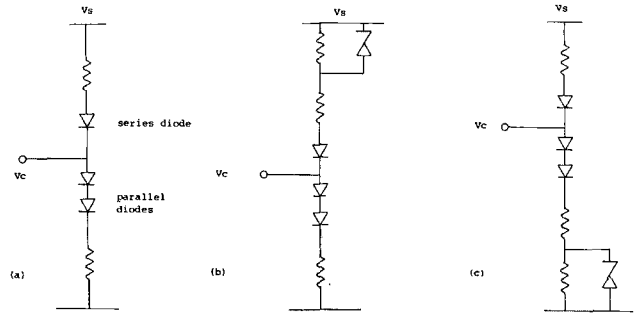


Figure 5: Bias driver circuits

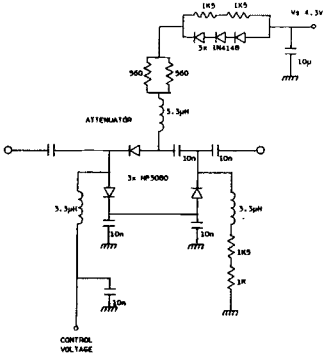


Figure 6: Final pi attenuator circuit

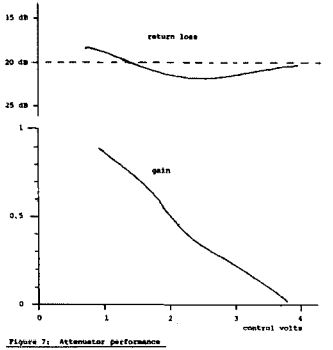


Figure 7: Attenuator performance

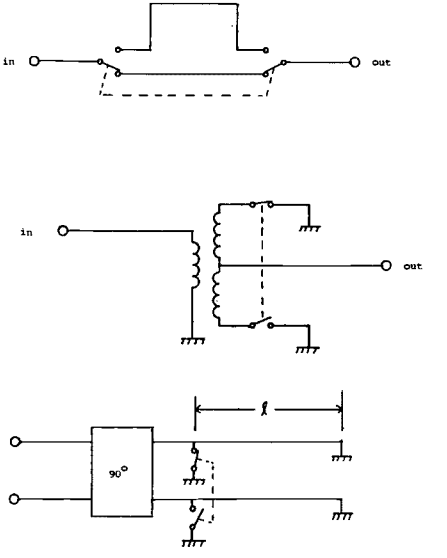


Figure 8: Phase shifter circuits

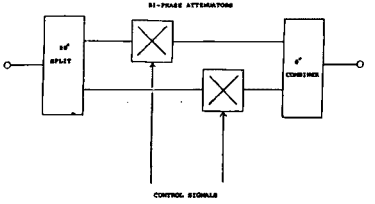


Figure 9: Vector modulator

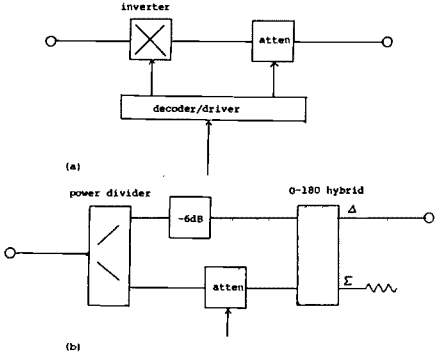


Figure 10: Bi-phase attenuators

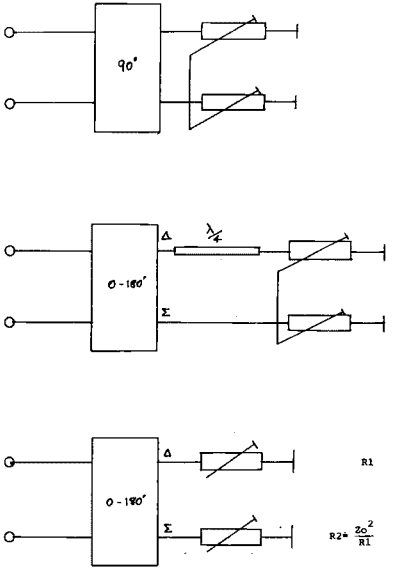


Figure 11: Hybrid coupler attenuators

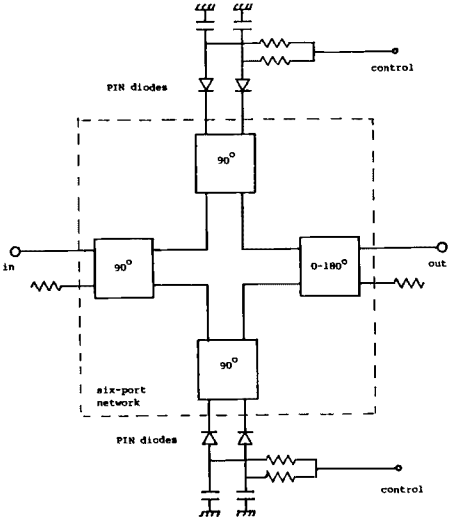


Figure 12: "Six-port" Vector Modulator

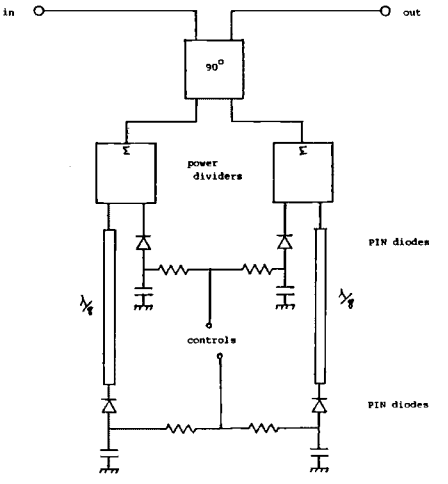


Figure 13: Reflective Delay Line Vector Modulator

High-Voltage HF/VHF Power Static Induction Transistor Amplifiers

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GTE Laboratories Incorporated
40 Sylvan Road
Waltham, MA 02254

The operation and performance of power static induction transistors (SITs) in HF/VHF amplifiers will be discussed in this presentation.

Unprecedented saturated CW output power levels of greater than 200 W at 225 MHz, with 6-dB power gain and 70% drain efficiency, have been demonstrated by single-ended transistors connected in the common-gate configuration. Small-signal measurements on these power SITs indicate a nearly flat 10-dB gain response from 100 MHz to 3 GHz, and a unity power gain frequency in X-band.[1,2]

Static induction transistors, which are operated in a common-source configuration, however, can provide very high gain at frequencies in the HF/VHF and lower UHF frequency bands. To accomplish this, the parasitic drain-to-gate capacitance must be neutralized.

The broadband neutralization schema to be presented is similar to the cross neutralization scheme successfully used for push-pull triode vacuum tube amplifiers (Figure 1). In this design, the parasitic feedback capacitance, C_{PG} (capacitance plate to grid), of each active device is neutralized by adding two neutralization capacitors, externally, which are approximately equal in value to the individual parasitic feedback capacitance values. The addition of these neutralization capacitors to the circuit results in a capacitive bridge, as illustrated in Figure 1. Proper selection of the neutralization capacitors balances the bridge, thereby "nulling out" any potential feedback signals between the output and input of the balanced device. The analogous solid state SIT amplifier is shown in Figure 2.

The computed small-signal gain response and stability factor of this cross-neutralized SIT amplifier, shown in Figure 3, demonstrates the broadband performance potential of this neutralization scheme. Effective broadband neutralization depends upon judicious selection and placement of neutralization capacitors *within the transistor package* and attention to the bond wire inductance associated with connecting the neutralization capacitors to the SIT chips. The neutralization capacitors are implemented as discrete, high Q, low loss capacitors mounted inside the power transistor package in close proximity to the active SIT chips. Very short bond wires are used to connect them, thus *eliminating completely* the potential for resonance conditions. As shown in Figure 3, the calculated gain is approximately 14 dB across the entire 1- to 200-MHz band with a stability factor of >14. Experimental cross-neutralized SITs were fabricated in our laboratory using two, six-cell, 7-μm pitch SGSITs connected in a single balanced transistor package along with a pair of 27-pF chip capacitors mounted inside the package to provide neutralization. The amplifier was designed and fabricated using coaxial 4:1 transformers and baluns wound on high permittivity ferrite toroids. Initial power tests were performed at 100 MHz, where the amplifier exhibited 50 W CW output power with 12.2-dB power gain, as shown in Figure 4. This amplifier performance reflects the power performance in an "as-fabricated" state, without tuning to optimize the performance. The device contains enough active area (W_g = 24 cm) to deliver about 200 W of output power; however, the package which was used is only capable of dissipating approximately 100 W of average power. To establish the CW potential of this amplifier, pulsed operation at a 10% duty was examined. Figure 5 illustrates the peak power capability of this device. A peak output power level of 120 W was observed with 13-dB gain and 40% average efficiency. With a proper package and design refinements, output power levels of nearly 200 W across the band should be possible with this design.

Acknowledgment

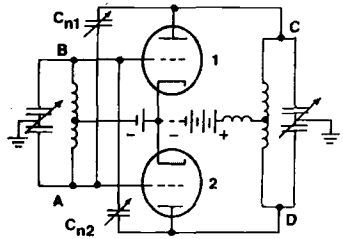
The authors gratefully acknowledge Mehdy Abdollahian, Anthony Varallo, and Marguerite Delaney for their talented work in device packaging, amplifier fabrication, and characterization; Emel Bulat, Maureen Sullivan, Charles Herrick, Steve Rose, and Theresa Rubico for device fabrication; and Drs. Paul Haugsjaa, Harry Lockwood, and Les Riseberg for their continuous support throughout this work. In addition, we thank Frank Stites of GTE Government Systems for his valuable comments and suggestions.

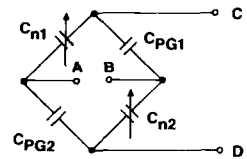
References

1. R. J. Regan and S. J. Butler, "High Voltage UHF Power Static Induction Transistors," Proceedings of RF Technology Expo '85, Anaheim, CA, January 1985, pp. 81–84.

2. R. J. Regan, I. Bencuya, S. Butler, F. Stites, and W. Harrison, "New UHF Power Transistor Operates at High Voltage," *Microwaves and RF 24 63*, (April 1985).

PUSH-PULL
CROSS NEUTRALIZED AMPLIFIER





EQUIVALENT BRIDGE CIRCUIT

GTE Laboratories

Figure 1.

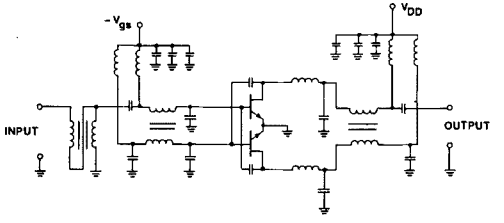


Figure 2. Cross-Neutralized Common-Source Push-Pull Static Induction Transistor Amplifier Design

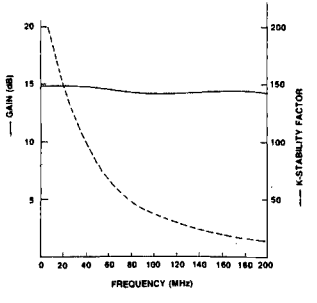


Figure 3. Computed Small-Signal Gain and Stability Factor for Cross-Neutralized Push-Pull SIT Amplifier Shown in Figure 2

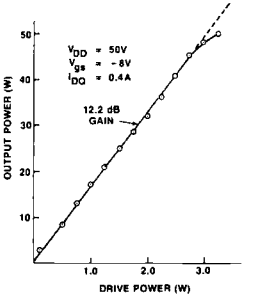


Figure 4. 100-MHz cw Power Performance for the Cross-Neutralized Push-Pull Common-Source SIT Amplifier

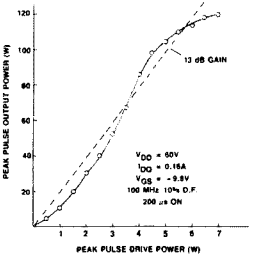


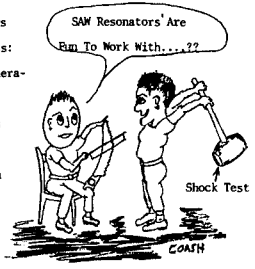
Figure 5. 100-MHz Pulsed Power (10% Duty Cycle) Performance of Cross-Neutralized Push-Pull Common-Source SIT Amplifier

Title: AN EVOLUTION INTO SAW RESONATORS (Low Power Security -- FCC Part 15)

by
Ronald J. Coash -- Notifier/EMHART, 6050 N. 56 St.
EMHART Electrical/Electronic Group Lincoln, NE 68507

SUMMARY

Surface Accoustic Wave Resonators are being used in applications such as: CATV, satellite subsystems, signal generators, security systems,garage door openers, etc. At Notifier, the SAWRs are being used in low power security systems. Few books have been written on SAWRs, so the best information to date appears in technical magazines and papers.



Fundamential frequencys of SAWR oscillator circuits range from 150 MHz to beyond 1,500 MHz. SAWRs exhibit characteristics of the historical bulk crystal devices, yet belong to a much different subclass of frequency stabilizers. The selection of a SAWR is more diversified than its lower frequency bulk crystal class of frequency stabilizers. Selection and evaluation are key words and are the main issues of this paper. The last page of this paper lists other sources of information on the subject of SAWR technology.

INTRODUCTION

The factors involved in the use of SAWRS in short range wireless data communications are paradoxical with cost and dependability being the most important issues. Traditionally, low power (about 6,000 uV/m at 3 meters) security alarm transmitters have been limited to LC and bulk crystal devices, but some manufactures are now using Surface Accoustic Wave oscillators as the frequency stabilizing element. The range of these devices is about 200-350 feet (Null Free not Free Space Range).

1.1 Current FCC requirements have made it increasingly difficult to design and manufacture cost effective "miniture" RF transmitting and receiving devices. In several cases manufacturers are operating (or were at one time) under special wavers, thus prompting some of us to use slightly more expensive SAWR technology. Recently, costs have been reduced somewhat, thus making SAWRs more feasable with regard to EM/SAWRs being used in cost conscious designs. Many computing devices and portable radios radiate more interference (RFI/EMI) than is allowed for life safety devices under FCC Part 15. To further complicate the situation other regulations (UL 1023) require a one year battery life from a 9 volt "transistor radio battery". Formerly, Notifier manufactured bulk type crystal controlled frequency multiplier VHF transmitters that consummed more power per period of time than the present units do. In this particular case the transmitters transmit a supervisory signal once a minute for 24 hours/day. Note also that the transmitters are in the UHF range instead of previous VHF range.

1.2 Paradox/Contradictions = Strict Design Parameters (for cost effectiveness) Transmitter specifications: cigarette pack size, at least 300 ft. range, low battery detect alarm, 256 system codes, 32 transmitter codes, 4 transmitter function codes, error code, 15 uA. idle current, one year battery life, one minute short supervisory transmissions (every minute of the day), 8 special codes, rugged, .25% bandwidth, special scheduled transmissions, no external antenna, and do all this for the nominal sum of $15 cost (factory). Then meet FCC and UL requirements for life safety devices that have greater restrictions than do other devices not involved in life safety issues. BY THE TIME THE DIGITAL DESIGN IS COSTED THERE IS LITTLE MONEY LEFT FOR THE R.F. SECTION.

2.0 USE OF SAWR TECHNOLOGY VERSES LC CRYSTAL, etc.

2.1 What is a Surface Accoustic Wave Resonator? A SAWR is a frequency stabilizing devise which is used in much the same way as are typical bulk crystal elements, but does so at higher fundamental frequencies (150-1,500 MHz). However, the variations in the use of SAWRs used here are more extensive and the specifications vary considerably. There are various articles and papers that have been written on this subject and the purpose of this paper is to cover the somewhat obscure aspects experienced in working with SAWRs.

Since the SAWR operates on a surface phenomenum that does not appear to affect the bulk of the piezo-electric substrate, it was decided to try a truly fine idea as shown in Figure 2. The Modulator (Bulk) changes the length of the substrate and thus mudulating the spacing of the surface waves which determine the SAWR's frequency.

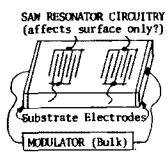


Figure 2

2.2 ADVANTAGES	DISADVANTAGES
Small size	Manufacturing tolerances
Up to +20 dBm in DIP (14 pin)	Aging > Bulk Crystal (10ppm/.1ppm)
Phase Selection (0 or 180 deg.)	Variation in Types (Selection)
Frequency Range 150-1500 MHz	Limited to above 150 MHz
Tolerance better than LC	Yeild % (Mfg.)
Rugged (Comp to VHF Bulk Xtal)	Still has harmonics
Power Disipation > Bulk Xtal	Initial tooling $4,000-6,000
FSK/FM (Wide Deviation)	Limited Number of Hybrid Low Cost Vendors
Simplifies Design	
Frequency Stability	
Lower total current than Xtal Osc.@ UHF	
Few Spurious Oscillations	
Fewer adjustments (especially at UHF)	
Reasonably Priced in Hybrid Osc. form	

(The above list is a partial one, but points out some obsecure facts See Page 9)

RESULTS OF EVOLUTION

3.0 The change from both LC oscillators and bulk crystal oscillators is a somewhat intermediate one with respect to overall characteristics. The SAWR manufactures have improved the devices over the past 3 years with respect to cost, tolerences, and yeilds. A lot of new ideas developed in piezo-electric applications-pressure sensors, active filters, etc.

3.1 Developement of the FSK/FM hybrid oscillator (transmitter) occured with requirements in reduced size and adjustment expense. Below is one of the early circuits used for evaluation of FSK/FM SAW Resonator Oscillators.

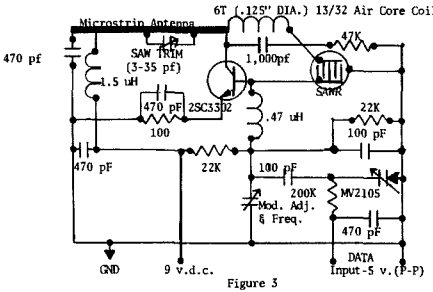
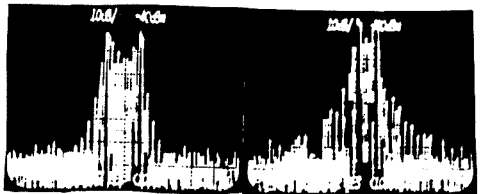


Figure 3

The circuit above was later modified so that only one adjustment is necessary to set the main frequency and the frequency deviation. In adjusting the SAW TRIM capacitor, one tends to center the main frequency too much to allow for a frequency deviation range of 90-100 kHz. The component Q and design parameters of the phasing inductors connected to the SAWR are somewhat different than expe ted. The use of high Q coils resulted in the oscillator running intermittently in a "free run mode" when being modulated. Reduction of coil wire size and coil size increased the pullability of the oscillator but the losses of the circuit were greater, thus requiring a different transistor bias level. The circuit components were placed in the same physical orientation as in the schematic diagram in Figure 3.

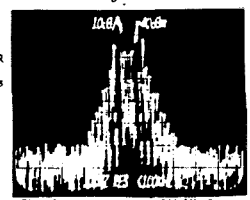
A rather basic oscillator test procedure was used: voltage variations, power supply switching, frequency and deviation amplitude measurements, etc. The most profound test was performed by placing the hand in contact with all of the oscillator components and upon removal watching the results as the preceeding tests were performed. Then the circuit was tested for maximum frequency deviation while maintaining stability, as shown in Figure 4. The object of the hand interference test is to test for oscillator recovery with and without the circuit pulled off frequency by the modulator. Variations in power supply voltage do not display the same results.

CAUTION -- The circuit involved can eventually deteriorate the SAWR and its occurance is so gradual that it is not noticed at first. Changing the bias resistors on the base circuit is necessary for better long range performance. Damage to the SAWR occured at about +18 -- 20 dBm. At about +12 dBm the centerline frequency of the SAWR used would change perhaps indicating some internal heating of the SAWR itself. The goal to obtain signal output levels of 12,333 uV/m at 3 meters with a single stage SAWR was not obtained. Therefore, a hybrid oscillator with a buffer booster stage was added to the oscillator to obtain more output and save space. Note also that marketing requirements did not allow for a separate antenna to aid in design and range requirements in the initial descrete SAWR design. Essentially the goal became almost impossible to obtain thus making it necessary to maximize all aspects of the design. Again the parameters obtained are intermediate with respect to the advantages between LC and bulk crystal oscillators. The term intermediate is used here primarily due to the manufacturing frequency tolerance of low cost SAWR devices.



Discrete SAWR Osc. with 180 kHz Dev.
Figure 4

Hybrid Oscillator with 100 kHz Dev.
Figure 5



IPR Signal Generator @ 100 kHz Dev.
Figure 6

SPECTRUM ANALYSIS -- MODULATION

It should be noted that the SAWR manufactures reccmend deviation rates of about 100 ppm and not as is shown in these figures. A typical SAWR oscillator specification sheet is on page 9. (Courtesy of RF Monolithics, Dallas, Texas)

3.2 The circuit in Figure 3 was modulated with a logic (data) signal voltage of 4.6 volts = logic high and about 0.15 volts = logic low. The modulation deviation curve is shown in Figure 7. The same device could be used as a VCO local oscillator in a receiver. In this case the VCO d.c. supply did not stay stable enough over a period of time, thus a fixed SAWR oscillator is used. The particular I C used exhibited voltage reference drift that was significant.

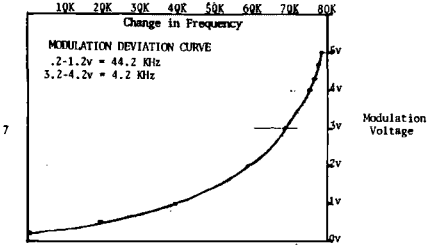
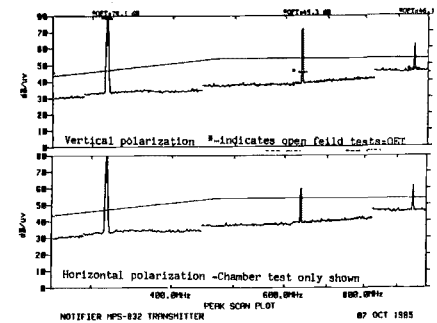


Figure 7

3.3 The harmonic level mentioned in Section 2.2 is somewhat varied and depends upon the output circuits. An interesting observation occured during near field measurements in a chamber @ 1 meter and open field measurements @ 3 meters, as shown in Figure 8. The asteriks designate the open field results. Also note the differences in horizontal and vertical polarization tests.



(Courtesy of RF Monolithics)
Dallas, Texas

FIGURE 2 Typical SAW hybrid oscillator specifications

Operating Frequency:	
Fundamental output range	150 MHz to 1500 MHz
With integral multiplier	up to 6000 MHz
Frequency Tolerance:	± 10 ppm at 25° C
Temperature Stability:	Maximum operating frequency shift
Uncompensated	Less than 100 ppm for 100°C change
With integral compensation	Less than 10 ppm for 100°C change
SSB Phase Noise:	500 MHz operating frequency
at 0.1 KHz offset	Less than − 75 dBc/Hz
at 1.0 KHz offset	Less than − 105 dBc/Hz
at 10 KHz offset	Less than − 130 dBc/Hz
Noise floor	Less than − 135 dBc/Hz
Power Output:	− 30 dBm to + 20 dBm
Modulation Options:	
Pulse modulation	40 dB on/off ratio standard at 50 KHz clock rate
FSK modulation	Up to 100 ppm frequency deviation at 50 KHz clock rate
Supply Voltage:	+5 Vdc, +9 Vdc, +12 Vdc ± 10% standard
Packaging:	Dual in line metal package; Surface mount metal package; Custom

Not Freq/EMART at 315ppm at 2KHz Clock (also 10KHz Clock) 318MHz ±Fo

FIGURE 3 Free running phase noise of 567 MHz SAW resonator oscillator

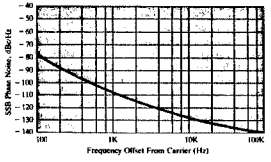
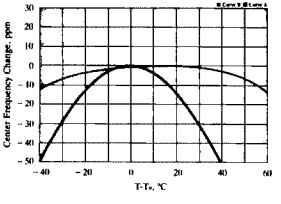


FIGURE 4 SAW Hybrid oscillator temperature performance. Curve A — uncompensated oscillator. Curve B — integrally compensated oscillator



4.0 CONCLUSIONS -- Some not so obvious SAWR characteristics -- SELECTION of SAWR

0 or 180 degrees (RS or RP) -- Depends upon active device used

1,2,3, or 4 Port -- Insertion Loss

Operating frequency note Offset FM Characteristics

Frequency tolerance

Temperature Stability of various types

2,3, or 4 Poles

Tooling Charges for new frequencies

Input and output capacitances

Unloaded Q

Turnover temperature

Bandwidth -- On FSK/FM uses

DC Breakdown Voltage

Series Capacitance -- Resistance -- Inductance

Max Power disipation (if running near limit)

There are other factors involved and awareness of the above is the purpose intended here. As an exercise, try deciding between a 0 degree and 180 degree SAWR and the benefits of each. In building an impedance inverting Pierce oscillator, one would probably use a dual gate FET and a 180 degree SAWR, only to later decide to use a 0 degree device in a hybrid circuit with a buffer stage. The point being that there are many variations in the use of SAWRs and some pre-study and planning is needed to avoid mistakes.

Sources of SAWR technology information: RF Monolithics--Dallas,TX; SAWTEK--Orlando, FL; Andersen Laboratories--Bloomfield, CT; Frequency Control Symposium; RF Design Magazine; Microwaves & RF Magazine.

A TRACKING IMPEDANCE MEASUREMENT SYSTEM for Control of Tunable Networks

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ABSTRACT

Applications for advanced design, tunable, HF impedance matching networks and filters require accurate impedance measurements. This paper describes a Tracking Impedance Measurement System (TIMS) which provides capability for actual in-line impedance measurements. For comparison, a conventional phasing-loading discriminator provides only relative magnitude and phase angle measurements based on a reference impedance. The TIMS operates over a wide power range in the HF band yet generates virtually no noise or spurious signals. Digital outputs are updated rapidly and may be used to calculate impedance, reflection coefficient, and VSWR in real time. These features permit performance of remote impedance measurements. The TIMS also provides selectivity to reduce errors due to interfering signals.

INTRODUCTION

Impedance networks are used for antenna couplers (matching networks) and filters in the high frequency range. Figure 1 shows simplified examples of a typical antenna coupler circuit and a bandpass filter (BPF) circuit. Fixed tuned impedance networks are used for applications in which only one frequency is used such as broadcast transmitters. For applications requiring the use of several frequencies, adjustable or tunable impedance networks are needed. Manually adjustable impedance networks were used for many years and are still used for applications which require infrequent retuning. Applications requiring many frequency changes or rapid retuning use automatically tunable impedance networks.

Automatic tuning of an impedance network requires a control system and a sensing device. The control system may be a closed loop analog servo control system or a digital control system. In either case a sensing device and tuning criteria are needed. In this presentation I will be primarily discussing sensing devices. I will first review the function, application, and limitations of the conventional Phasing-Loading discriminator. I will then present a new concept in sensors for automatic tuning systems called a Tracking Impedance Measurement System (TIMS) which I will call TIMS for short. I will discuss the

function, operation, and application of the TIMS.

The TIMS was invented by Mr. Harvey L. Landt of Collins Defense Communications, Rockwell International Corporation, Cedar Rapids, Iowa. Mr. Landt holds United States Patent No. 4,506,209 issued March 19, 1985 for the TIMS. Full credit and acknowledgement is given to Mr. Landt for this design and for his assistance in the preparation of this paper.

CONVENTIONAL PHASING-LOADING DISCRIMINATOR

Tuning criteria which have been used in the past for manual adjustment of impedance networks are not easily adaptable to automatic tuning control systems. For example, finding minimum current or voltage, maximum current or voltage, or minimum reflected power are criteria that may be used in a manual tuning system, but are not easily adapted to automatic tuning systems. Figure 2 shows typical sensor signals versus tuning element position. In 2(A) a minimum is to be detected and in 2(B) a maximum is to be detected. In either case the sensor signal or error voltage is always of the same polarity and cannot be detected with a zero seeking closed loop servo control system. Figure 2(C), however, shows a sensor signal which passes through zero at the tune point and has opposite polarity on either side of the tune point. This signal can be used with a zero seeking servo control system and the system will be stable at the tune point. The conventional Phasing-Loading Discriminator provides this type of error signal.

FUNCTIONAL DESCRIPTION

The conventional phasing-loading discriminator is placed in series with the RF transmission line at the point tuning information is desired. This is usually at the input of an antenna coupler or filter. It contains two error sensing circuits, one for phasing and the other for loading.

The phasing circuit shown in Figure 3 combines RF voltage and current samples vectorially , rectifies the vector sums, and combines the DC voltages to provide a DC output error signal. This error signal is a function of the phase angle between the transmission line voltage and current. The phasing circuit is adjusted to provide an error signal of zero volts when the phase angle is zero. A positive DC error signal may indicate the phase angle is inductive and a negative DC error signal would then indicate the phase angle is capacitive. In either case the magnitude of the error voltage is a function of the phase angle magnitude, but it is not necessarily proportional.

The loading circuit shown in Figure 4 rectifies the individual voltage and current samples and then combines the DC voltages to produce a DC output error signal. This error signal

is a function of the impedance magnitude. The loading circuit is adjusted to provide an error signal of zero volts when the impedance magnitude is the desired tuned impedance, usually 50 ohms. A positive DC error signal may indicate an impedance magnitude greater than 50 ohms and a negative DC error signal would then indicate an impedance magnitude less than 50 ohms. In either case the magnitude of the error voltage is a function of the ratio of the actual impedance magnitude to 50 ohms, but it is not necessarily proportional.

The combination of the phasing and loading circuit response is shown in Figure 5 using a Z-plane which is a graphical representation with rectangular coordinates plotted as (R, jX). Note there are four basic zones separated by the R axis and the |Z| curve. The phasing and loading discriminators individually provide directional and speed control error information for a zero seeking servo control system for one of the reactive tuning elements. With appropriate logic control and servo gain and stability circuits the reactive elements can be positioned so the impedance at the discriminator location is 50 + j0 ohms.

APPLICATIONS AND LIMITATIONS

The phasing-loading discriminator is used primarily with analog servo control systems. Many automatic tuning antenna couplers have been designed and produced with this type control system in the past 30 years for use on aircraft, land vehicles, transportable shelters, shipboard, and submarines. Also automatic tuning bandpass filters have been designed and produced for many applications including high power filters for shipboard multicouplers. The phasing-loading discriminator has also been used in the last several years with automatic digital tuning control systems for antenna couplers.

Some important limitations of the phasing-loading discriminator are:

1. Not calibrated for impedance measurement
2. Susceptibility to interfering signals
3. Diode noise
4. High RF power level required

Impedance Measurement

The accuracy of the DC output signal voltage from the phasing or loading discriminator is affected by several factors such as RF power level, diode characteristics versus frequency, and sampling circuit characteristics versus frequency. Therefore the phasing and loading error signals cannot be calibrated to enable accurate impedance measurements. Referring again to Figure 5 only relative impedance information is available as described by the four zones on the graph. For example at point A, the impedance magnitude is greater than 50 ohms and the phase angle is inductive. At point B the impedance

magnitude is less than 50 ohms with a capacitive phase angle. Thus only coarse logic decisions can be made to aid the control system to adjust the tuning elements for the tune point.

Susceptibility

The conventional discriminator provides no selectivity for rejection of interfering signals conducted from the antenna through the antenna coupler to the discriminator (back door interference). Interfering signals at a different frequency coupled to the antenna from other nearby transmitting antennas can thus cause the antenna coupler to mistune.

Diode Noise

The rectifier diodes in the conventional discriminator can cause noise to be transferred to the RF transmission line. This is an important consideration for low noise transmitter systems.

Power Level

The voltage and current samples must be lightly coupled to the transmission line to minimize power loss and alteration of the transmission line impedance. Light coupling results in small sample voltages. The RF power level must be high enough so the sample voltages can sufficiently overcome the diode voltage drop and provide the necessary sensitivity for the servo control loop. The required RF power level for the conventional discriminator is usually in the 100 watt to 200 watt range.

TRACKING IMPEDANCE MEASUREMENT SYSTEM

The Tracking Impedance Measurement System or TIMS was developed to overcome the limitations of the conventional phasing-loading discriminator.

FUNCTIONAL DESCRIPTION

The TIMS shown in the block diagram of Figure 6 is an impedance measurement system consisting of a directional coupler, discriminator stage one, discriminator stage two, an A/D converter, and an I/O device.

The directional coupler is placed in series with the transmission line at the point impedance measurements are desired. It provides forward and reflected RF voltage samples to the discriminator stages. From the forward voltage sample, an injection signal is derived which tracks the signal from the signal source but is offset by 10 kHz. The injection signal is then used to convert the forward and reflected voltage samples to 10 kHz signals which are representative of the original voltage samples. The frequency of the converted signals is constant at the offset frequency of 10 kHz, regardless of the operating signal frequency. These constant frequency signals are filtered to provide selectivity and processed with low frequency circuits to derive voltage analogs of the forward

voltage, reflected voltage, and phase angle between them. These three voltage analogs are supplied to the A/D converter. An I/O device such as a microprocessor can then use the digital form of the forward voltage, reflected voltage, and phase angle to calculate the reflection coefficient, impedance, and voltage standing wave ratio (VSWR).

The TIMS overcomes the limitations previously noted for the phasing-loading discriminator.

Impedance Measurement

The TIMS automatically tracks the signal frequency and provides accurate impedance measurements rapidly when the signal frequency is changed.

Susceptibility

The TIMS provides selectivity to reject interfering back door signals.

Noise

The directional coupler contains no noise sources. It provides 30 dB of isolation between the transmission line and possible noise sources in the discriminator stages.

Power Level

The discriminator stages operate with low level signals. With appropriate signal attenuators between the directional coupler and the discriminator stages, the TIMS can provide accurate impedance measurements even with the forward power level as low as 10 milliwatts.

OPERATIONAL DESCRIPTION

Directional Coupler

The directional coupler is a balanced bi-directional assembly which provides an RF forward voltage sample and an RF reflected voltage sample. Approximately 30 dB isolation is provided between the transmission line and the voltage sample output. The directivity is greater than 40 dB. For example if the directional coupler is terminated with a 50 ohm resistive load with a forward power of 100 watts, the reflected voltage sample will erroneously indicate a reflected power of 10 milliwatts or less. The resulting VSWR error is less than 1.02:1.

Discriminator Stage One

The block diagram for discriminator stage one , which is essentially a dual *channel receiver, is shown in Figure* 7. The forward voltage sample is applied via a fixed attenuator to an automatic gain control (AGC) circuit which is part of the forward voltage channel. The AGC circuit controls the signal level of both the sampled forward voltage and the sampled reflected voltage. The AGC circuit in the forward voltage channel includes an electronically variable attenuator and an RF amplifier, the combination of which comprises a variable gain

amplifier. The output of the variable gain amplifier is applied to another RF amplifier and then to an RF detector and bias amplifier which converts the sample forward voltage signal to a variable amplitude DC signal which is used to adjust the variable attenuator. This automatic gain control maintains the voltage level and provides a signal at the output of the variable gain amplifier which is representative of the forward power applied to the directional coupler. The combination of the fixed attenuator, the variable attenuator, and the directional coupler isolation reduce the signal to the appropriate level for the discriminator circuitry. The variable attenuator is automatically adjusted over a 56 dB range for proper operation of the discriminator with variations of the power level at the input to the directional coupler.

One output of the forward voltage channel variable attenuator circuit is an RF sample which is applied to discriminator stage two for generation of the injection signal. The injection signal is applied back to discriminator stage one where it is applied to a power splitter. One output from the power splitter is mixed with the forward voltage signal output from the variable attenuator. The output of the mixer is a 10 kHz signal which is applied to a low pass filter which passes 10 kHz. Signals above 30 kHz are terminated via a high pass filter and a resistor. The output of the low pass filter is applied to a fixed gain amplifier and then to a bandpass filter which passes 10 kHz. The signal is then rectified by a full wave rectifier to obtain the output signal EF which is a DC voltage analog that represents the voltage of the forward power applied to the directional coupler.

The reflected voltage channel also includes an electronically variable attenuator which is controlled by the AGC circuit. The operation of the reflected voltage channel is identical to the forward voltage channel operation with one exception. In the reflected voltage channel a dual gain amplifier is used between the low pass filter and the bandpass filter. When the circuit is initially used and there is a substantial amount of reflected voltage sampled by the directional coupler, then the low gain setting of the dual gain amplifier is utilized. However as the impedance network being tuned approaches the tuned condition, then the reflected sample decreases and to provide an accurate measurement, the high gain setting of the dual amplifier is used which essentially expands the scale of the reflected voltage measuring circuit. The output signal ER is a DC voltage analog that represents the voltage of the reflected power existing at the directional coupler.

The phase angle between the forward voltage and reflected voltage output signals from the respective bandpass filters is

obtained by the phase comparator. Each channel bandpass filter output is applied to a zero cross detector that senses every time the alternating current signal crosses the zero voltage potential. The outputs of the two zero cross detectors are logic signals and are compared by a phase detector which provides a signal whose length in time represents difference in occurence of an output pulse from the two zero cross detectors. The output of the phase detector is filtered and amplified and provided as output signal "theta" which is a DC voltage analog representing the phase angle between the voltage of the forward power and the voltage of the reflected power which exists at the directional coupler.

Discriminator Stage Two

The block diagram for discriminator stage two is shown in Figure 8. The RF sample previously derived by discriminator stage one is applied to discriminator stage two and is used to generate the injection signal. The injection signal is a single sideband signal that tracks the input RF signal that is applied to the directional coupler but is offset from that input signal by 10 kHz.

The RF sample is applied to a variable gain amplifier whose output is varied by the injection signal and then applied to a power splitter. One output of the splitter is applied to a buffer amplifier, an output amplifier and pulse shaper, and a divider which divides the signal by 100 to provide the signal VRF which may be used by a frequency counter circuit to determine the input signal frequency. The second output of the power splitter is applied to a buffer amplifier and then to a signal sideband generator.

The single sideband generator uses a phase difference technique to generate the RF injection signal. The output of the buffer amplifier is applied to a broadband 90 degree RF splitter which provides an in-phase signal and a quadrature signal. The in-phase signal is applied to an in-phase mixer where it is mixed with a signal that is provided by a 10 kHz oscillator via the in-phase terminals of a 90 degree audio splitter and a 10 kHz bandpass filter and driver. The quadrature phase signal from the RF splitter is applied to the quadrature phase mixer where it is mixed with a signal that is provided by the 10 kHz oscillator via the quad-phase terminals of the 90 degree audio splitter and a 10 kHz bandpass filter and driver. The outputs of the in-phase mixer and the quadrature phase mixer are combined and the result is applied to an RF output power amplifier which provides the drive power for the injection signal. The injection signal is applied to an RF detector and bias amplifier to generate the signal to control

the variable gain amplifier. The injection signal is applied to discriminator stage one as previously described.

A forward power sample derived from the RF forward voltage sample output of the directional coupler is applied through an RF amplifier to an RF detector. The detected signal is applied to a threshold comparator whose output digital signal FFP will indicate whether enough power is present at the directional coupler to appropriately operate the TIMS and the equipment which is being tuned.

CONSTRUCTION

The directional coupler is constructed in a metal chassis. Type N coaxial connectors are used for the transmission line connections which must conduct up to 2000 watts PEP. Type TNC coaxial connectors are used for the forward voltage sample and reflected voltage sample outputs to prevent misconnection of the high power input signal to these low power outputs. Coaxial transmission lines, shielded compartments, toroidal coupling coils, and layout techniques are used to minimize stray coupling and enhance accuracy.

Discriminator stage one is built on one printed circuit card using shielded compartments to isolate the various stages of the circuitry and control electromagnetic interference (EMI). The forward voltage and reflected voltage channels are constructed with nearly identical component layouts considering the small variations between their circuits. Special care is taken to keep the two variable attenuators nearly identical with small tolerance components so their output voltages will accurately track with each other for variations in the input power to the directional coupler.

Discriminator stage two is built on a second printed circuit card with similar shielded compartment construction.

APPLICATIONS

The first application of the TIMS was in a shipboard antenna coupler group designed to solve shipboard simultaneous operation (SIMOP) problems. Currently the TIMS is being incorporated into the design of an aircraft antenna coupler group to solve aircraft SIMOP problems. The TIMS could have applications in many advanced antenna coupler or filter developments.

SHIPBOARD APPLICATIONS

The Problem

To describe the shipboard application, I will first discuss the problem which the shipboard antenna coupler group solves. Figure 9(A) illustrates the SIMOP problem that exists when transmitting antennas are closely spaced (collocated) due to

space restrictions on board ship. A separation of only 25 feet is not unusual on a ship and substantial coupling occurs between antennas in portions of the HF range. The various transmitting systems obviously must use different operating frequencies but operation with frequencies as close as 5% of each other is often desired. Two types of coupling are of concern -- power coupling and impedance coupling.

Power Coupling: Let us first consider power coupling. Consider case 1. With system B transmitting at frequency F2, system A is automatically tuning at frequency F1. Some portion of the power radiated by the system B antenna is coupled to the system A antenna. Usually the power coupled to antenna A is 10 dB or more below the power radiated from antenna B but in the worst case it may be only 3 dB below the power radiated from antenna B. A typical antenna coupler exhibits very little selectivity to attenuate F2. The typical phasing-loading discriminator has neither selectivity nor directivity and cannot distinguish transmitter A signals from antenna B signals. The discriminator can only detect impedance magnitude and phase angle based on the voltage and current existing in the transmission line at the discriminator location. But in this case, the voltage and current are the result of the mixing of the voltages and currents for F1 and F2. Therefore erroneous discriminator output signals are detected which cause mistuning of antenna coupler A.

Now let us look at case 2. Consider that while system B was not transmitting, antenna coupler A was tuned and is now transmitting on F1. Now system B is keyed and begins to radiate power at F2. The power coupled to antenna A causes erroneous discriminator outputs as in case 1. If antenna coupler A has its automatic tuning circuits activated, for example by constant surveillance or demand surveillance, it will attempt to retune to satisfy the discriminator output signals. Then when system B is unkeyed again and stops radiating, antenna coupler A will attempt to retune to its original settings for F1.

In typical SIMOP situations a combination of case 1 and case 2 will occur mutually affecting both system A and system B. The resulting disruption of communications in each transmitting channel is evident.

A possible solution to the power coupling problem would appear to be to simply tune each antenna coupler while the others are not transmitting and then de-activate the automatic tuning controls. This method might be feasible when only two antennas are collocated but many installations have several antennas collocated. More importantly, this method does not solve the other coupling problem--impedance coupling.

Impedance Coupling: Referring now to Figure 9(B) note the equivalent circuit representing mutual impedance coupling

between the antennas. To illustrate the problem let us ignore the power coupling. Consider that antenna coupler A is tuned correctly for F1 while antenna coupler B is tuned correctly for F2. Now while system A is transmitting, let system B retune to a new frequency F3. When antenna coupler B is tuned, the back impedance ZB looking from the terminals of antenna B to the output terminals of antenna coupler B is now different than it was when antenna coupler B was tuned for F2. ZB represents the load impedance for the equivalent T network which represents the collocated antenna system. Consequently ZC, the load impedance for antenna coupler A, is now different and antenna coupler A is no longer correctly tuned. The automatic tuning controls for antenna coupler A must be activated so it can retune to the new load impedance, but now the coupled power problem (which we ignored for illustration) may prevent correct tuning.

The combination of coupled power and coupled impedance occur in varying degrees in the HF band depending on type of antenna, separation from collocated antennas, other nearby structures, and the configuration of the antenna coupler impedance matching circuits.

The Solution

Figure 10 illustrates the solution to the shipboard SIMOP problem. A band pass filter is placed between the transmitter and the antenna coupler. The sensing device for automatic tuning is located at the RF input to the BPF instead of at the RF input to the antenna coupler. The F2 signal power coupled to antenna A is now attenuated by the selectivity characteristics of the BPF so the sensing device at the BPF input does not respond to the F2 signal. The selectivity of the BPF also reduces the level of intermodulation distortion (IMD) resulting from mixing of F1 and F2 at the transmitter.

A new problem is created by this configuration. The antenna coupler must be located above deck at the antenna base. On shipboard there is usually insufficient space near the antenna base for the BPF. Thus the BPF is located below deck, probably but not necessarily near the transmitter. A long coaxial transmission line is therefore required between the BPF and the antenna coupler. The length of the coaxial transmission line will be different for each different class ship installation. Tuning of the antenna coupler becomes the problem because the input impedance to the antenna coupler will be translated depending on the coaxial transmission line length and the operating frequency. In other words, the impedance at the input to the BPF where the sensing device is located is not representative of the impedance at the input to the antenna coupler. Therefore a new method is needed to correctly tune the antenna coupler. The TIMS provides that new method and is incorporated into the shipboard antenna coupler group.

Functional Description

The block diagram of the shipboard antenna coupler group is shown in Figure 11. The equipment uses an analog tuning system and is capable of operation with 1500 watts average and 2000 watts PEP RF input power. The tuning elements are servo motor driven vacuum variable capacitors. The directional coupler is located at the RF input to the bandpass filter. The forward and reflected voltage samples are supplied via coaxial transmission lines to the discriminator stages which are located in the control-power supply . The voltage analogs of the forward voltage, reflected voltage, and phase angle are applied via sample and hold circuits and A/D circuits to the Intel 8086 microprocessor circuit. Using these signals the microprocessor calculates the impedance which exists at the output of the directional coupler.

A calibration method is used to compensate for variations in the length of the forward and reflected voltage sample transmission lines from the directional coupler. A calibration module is included at the RF input to the antenna coupler where a phasing-loading discriminator would be located in previous antenna couplers. At initiation of a tuning cycle the directional coupler sample lines are calibrated. Tuning algorithms based on the calculated impedance at the directional coupler are used to tune the BPF. Then several known impedance RF loads are switched into the antenna coupler calibration module circuit. As each calibration load is inserted, the calculated impedance at the directional coupler is stored in memory. Subsequently during the antenna coupler tuning process, the real time calculated impedance at the directional coupler and the calibration impedances that were stored are used to calculate the impedance at the input to the antenna coupler. Tuning algorithms are used based on the calculated impedance at the antenna coupler input to control the analog tuning motor speed and direction to reach the tune point. Some of the algorithms rely on the capability of the TIMS to measure actual impedances rather than relative impedances as with the phasing-loading discriminator.

The antenna coupler group utilizes the variable attenuator capability of the TIMS for a low tune power capability. During the group tuning cycle a 6 dB pad is inserted at the input to the directional coupler to provide isolation between the untuned filter input and the transmitter output. The variable attenuator range can accomodate the 6 dB pad and the loss in the directional coupler sample coaxial transmission lines which can be up to 250 feet in length. The resulting tune power range is 50 milliwatts to 225 watts during initial tuning and 10 milliwatts to 2000 watts during surveillance tuning as a result of collocated impedance coupling. The TIMS as previously

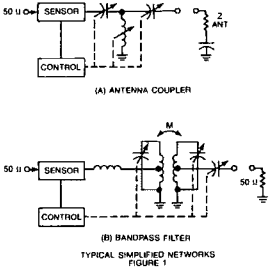
described also provides selectivity to further reduce susceptibility to the interfering signal.

AIRCRAFT APPLICATIONS

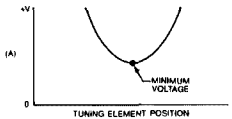
Aircraft have SIMOP problems also due to lack of space for antenna separation. We are currently implementing the TIMS into an aircraft SIMOP system. This system is for operation with 400 watts average or PEP RF input power, therefore the directional coupler can be smaller in size. Low power tuning is not a requirement so the variable attenuator is changed to a fixed attenuator and the discriminator injection frequency is changed to 50 kHz to reduce the size of the discriminator stages. The BPF and antenna coupler contain digital tuning elements.

SUMMARY

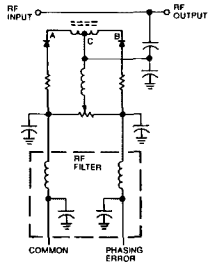
Sensing devices are needed to control automatic tuning of impedance networks. The conventional phasing-loading discriminator has been used for this purpose for many years but it has limitations for modern applications. The TIMS has been developed and patented for use as an impedance measurement system in automatically tunable impedance networks such as antenna couplers and filters. The TIMS overcomes the limitations of the conventional phasing-loading discriminator such as actual impedance measurement versus relative measurements, susceptibility to interfering signals, noise generation, and high RF power requirements. The TIMS provides accurate impedance measurements that can be used by a microprocessor along with calibration information to calculate impedances at a remote location. The TIMS has been successfully utilized in a shipboard antenna coupler group to solve SIMOP problems due to collocated antennas and is currently being implemented for an aircraft SIMOP solution.



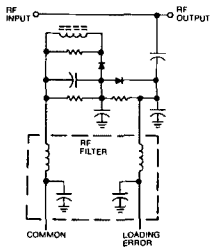
TYPICAL SIMPLIFIED NETWORKS
FIGURE 1



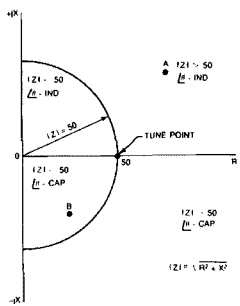
TYPICAL SENSOR SIGNALS VS ELEMENT POSITION
FIGURE 2



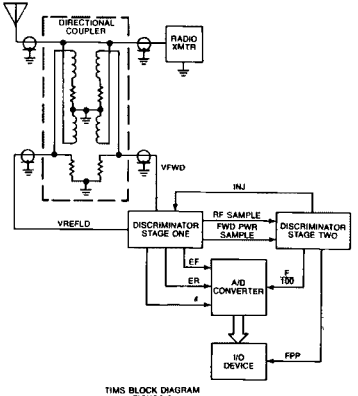
TYPICAL PHASING CIRCUIT
FIGURE 3



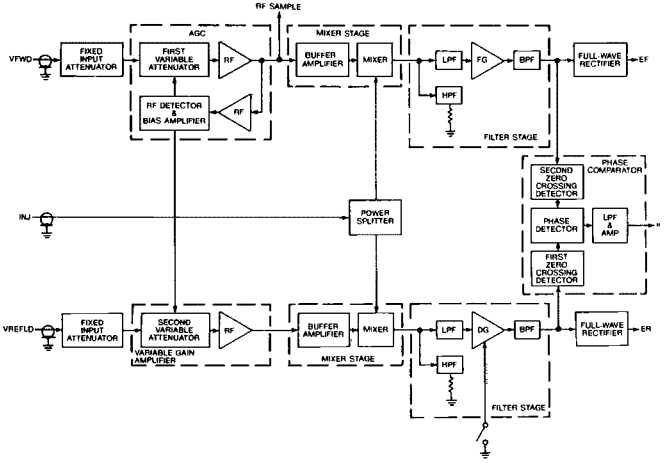
TYPICAL LOADING CIRCUIT
FIGURE 4



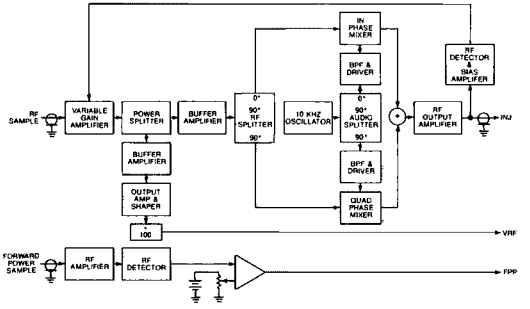
PHASING — LOADING DISCRIMINATOR RESPONSE
FIGURE 5



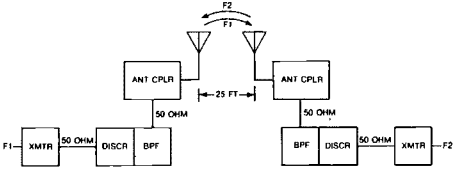
TIMS BLOCK DIAGRAM
FIGURE 6



TIMS DISCRIMINATOR STAGE ONE BLOCK DIAGRAM
FIGURE 7

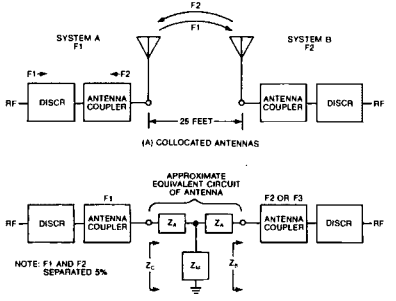


TIMS DISCRIMINATOR STAGE TWO BLOCK DIAGRAM
FIGURE 8

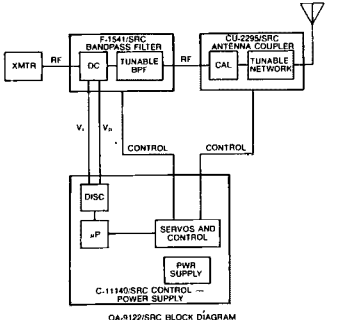


ANTENNAS MAY BE CLOSELY COLLOCATED PREVENTS TUNING PROBLEMS DUE TO INTERFERING SIGNALS. REDUCES IMD

SIMOP SOLUTION
FIGURE 10



SIMOP PROBLEM
FIGURE 9



OA-9122/SRC BLOCK DIAGRAM
FIGURE 11

CHOOSING THE RIGHT CRYSTAL AND OSCILLATOR FOR THE APPLICATION

by

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Some of the considerations which go into a decision on the choice and design of crystals and crystal oscillators are listed below:

1. Fundamental versus overtone mode crystal.
2. Parallel mode versus series mode.
3. VHF crystal versus multiplier chain.
4. Uncompensated versus TCXO or OCXO.
5. Trimable versus no trim adjustment.
6. Solder sealed package versus hybrid.
7. Voltage control required.
8. Stringent short term stability requirements.
9. Tight ageing requirements.
10. Start-up time.
11. Radiation requirements.
12. Shock and vibration rquirements.
13. Low current (battery operated).
14. Low parts count. Gate Oscillator.

In order to organize some of the above considerations, this paper arbitrarily begins with a 20 MHz , fundamental mode crystal in an HC-18 holder, to be used in an oscillator driving a receiver local oscillator chain to 400 MHz.
The characteristics of this crystal and its circuit are described and some of the options and considerations of the list are compared to this 20 MHz example.

FREQUENCY STABILITY

Assume that the oscillator has a temperature stability of ±40 PPM (parts per million) over the temperature range of -40°C to +85°C. To this must be added an ageing factor. One can conservatively assume 2 PPM ageing the 1st year of operation and a life time ageing factor of 4PPM. Using these assumptions, the worst case frequency error will be 40 + 4 or 44 PPM.

In Hertz;

$$20 * 10^{6} * 44 * 10^{-6} = 880 \text{ Hz},$$

and at the end of the x20 multiplier chain

$$20 \times 880 = 17{,}600 \text{ Hz}.$$

This frequency error would be tolerable if this fictitious local oscillator was part of a receiver with a 200 kHz I.F. bandwidth. If, however, the bandwidth were only 2 kHz,a 17600 Hz error in the local oscillator would be excessive. The narrow band assumption will be made in order to see where it leads the

oscillator design. The maximum error must now be restricted to about 200 Hz, or

$$\delta F, \text{ PPM} = 200/400 = 0.5 \text{ PPM}$$

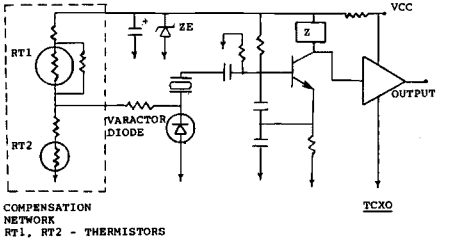
This new requirement forces the design to either a much more stable crystal oscillator, or to a system in which the oscillator is locked to a stable master reference. These two approaches will be considered next.

TCXO's and OCXO's

(Temperature Compensated Crystal Oscillator and Oven Controlled Crystal Osoillators)

Before considering the two options of TCXO and OCXO, the questions of ageing and setability must be addressed. If the receiver must operate without adjustment throughout its life, then ageing will probably determine the quality of crystal oscillator required (and therefore the price, size and D.C. power). If the frequency of the oscillator can be corrected by electrical or mechanical adjustment to remove frequency error due to ageing, the frequency accuracy will be dominated by temperature rather than age. TCXO's and OCXO's will be considered with this assumption.

Briefly, a TCXO corrects the crystal frequency versus temperature characteristic by means of a compensation network which applies a correction voltage to a varicap diode in series with the crystal. An OCXO addresses the problem by controlling the temperature at the crystal with a miniature oven. Simplified schematics of a typical TCXO and OCXO are shown in Figure 1.



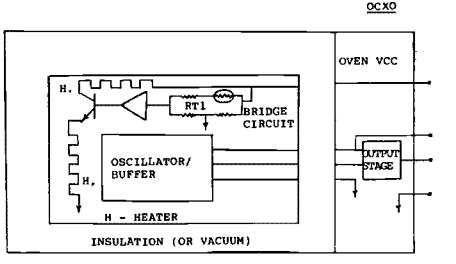


Figure 1, Simplified TCXO and OCXO

The new specification of .5 PPM puts the requirement somewhere in the grey area between TCXO's and OCXO's. Low cost, commercial TCXO's typically meet ±1 PPM over 0°C to 50°. The example oscillator's specification and temperature range puts the design near the border of the best that can be done with a TCXO, and consequently it would be a costly unit. OCXO's easily provide stabilities of $\pm 1 \times 10^{-8}$ over the required temperature range, and provide ageing rates less than 1×10^{-9} per day.

However, ovenized units are larger, heavier, and consume much more power than non-oven types. Representative specifications are shown in Table 1. Notice that some compromises may have to be made between requirements, performance, and price.

PHASE LOCKED SYSTEM

As an alternative, assume that this system already contains a stable master oscillator at 5 MHz. The basic crystal oscillator can then be locked to this master using a phase locked loop. Figure 2 illustrates the circuitry involved. Notice that a varactor in series with the crystal has been added in order to be able to pull (frequency shift) the frequency to exactly four times the reference 5 MHz.

Some notes concerning phase locking a crystal oscillator are appropriate.

1. The gain constant of a crystal controlled oscillator, KO, in Hertz per volt, is typically three to four orders of magnitude

TABLE 1 -- TYPICAL OCXO AND TCXO

SPECIFICATION	OCXO	TCXO
Frequency	5 or 10 MHz	5 to 50 MHz
Output Level	1 Vrms into 50 ohms	sinewave, TTL, or CMOS
Harmonic Distortion	-40 dBc	-20 dBc
Frequency Adjustment	+2.5 PPM minimum coarse mechanical. ±2x10E-7 fine ±1 PPM voltage control	±2x10E-6 minimum
Input Voltage	+ 12 V.D.C., ±10%	+ 12 V.D.C., ±5%
Frequency Stability vs Input Voltage	±3x10E-9 for ±10%	±2x10E-7 for ±5%
Frequency Stability vs Load	±1x10E-9 for ±10%	±2x10E-7 for ± 2:1 VSWR
Frequency Stability vs Temperature	±5x10E-9 -20°C to +75°C	±5x10E-7 -20°C to +60°C
Warm-Up Time	±1x10E-7 in 15 mins ±1x10E-8 in 20 mins	< 1 second
Aging Rate	1x10E-9/24 hours	1x10E-8/24 hours
Short Term Stability	3x10E-11 r.m.s Tau = 1 sec	1x10E-9 r.m.s Tau = 1 sec
Input Current	340ma. at turn-on 138ma. at 25°C 225ma. at -20°C	15 ma.
Size	2" x 2" x 4"	1" x 2" x 0.5"

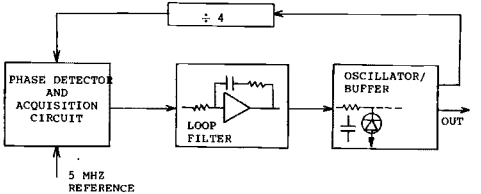


Figure 2, Phase Locking

less than that for a VCO (voltage controlled oscillator). The 20 MHz example would have an average KO of 500 Hz per volt.

2. The loop bandwidth for a phase locked loop using a crystal controlled oscillator is typically 10 to 200 Hz. Very much narrower bandwidths may cause loop phase jitter problems. Wider bandwidths are limited by frequency response roll-off caused by the narrow band nature of the oscillator.

3. The crystal oscillator must be capable of being pulled, or slewed, by an amount equal to its' temperature and ageing frequency error. This assumes that the master oscillator drift is negligible. The TCXO and the phase locked oscillator both require electronic tuning, by means of a varactor diode, or varicap. It is appropriate to discuss varactor tuning in more detail, before discussing overtone crystal oscillators because overtones have very limited "pullability."

VCXO (VOLTAGE CONTROLLED CRYSTAL OSCILLATOR

The equivalent circuit for a crystal is shown in Figure 3.

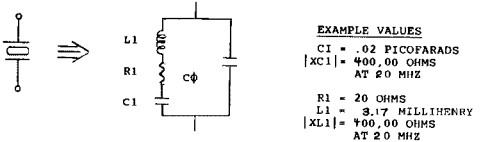


Figure 3, CRYSTAL EQUIVALENT CIRCUIT

L1, C1 and R1 represent the piezoelectric coupled mechanical resonator characteristics. C0 is the capacitor formed by the crystal electrodes. Typical values for the 20 MHz crystal are shown. When the crystal is part of a complete circuit,as shown in Figure 4, oscillation occurs at a frequency above F1, where the crystal series arm presents a net inductive reactance, resonant with the capacitors and inductors in the circuit.

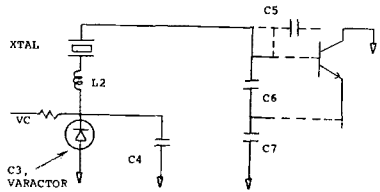


Figure 4, CRYSTAL AND CIRCUIT

The resonant frequency of the complete circuit can be calculated for any particular set of values by writing the appropriate equations for the resonant frequency and solving. This is conveniently done on a computer. Seven cases have been calculated and presented in Table 2 for typical circuit values.

In Table 2 the values of C1, C4, C6/C7, L2 and the varactor parameters (C3) are varied to show the effect on frequency pulling and linearity. A control voltage range of 1 volt to 10 volts is assumed. The frequency data is listed as; (1) PPM away from crystal series arm resonance, (2) the 1 V to 10 V frequency delta, (3) The frequency voltage sensitivity in PPM per volt, at the ends of the range.

In case 1, the difference in sensitivity at 1 V and 10 V is extreme. This results from the varactor capacity-voltage characteristic and from the loss of sensitivitiy as the crystal is pulled further from resonance. Case 2 is like Case 1 except that C1 has been halved. It is seen that the delta F is also reduced by 2, showing the direct dependance of "pullability" on C1. This is discussed in the section on overtone operation. Notice that the difference in 1 V to 10 V sensitivity is not as extreme in case 2 because the crystal is not pulled as far from series resonance. Case 3 shows that C4 reduces pulling and degrades linearity.

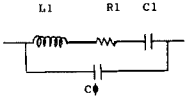
In Case 4 the varactor 4 volt value is changed from 30 picofarads to 15 picofarads, resulting in greater pullability and better linearity. Cases 5, 6, and 7 use a hyperabrupt varactor (gamma = .8) instead of the abrupt junction one. This yields improvement in pulling and linearity. Finally, Case 7 shows that the addition of a three microhenry series inductor (L2) further increases pulling. One note of caution. Reducing the varactor capacity results in an increase of the circuit parallel loss. In Case 6, for example, unless the crystal resistance is suitably low, the circuit may stop oscilleting at 10 volts.*

* This topic is addressed in the paper "Maximizing Crystal Oscillator Frequency Stability" Session R-2, r.f. expo 86.

THE OVERTONE CRYSTAL AND OSCILLATOR

It might be asked of the modal local oscillator chain, "Why start at 20 MHz?" "Why not use a 5th overtone crystal at 100 MHz, save a lot of multiplication and move the close in spurious out by a factor of 5"?

For the original stability assumption of ± 40 PPM, this might be an attractive choice. With a tight frequency tolerance, it is not, and to see why, the overtone equivalent circuit will be examined. Shown in Figure 6 below is the equivalent circuit of the same 20 MHz crystal, but for the 3rd or 5th overtone mode:



L1 = 3.17 μH; R1 = 10 TO 100 OHMS

C1; 3rd OVERTONE = $\frac{C1, \text{ FUND.}}{9}$

≈ .0022 PFD.

5th OVERTONE = $\frac{C1, \text{ FUND.}}{25}$

≈ .0008 PFD.

Figure 5, OVERTONE EQUIVALENT CIRCUIT

It is seen that the inductance remains the same, while C1 is reduced by a factor N^2, where N is the overtone, 3, 5, 7*, 9* etc. Consequently, the "pullability" of an overtone crystal is reduced by approximately the overtone number squared, compared to the fundamental mode. Typical pullability for a 60 MHz 3rd overtone would be on the order of ±30 PPM, and for a 100 MHz 5th overtone, ±10 PPM. Clearly, there is not enough pull range to use these modes in the TCXO or phase locked examples described here.

* Higher than 5th are relatively rare.

SHORT TERM STABILITY

Thus far, these systematic changes in frequency have been discussed which are due to factors such as temperature and time. Oscillator frequency is also perturbed by random, noise-like factors, and these perturbations typically are important for disturbances with time constants from microseconds to seconds. This short term stability is measured in the time domain where some type of frequency counter is the key instrument, and in the frequency domain, where spectral analysis of one form or another is used.

In many of these measurements it is necessary to use two oscillators, either with a small frequency offset, or locked together in a phase locked system. Some typical time domain values are listed in Table 1.

OTHER TOPICS IN CRYSTAL AND OSCILLATOR SELECTION

1. Clock oscillators: Miniature, self contained crystal oscillator and output buffer combinations. These hybrid units are available with output frequencies from sub-Hertz to 150 MHz. Outputs are compatible with standard logic families, TTL, CMOS, ECL. Militarized units are available with stabilities of ±50 PPM

over the temperture range -55° C to +125° C.

2. Low power oscillators: Oscillators for battery operated equipment must sometimes operate on less then one milliampere. Using AT cut crystals in the low megahertz range and special circuits this kind of requirement can be met while retaining the advantage of the AT cut crystals. For outputs in the tens of kilohertz, where looser frequency tolerances or narrower temperature ranges obtain, tuning fork crystal oscillators are available with current drains in the tens of microamperes.

3. AGC: Simple AGC control of the oscillator operating point provides many advantages. Low crystal power dissipation, important for good ageing, can be achieved while avoiding circuit start-up problems sometimes associated with very low power operation.

SUMMARY

Choosing a crystal and crystal oscillator circuit requires matching between the requirements of the application and the characteristics of the oscillator. If the oscillator must be pulled more than 10 or 20 PPM, a fundamental crystal in the 10 to 25 MHz range is probably indicated. If the ultimate in temperature stability, ageing and close-in noise is the object, a 3rd or 5th overtone, 5 MHz, ovenized unit is indicated. For small size, low cost, and nominal AT cut stability, a clock oscillator might meet the objectives.

If VHF or UHF outputs are needed a 3rd or 5th overtone crystal oscillator, operating up to 150 MHz might simplify the design.

TABLE 2 - VCXO

	CIRCUIT PARAMETERS C3, VARACTOR									FREQUENCY PULLING DELTA F, PPM				
CASE	C1	CD	4V.C	GAMMA	C4	C5	C6/C7	L2		1V	10V	DELTA	DF/DV (1V)	DF/DV (10V)
1	.02	5	30	.5	0	2	100	0		322	519	197	38	4
2	.01	5	30	.5	0	2	100	0		161	259	98	19	7
3	.02	5	30	.5	20	2	100	0		284	363	79	20	4
4	.02	5	15	.5	0	2	100	0		447	753	306	65	20
5	.02	5	15	.8	0	2	100	0		379	858	479	87	34
6	.02	5	15	.8	0	2	50	0		488	912	424	76	30
7	.02	5	15	.8	0	2	100	3		-5	680	685*	130	45

* Even greater pulling can be accomplished with a more complex circuit.

THE USE OF A COMPUTER MODEL TO DETERMINE THE COMPLEX PARAMETRIC RELATIONSHIPS OF A CRYSTAL OSCILLATOR CIRCUIT

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INTRODUCTION

The circuit modeled by the computer program is a 10Ø MHz Pierce crystal oscillator driving a common base buffer amplifier. The oscillator was developed by Piezo Systems for a satellite project. Because of the strict design criteria required by the customer for qualification of the oscillator, the modeling program was developed to allow design and analysis to be performed during the prototype phase of the project. As will be shown in this paper, the modeling program created an extremely valuable tool for the oscillator design and was used throughout the project for complex analysis which would have been extremely difficult and time consuming. From this analysis, some very important complex parameters of the oscillator circuit were determined. These include crystal drive, gain margin, loaded Q of the resonator, group delay of the feedback loop and phase slope. The calculation of these parameters allow a prediction of the phase noise contribution of the oscillator as a signal source.

THE COMPUTER MODEL

The computer program models the circuit in an open loop configuration. As shown in Figure 1, the loop is broken at the input to the base of the oscillator transistor. The input impedance of the oscillator transistor is included in the calculation of the collector load. Therefore, the program analysis is simply the calculation of the swept response of a two port network with a complex load determined by the relationships of the circuit elements. From the two port response, the following may be determined: the transistor stage gain with respect to the collector load, the loss due to the feedback loop network, the loss due to the power output to the buffer amp, the magnitude and phase of the collector load and the magnitude and phase of the total loop gain around the oscillator circuit.

The various gain blocks described above are broken down by using complex algebra to calculate the equivalent networks of the circuit elements. The transistor's contribution to the gain blocks is found by using S parameter data obtained for the transistor at the same DC operation point as used in the circuit. As shown in Figure 2, the circuit elements are divided into 2 gain blocks. Gain block 1 includes the crystal resonator and the two paralleled capacitors across the base of the oscillator transistor (C2 and C3). The complex impedance of the crystal includes the shunt capacitance (Co) of the crystal

enclosure and the equivalent reactive elements and series resistance of the resonator as entered at the initialization of the program. Gain block 1 represents the loss of the feedback network of the circuit. Gain block 2 includes the capacitive tap off the collector tank (C7 and C9), the coupling resistor between the stages (R13) and the input impedance of the buffer amp. The input impedance of the buffer amp was measured to be about 27 ohms resistive. Though the common base amp should be very low impedance at 100 MHz, enough positive feedback occurs through stray circuit board reactance to increase it to its measured value. The emitter degeneration resistor (R5) is included with the input impedance of the buffer amp to give the circuit element (ZIN2) of Figure 2. Gain block 2 represents the loss due to the power incident to the buffer amp through the capacitive tap (C7 and C9).

The available power gain of the transistor stage is calculated by the use of the measured S parameters of the transistor two port and the reflection coefficient of the collector load normalized to a 50 ohm system. First, the impedance of gain blocks 1 and 2 is calculated as two paralleled networks. The reactance of the capacitive tap capacitor C7 is then added in series. The collector load (ZL) is calculated by the paralleled impedance of the equivalent impedance of the gain blocks 1 and 2 and the impedance of the collector tank (L1, C5 and C6). This allows the reflection coefficient of collector load in a 50 ohm systems to be determined by the formula:

$$\Gamma L = \frac{(ZL - 50)}{(ZL + 50)}$$

The available power gain is found by the ratio of the reverse scattering coefficient of the equivalent two port to the forward scattering coefficient with respect to L. This is calculated by the use of the following formula:

$$Pav = \frac{(S_{21} \times \Gamma L) + S_{21}}{((1 - (S_{22} \times \Gamma L))\ (1 + S_{11}))\ (S_{12} \times S_{21} \times \Gamma L)}$$

Also, the input impedance of the oscillator transistor may be calculated by the formula:

$$\Gamma in = S_{11} + (S_{21} \times S_{12} \times L)$$

$$Zin1 = \frac{50\ (1 + \Gamma in)}{(1 - \Gamma in)}$$

From the development of the gain blocks, the total loop gain is simply:

$$Aloop = Pav \times G_1 \times G_2; \quad \begin{matrix} G_1 \text{ is the loss of gain block 1} \\ G_2 \text{ is the loss of gain block 2} \end{matrix}$$

The above description of the analysis illustrates the completeness by which all of the circuit elements are modeled. This allows a fairly large and detailed initializaton table to be constructed for the model. The effects of individual circuit elements may therefore be examined. Table 1 lists the circuit elements available for input at initialization. The program runs in a "DO FOR" loop with each repetition corresponding to a subsequent increase in sweep frequency. Initially, the program

starts at 500 Hz below the series resonant frequency of the crystal and increases in 50 Hz steps to 2500 Hz above the series resonance frequency of the crystal. The oscillation point occurs where the "phase open loop" term goes to zero. Table 2 is the computer model's output for a 35 ohm crystal swept from 700 Hz to 2100 Hz above series resonance of the crystal. The output headings are summarized in Table 3. The explanations for the "E2" and "Ixstal" columns will follow in the next section of the paper.

CRYSTAL DRIVE ESTIMATION BY THE COMPUTER MODEL

The crystal used in the oscillator circuit is a 100 MHz, 5th overtone AT-cut. A major problem with AT-cut resonators is flexure mode coupling of other resonant responses within the crystal at fairly high drive levels. Crystal drive is the power dissipation in the resonator. It is determined by the series resistance of the crystal and the AC current through the resonant circuit by the formula: $P = I^2R$. The effect of the model coupling is pertubations in the frequency/temperature curve of the crystal. These unwanted frequency dips can cause sudden drops in frequency by as much as 2 to 3 ppm at specific temperatures over the operation range.

Figure 3 is an example of a crystal with temperature pertubations. During the design review of the crystal development for the oscillator project, a guard band of 2 mW of drive was imposed by the customer to screen the crystals for acceptance. The 2 mW drive was selected to secure against possible drive increases during the oscillator's life in the satellite. However, this estimated drive level caused frequency pertubations in most of the resonators. The yield through the screening process fell to a severely low level. Because of the computer program's ability to determine current gains around the oscillator loop, the analysis of the output parameters was used to re-evaluate a more reasonable screening level for the resonator drive. The end-of-life criterion could more accurately be determined.

For the drive prediction, a way to determine crystal current is needed. This was developed by straightforward network analysis from the output parameters of the program. The feedback network of gain block 1 is driven by the AC voltage developed at the junction of the capacitive tap C7 and C9. This AC voltage is designated "E2" by the program. E2 is calculated by the following formula:

$$E2 = I_{limit} \times G2 \times ZL$$

"I_{limit}" is the measured DC collector current of the oscillator transistor. An average value of 7.19 mA was used for this parameter. G2 is simply the actual gain ratio of the "DBG2" output parameter and ZL is as stated in Table 3. Multiplying

llimit by ZL gives the maximum AC collector voltage. G2 then incorporates the loss to the output buffer. With E2 determined, the crystal current may then be calculated. At the capacitive tap, the crystal is a series element to the input of the oscillator transistor. The input impedance of the transistor and the base to ground capacitors C2 and C3 form a reactive divider. This voltage division is represented by "DBG1". G1, the actual gain ratio of "DBG1", is the value:

$$G1 = \frac{E1}{E2}$$

E1 is the voltage incident on the base of the oscillator transistor on the opposite side of the crystal. Therefore, the crystal current may be calculated by using the crystal impedance at the point of interest:

$$Ixstal = \frac{Vxstal}{Zxstal}$$; Vxstal is the voltage drop across the crystal; Zxstal is the complex impedance of the crystal

$$Vxstal = E2 - (E2 \times G1) = E2 - E1$$

therefore, $$Ixstal = \frac{E2 - (E2 \times G1)}{Zxstal}$$

From this analysis, not only was an accurate crystal current determined but an easily measurable point, "E2", was found to make empirical measurements of crystal drive in the actual oscillator unit.

The voltage at E2 can be measured with a high impedance RF voltmeter. The capacitance of the voltmeter probe is approximately 2.2 pF which is only 6% of the capacitance of C9. Therefore, the loading impact to the circuit is minor. Table 4 lists the measured value of E2 for various crystals at acceptance screening. Notice that the values of the measured E2 voltage are within 5% of the E2 values predicted by the computer program. The predicted values for E2 of each crystal were determined by inserting the individual crystal parameters into the initialization of the input to the program. The calculated drive for crystal serial number 232:

$$(4.753 \text{ mA})^2 \times 39 \text{ ohms} = 881 \text{ microwatts}$$

Because of the accuracy of the predicted E2, the predicted Ixstal could be used to calculate the drive above. Since the calculated drive for the oscillator is under 1 mW, a re-evaluation was accomplished by varying the initialization table of the program by realistic end-of-life tolerances on the circuit elements and DC input. Table 5 lists impact to the drive budget of various tolerance changes of the oscillator circuit elements. Very little change is recorded by component changes due to tolerance drift. The DC input variance of the power supply is guard banded by +/-5%. By changing the DC input by +/-5% and measuring the E2 value with the RF meter, the worst case increase in drive was found to be less than 100 microwatts. Therefore, a more accurate guard band in drive was estimated to be 1.1 mW. An additional 400 microwatts was added to the guard

band to insure a margin. The new screening drive for crystal acceptance was reduced to 1.5 mW.

The empirical measurement technique was then used to set the oscillator for 1.5 mW drive level by increasing the power supply to arrive at the necessary E2 value. Table 4 summarizes the results of the screening test. The 1.5 mW "Ixstal" was determined by:

$$(1.5\ \text{mW})\ \text{Ixstal} = \sqrt{\frac{1.5\ \text{mW}}{\text{Xstal resistance}}}$$

The required E2 voltage is found by:

$$\frac{(\text{E2 predicted})(1.5\ \text{mW Ixstal})}{(\text{Ixstal predicted})} = 1.5\ \text{mW E2 measured}$$

The accuracy of the computer model is confirmed by the above discussion. Therefore, it should have the ability to predict some more difficult circuit parameters.

DETERMINATION OF COMPLEX CIRCUIT PARAMETERS BY THE PROGRAM MODEL

Figure 4 is a graph of four important output parameters of the program over a wide sweep of the circuit in 100 Hz increments. The various curves illustrate the operation of the Pierce oscillator. The loop gain is shown increasing to a peak at around 700 Hz above series resonance. This allows the oscillation build-up to occur before the oscillator achieves a steady state at "zero loop phase". Consequently, the Allen variance of the oscillator will decrease to a final steady time domain value. At the same time, the crystal current is seen building as the loop gain increases, peaking at 700 Hz. This corresponds to a crystal drive of 1.46 mW, almost 600 microwatts greater than the final steady state value. Again, the extra drive causes a rapid build-up of energy in the resonator to overcome the unstable loop phase at start-up. The start-up times measured for the oscillators were approximately 12 msec.

The E2 curve illustates the effect of the resonator impedance. The curve reaches a minimum approximately at series resonance of the crystal. This where the crystal has its lowest impedance and therefore loads E2 the most. As the phase approaches zero, the resonator circuit becomes increasingly higher in impedance. E2 rises until the resonator impedance reaches its maximum and E2 no longer changes. Notice that the E2 curve is very much like the passive network sweep of a crystal resonator. The phase of the loop steadily decreases to an operating point about 1400 Hz above series resonance. From Table 4, this gives an operation frequency of 100 MHz +/-2ppm for all of the series resonance frequencies listed. The oscillator indeed operates at 100 MHz. Further examination of the curves of Figure 4 allows gain margin, loaded resonator Q, and phase slope to be determined.

Just as the computer model can perform an open loop sweep of the modeled circuit, an actual empirical sweep may be accomplished. Figure 5 shows the test schematic for the empirical sweep. The circuit is broken at the input to the

crystal. This occurs at the junction between gain block 1 and 2. The terminations at the circuit breaks are chosen to approximate those seen during closed-loop conditions. The input to gain block 1 is terminated by a paralleled resistor/capacitor combination equivalent to R13 and Zin2. The input to gain block 2 is terminated by a "dummy" crystal and capacitor in series to simulate the loading of gain block 1. A frequency synthesizer was used to drive the loop and a vector voltmeter was used to record phase and gain changes on either side of the open circuit. Probe A, the reference probe, measures the input to the loop, while probe B measures the phase and gain change. The vector voltmeter connects the loop in a way without completing the circuit.

The gain margin of the oscillator loop is the excess gain present in the circuit above that required for stable oscillation. By what is commonly referred to as the Nyquist criterion, the active gain and the feedback must satisfy the inequality $\alpha x\ B > \text{or} = 1$. The gain margin is a guard band for this function. In other words, the excess gain allows an amount of loss due to detrimental effects such as transistor transconductance decrease or loop impedance increase. The greater the gain margin, the stronger the oscillator's ability to withstand such effects. Table 6 is the data gathered for an empirical open loop measurement of a typical 35 ohm crystal. At zero loop phase, a gain margin of 5.6 dB is calculated. Gain margin is found by the formula:

$$\text{Gmargin} = 20 \times \text{LOG}\left(\frac{B}{A}\right) - 20 \times \text{LOG}\ (\text{COS}\ \emptyset)$$

The value found on Figure 4 at the operating point is about 6 dB. This is an error of 7%. However, it should be noted that the empirical open loop sweep was done on small signal levels which may cause some error in measurement correlation.

The loaded Q of the resonator and the phase slope of the open loop are important parameters in the phase stability of the oscillator. The loaded Q of the resonator represents the actual resonance bandwidth of the crystal in the loop. By examining the crystal current in Figure 4, an estimate of the loaded Q can be made. The maximum current is 6.471 mA. The 3 dB current is 3.243 mA. Therefore, the calculated loaded Q is found by the formula:

$$Q_L = \frac{Fo}{BW_{3dB}}$$

A value of 34,385 is determined. This represents about 30% of the typical unloaded Q of the resonators which is generally true for Pierce oscillators. The phase slope is the rate of change in phase with frequency. This curve represents a transfer characteristic to frequency stability. The phase jitter of the oscillator is directly dependent on the phase slope. An operating point is found on a rather shallow portion of the curve. It may be assumed that the phase stability of the oscillator is not as great as it could be. Phase slope may be related to the loaded Q of the circuit by the following:

$$\frac{\Delta\theta}{\Delta f} = \frac{2Q_L}{f_o}$$

However, the group delay of the oscillator is related by the relationship $Q = \pi \times f_o \times \tau$, where τ is the group delay. The group delay through the oscillator is the propagation delay around the loop. Oscillators with large group delays exhibit very good short term stability in the time domain. The group delay is related to frequency jitter by:

$$\frac{\Delta f}{f_o} = \frac{Q}{2\pi f_o \tau}$$

The advantage of analyzing frequency jitter this way is that the θ and τ variables may be split into their individual components. 1) It is not in the scope of this paper to present this concept. However, the group delay can be calculated for the oscillator by the formula:

$$\frac{\Delta\theta}{4f(360)} = \tau$$

This is directly proportional to the phase slope. From Figure 4, a value of 0.109 msec. is calculated at the operating point. The group delay may be determined in another way. Since the loaded Q is known, the group delay is found by:

$$\frac{Q_L}{f_o \pi} = \tau$$

Again, the value of 0.109 msec. is calculated. The group delay for the oscillator has been determined in two different ways using the output parameters of the program. The loaded Q of the oscillator can allow a prediction of the phase noise response of the circuit.

The construction of the phase noise response occurs in three steps: the signal to noise floor, the noise rise due to white noise within the resonator bandwidth and the contribution of 1/f noise from the active device. The signal to noise ratio is found by the following:

$$SNR = 10 \log \left(\frac{Pavs}{FkT}\right)$$
$$SNR = Pavs - NF - 174 dBc/Hz$$

Pavs is the power available from the gain source. It can be determined by adding "DBG2", DBG1 and "DBOPLOP" from the program parameters. This represents the gain of the oscillator transistor. A value of 26.44 dB is found for the operation point of Table 2. Since no noise figure analysis was done for the oscillator amplifier, a value will have to be assumed. A value of 3.5 dB is reasonable for semiconductors of the type used in the oscillator circuit. This gives a signal to noise floor of 151 dB. The noise rise due to modulation within the resonator bandwidth can now be determined. A general formula used for this purpose is:

$$\mathcal{L}(fm) = -SNR - 3dB + 10 \log \left(\frac{f_o}{2fm\ Q_L}\right)$$

The formula relates the FM modulation index with the loaded Q of the circuit. 3 dB is subtracted due to AM contributions occurring simultaneously in the noise floor. Finally, the 1/f noise contribution is added. With an oscillator of this type, the major contribution of shot noise is from the transistor. The formula which can relate this contribution to the previously determined noise is:

$$(fm) = -SNR - 3dB + 10\log\left(\frac{fo}{2fm\ Q_L}\right) + 10\log\left(1 + \left(\frac{fo}{2fm\ Q_L}\right)^2\right)$$

Table 7 shows the phase noise prediction with the use of this formula to the actual measured noise of the circuit. The two predictions are based on the two loaded Q's available from the analysis. One is the 3 dB current bandwidth found from the computer program. The other is the phase slope determined from the open loop sweep of Table 6. The phase noise prediction is therefore fairly accurate both with the empirical and modeled open loop sweeps.

SUMMARY

The advantage of the computer model is clearly demonstrated by the above results. Rather straightforward network analysis produces a labor saving tool because of the computer's number handling capability. Insight gained by examining the analysis led to new empirical techniques for rather complex measurements. Because of the accurate characterization of the circuit, the operation of a Pierce oscillator was presented in graphic detail. Further examination of the output parameters allowed difficult but important circuit relationships to be determined. It is apparent that with more detailed analysis of the computer model's output, further work can be accomplished in the oscillator's design and improvement. Ultimately, the model could be generalized to meet various oscillator types and improve the understanding of crystal oscillator circuits.

REFERENCES AND ACKNOWLEDGMENTS

The author expresses his appreciation for the contributions of Pat Godwin to the development of the computer model.

1) Ron Rippy, "A New Look at Source Stability," Microwave, August 1976, pp. 42-48.

2) Roger Muat, "Designing Oscillators for Spectral Purity, Part 1," Microwaves and RF, July 1984, pp. 133-142 and p. 160.

TABLE 1

C2 and C3: parallel capacitors to base of oscillator transistor

C0: stray capacitance of crystal enclosure (TO-5 style package)

C_1: motional capacitance of crystal resonator

R_1: series resistance of crystal resonator

Zin2: complex matrix of input impedance of the buffer amp

R13: coupling resistor between oscillator and buffer amp

C9: grounding capacitor of capacitive tap

R5: emitter degeneration resistor of buffer amp

C7: coupling capacitor of capacitive tap

RL1: resistance of collector tank inductor of oscillator

L1: inductance of collector tank inductor of oscillator

C5 and C6: tuning capacitors of collector tank of oscillator

F1: series resonance frequency of crystal

S_{11}, S_{12}, S_{21}, S_{22}: S parameters of oscillator transistor

FD	DBOPLOP	PHOPLOP	PXL	PHXL	DB01	PH01	DB02	PH02	E2	Intel
700	9.508	44.300	119.196	-61.014	-6.2811	-120.018	-6.7509	51.162	0.313	6.471
750	9.459	40.640	121.106	-59.870	-6.7723	-123.502	-6.4360	50.026	0.330	6.482
800	9.373	36.992	123.333	-58.882	-7.2708	-126.646	-6.1667	48.707	0.347	6.470
850	9.252	33.386	125.809	-55.069	-7.7708	-129.482	-7.9425	47.281	0.363	6.434
900	9.098	29.848	128.457	-57.436	-8.2680	-132.039	-7.7608	45.808	0.378	6.375
950	8.912	26.404	131.203	-56.980	-8.7592	-134.348	-7.6173	44.338	0.393	6.295
1000	8.697	23.075	133.974	-56.689	-9.2422	-136.436	-7.5073	42.905	0.406	6.197
1050	8.457	19.876	136.709	-56.546	-9.7158	-138.328	-7.4256	41.533	0.419	6.084
1100	8.195	16.819	139.358	-56.530	-10.1789	-140.046	-7.3676	40.238	0.430	5.958
1150	7.913	13.912	141.883	-56.621	-10.6312	-141.611	-7.3287	39.026	0.439	5.821
1200	7.616	11.157	144.257	-56.799	-11.0724	-143.038	-7.3059	37.900	0.448	5.677
1250	7.307	8.556	146.466	-57.044	-11.5026	-144.345	-7.2954	36.859	0.455	5.529
1300	6.987	6.107	148.500	-57.341	-11.9219	-145.543	-7.2948	35.899	0.462	5.377
1350	6.660	3.804	150.360	-57.674	-12.3306	-146.644	-7.3018	35.017	0.467	5.225
1400	6.328	1.645	152.051	-58.033	-12.7291	-147.659	-7.3147	34.207	0.472	5.073 900uW
1450	5.992	-0.383	153.575	-58.408	-13.1177	-148.597	-7.3322	33.462	0.475	4.923 848uW
1500	5.654	-2.282	154.954	-58.791	-13.4969	-149.465	-7.3530	32.779	0.479	4.776
1550	5.315	-4.041	156.188	-59.176	-13.8669	-150.270	-7.3763	32.151	0.481	4.633
1600	4.977	-5.727	157.292	-59.559	-14.2283	-151.019	-7.4014	31.573	0.483	4.493
1650	4.640	-7.289	158.278	-59.936	-14.5814	-151.716	-7.4276	31.040	0.485	4.359
1700	4.306	-8.752	159.158	-60.304	-14.9267	-152.366	-7.4546	30.549	0.486	4.228
1750	3.974	-10.125	159.941	-60.662	-15.2644	-152.973	-7.4819	30.096	0.487	4.103
1800	3.645	-11.413	160.637	-61.009	-15.5951	-153.542	-7.5094	29.676	0.487	3.983
1850	3.319	-12.623	161.257	-61.344	-15.9189	-154.074	-7.5367	29.288	0.488	3.867
1900	2.997	-13.760	161.807	-61.666	-16.2363	-154.574	-7.5638	28.927	0.488	3.757
1950	2.678	-14.830	162.295	-61.976	-16.5475	-155.044	-7.5905	28.592	0.488	3.650
2000	2.364	-15.837	162.729	-62.272	-16.8530	-155.487	-7.6168	28.281	0.487	3.549
2050	2.054	-16.786	163.113	-62.557	-17.1528	-155.903	-7.6425	27.990	0.487	3.452
2100	1.747	-17.682	163.454	-62.829	-17.4474	-156.296	-7.6676	27.718	0.487	3.359

Table 2

Notes: If C5 = 42 pF, F1 ≈ 100 000 000 – 1200 Hertz, FD = F – F1

Table 1. Computer Model predicted response (open loop) for a 35 ohm crystal.

7/11/84

TABLE 3

FD: offset + or - from crystal series resonance in Hz

DBOPLOP: open loop gain in dB

PHOPLOP: open loop phase in degrees

PZL: absolute magnitude of collector load of oscillator transistor in ohms

PHZL: polar angle of collector load in degrees

DBG1: circuit loss of gain block 1 in dB

PHG1: phase shift associated with gain block 1 in degrees

DBG2: circuit loss of gain block 2 in dB

PHG2: phase shift associated with gain block 2 in degrees

TABLE 5

Circuit Element	Tolerance Change	Drive at Zero Phase	Frequency offset From Series
Nominal 35 ohms xtal osc.		798 x 10^{-6} watts	1500 Hz
C7 and C9	C7 +1%, C9 -1%	800 x 10^{-6} watts	1500 Hz
C5	- .166pF	820 x 10^{-6} watts	1500 Hz
C5	+0.166pF	825 x 10^{-6} watts	1450 Hz
C2 and C3	(.2 + C3) -3pF	808 x 10^{-6} watts	1500 Hz
Nominal 19 ohm crystal		840 x 10^{-6} watts	1400 Hz
Nominal 40 ohm crystal		790 x 10^{-6} watts	1550 Hz

TABLE 4

XSTAL SERIAL #	SERIES RESISTANCE:	Co	C1	Fseries	COMP. PRED. E2	COMP. PRED. Ixstal	MEASURED E2	1.5mW Ixstal	1.5mW E2
232	39 ohms	2.34pF	0.00039pF	99.998510	486 mV	4.753 mA	500 mV	6.20 mA	652 mV
237	35 ohms	2.36pF	0.00038pF	99.998530	519 mV	5.429 mA	515 mV	6.55 mA	621 mV
214	35 ohms	2.40pF	0.00040pF	99.998180	518 mV	5.486 mA	519 mV	6.55 mA	619 mV
228	34 ohms	2.32pF	0.00041pF	99.998200	522 mV	5.497 mA	521 mV	6.64 mA	629 mV
221	35 ohms	2.30pF	0.00042pF	99.998250	520 mV	5.396 mA	520 mV	6.55 mA	631 mV
232	39 ohms	2.34pF	0.00039pF	99.998280	514 mV	5.028 mA	519 mV	6.20 mA	639 mV
246	34 ohms	2.32pF	0.00036pF	99.998160	521 mV	5.533 mA	520 mV	6.64 mA	624 mV
239	34 ohms	2.28pF	0.00042pF	99.998440	523 mV	5.450 mA	523 mV	6.64 mA	637 mV
230	34 ohms	2.24pF	0.00041pF	99.998280	522 mV	5.510 mA	520 mV	6.64 mA	626 mV
215	37 ohms	2.20pF	0.00036pF	99.998580	516 mV	5.287 mA	519 mV	6.36 mA	624 mV
244	34 ohms	2.28pF	0.00042pF	99.998410	523 mV	5.450 mA	520 mV	6.64 mA	627 mV
282	42 ohms	2.16pF	0.00041pF	99.998690	511 mV	4.850 mA	518 mV	5.98 mA	638 mV
283	42 ohms	2.14pF	0.00038pF	99.998870	517 mV	4.825 mA	517 mV	5.98 mA	640 mV
291	44 ohms	2.08pF	0.00033pF	99.998990	511 mV	4.649 mA	508 mV	5.83 mA	637 mV
284	47 ohms	2.12pF	0.00040pF	99.998920	507 mV	4.452 mA	510 mV	5.65 mA	647 mV
275	42 ohms	2.18pF	0.00038pF	99.998730	511 mV	4.819 mA	517 mV	5.97 mA	641 mV
281	39 ohms	2.19pF	0.00042pF	99.998850	515 mV	5.073 mA	512 mV	6.20 mA	625 mV
265	39 ohms	2.19pF	0.00042pF	99.998640	515 mV	5.073 mA	517 mV	6.20 mA	631 mV
286	44 ohms	2.12pF	0.00035pF	99.998930	509 mV	4.719 mA	512 mV	5.84 mA	633 mV

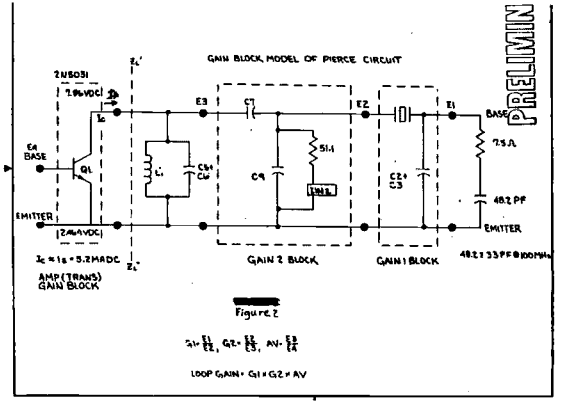
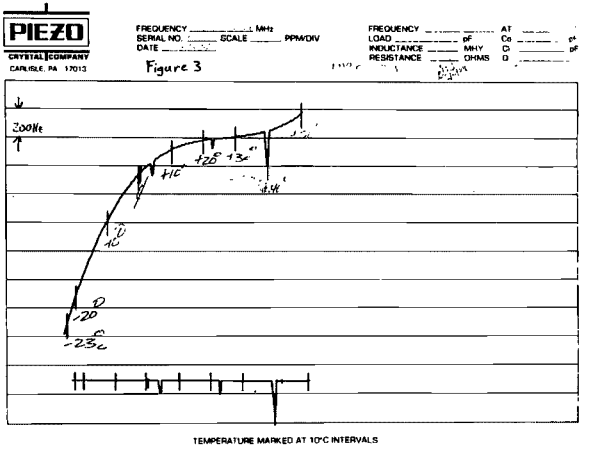
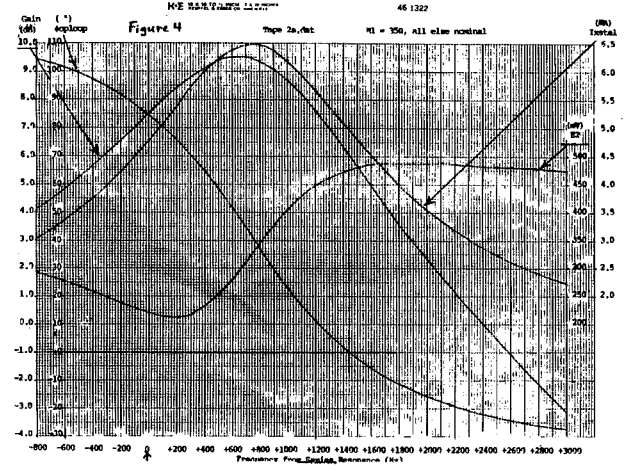


Figure 2



TEMPERATURE MARKED AT 10°C INTERVALS



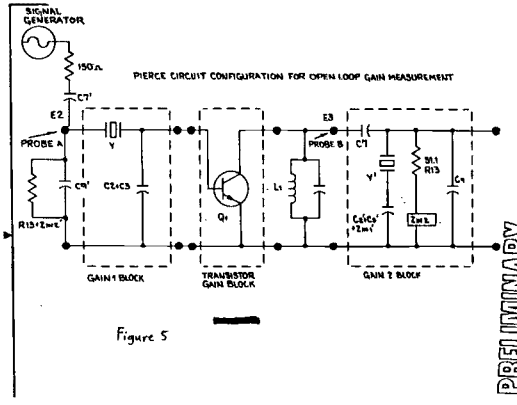


Figure 5

PRELIMINARY

HARMONIC FILTERING AT UHF AND MICROWAVE FREQUENCIES

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The need for good filtering at a reasonable cost, size and performance is important to the designer of communications systems and/or equipment. For instance, harmonic suppression in oscillators have traditionally utilized low or band pass filter circuits to reduce distortion. These types of filters usually have well defined "skirt(s)" and high out-of-band rejection that require coupled, multi-element, high Q resonators.

At UHF and microwave frequencies, distributed elements (transmission lines of prescribed impedance) are employed to achieve an acceptable design due to their higher Q and predictability at microwave frequencies compared with standard lumped elements. However, distributed element filters also have problems. Tuning ("tweaking") multi-distributed elements in production is tedious and odd frequency reentrant modes are omnipresent. Tuning is a problem in that the lengths of the distributed elements must be altered (shortened/lengthened) in the alignment of the filter. This is not easy since the multi-resonant elements interact. The reentrant issue is one that is difficult to deal with in design and generally requires a compromise in performance to minimize its effect. By concentrating on the harmonic frequencies and the reentrant nature of distributed elements, a designer can turn a problem into a simple solution.

Before actually designing any filter using transmission lines, it is important to understand transmission line resonant circuits and their reentrant behavior. The general expression for the impedance down a dissipationless transmission line is:

$$Zin = Zo*((Zl+jZo*\tan(B*l))/(Zo+jZl*\tan(B*l))) \qquad \text{(Eq.1)}$$

where: Zo = characteristic impedance of the transmission line

B = 2*Pi/L

L = the frequency wavelength in the transmission line.

l = the length of the transmission line between Zin & Zl.

Zl = the load impedance on the end of the line.

To form a simple minimum loss resonant circuit, Zl can be a short-circuit (Zl=0) or Zl can be an open-circuit (Zl=00). In reality, at microwave frequencies even a good short-circuit is slightly inductive (due to its finite length) and an open-circuit is slightly capacitive (due to end fringing capacitance). Both these parasitic effects require the transmission line to be

slightly longer to achieve a desired Zin that would normally be predicted by Eq.1.

If Zl=0 (short-circuit load) is substituted into Eq.1 then:

Zin = Zsc = jZo*Tan(2*Pi*l/L) (Eq.2)

From the transcendental nature of Eq.2, it is apparent that the impedance of a shorted transmission line has more than one unique length; (l) for a given wavelength, (L) at which it will be series resonant at Zsc = 0, and parallel resonant at Zsc = 00. Therefore, from Eq.2 the following information can be derived:

Zsc = 0 when l = 0, L/2, L, (3/2)*L, 2*L, ...

Zsc = 00 when l = L/4, (3/4)*L, (5/4)*L, (7/4)*L, ...

If Zl = 0 (open-circuit load) and is substituted into a rearranged form of Eq.1 then:

Zin = Zoc = -jZo*Cot(2*Pi*l/L) (Eq.3)

Eq.3 is also transcendental, and it is apparent that the impedance of an open transmission line has more than one unique length (l) for a given wavelength (L) at which it will be parallel resonant at Zoc = 00 and series resonant at Zoc = 0. From Eq.3 the following information can be derived:

Zoc = 00 when l = 0, L/2, L, (3/2)*L, 2*L, ...

Zoc = 0 when l = L/4, (3/4)*L, (5/4)*L, (7/4)*L, ...

From inspection of the derived length (l) data for Zsc and Zoc, it can be concluded that the shortest or fundamental line for a distributed resonant circuit is one-quarter wavelength (L/4). This excludes l=0 because it is outside the boundary conditions for a finite resonant element.

Thus far the discussion of distributed resonant circuits has been confined to a fixed wavelength (L) or frequency with a variable line length (l). This constraint has allowed the concept of the fundamental one-quarter wavelength to be established as a basic resonant building block for a filter. From a practical stand point (l) is fixed and by definition (L) is variable across the frequency spectrum. The relationship between wavelength (L) and frequency (F) is:

$$L = Vp/F \qquad \text{(Eq.4)}$$

where: Vp = velocity of propagation of the wave within the line.

For purposes of further discussion, the angular expression in Eq.2 and Eq.3 can be rewritten in the following form:

$$2*Pi*l/L = (Pi/2)*(F/Fo) \qquad \text{(Eq.5)}$$

where: l = Lo/4

Lo = Vp/Fo

Fo = fundamental resonant frequency

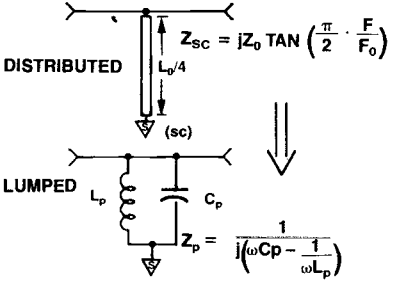


Figure 1.

Figures 1 and 2 show Lo/4 shunt transmission lines with short-circuit and open-circuit loads respectively. Their analogous lumped element equivalent is shown adjacent to them.

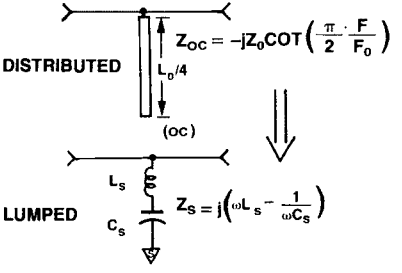


Figure 2.

The impedances (Zsc and Zoc) of the distributed circuits in Figures 1 and 2 are shown plotted versus freuency in Figures 3 and 4 respectively:

Figure 3.

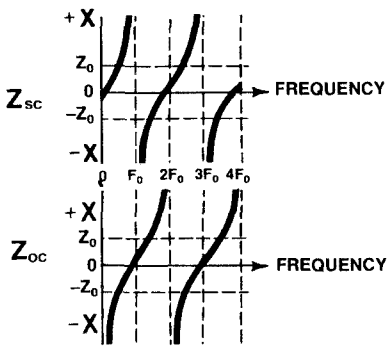


Figure 4.

The multiple parallel and series resonances are unique to distributed elements compared to their lumped element counterparts which have only one resonant frequency.

It should be apparent by now what is meant by the reentrant or periodic nature of distributed resonant elements from Figures 3 and 4 and how they can be used as repetitive band-reject filters to suppress harmonics in an oscillator application. However what might not be obvious is how to achieve parallel resonance at the fundamental oscillator frequency (F1) and series resonance at the even and odd harmonics of that frequency. The distributed circuit shown in Figure 5 is the key structure and the initial step in designing such a filter.

There is a unique characteristic about a shorted quarter-wave resonator. No matter where it is tapped along its length, it will always be parallel resonant.

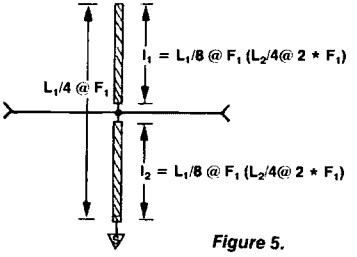


Figure 5.

The reason for this is that shorted transmission lines less than (L/4) (i.e. l2) will always be inductive and open transmission lines less than (L/4) (i.e. l1) will always be capacitive. If (l1 +l2) = (L1)/4 then the two resultant reactances (or susceptances) will be equal in magnitude and opposite in sign on the imaginary impedance axis. Thus the shunt configured circuit in Figure 5 is parallel resonant at the frequency F1. This can be readily proved by substituting l = (L1)/8 and L = L1 into Eq.2 and Eq.3 which yields:

Zsc = jZo and Zoc = -jZo

Since it makes little difference where a shorted quarter-wave transmission line is tapped to achieve a parallel resonance, the next question might be why was the circuit in Figure 5 configured such that l1 = l2 = (L1)/8? The answer to that is simple. Series resonance (band-reject) will occur: when l1 = L/4 at 2*F1, (3/4)*L at 6*F1, (5/4)*L at 8*F1,..... and when l2 = L/2 at 4*F1, L at 8*F1,..... Thus, the circuit in Figure 5 exhibits the composite impedance of that shown in Figures 3 and 4: where Fo = 2*F1.

The filter structure in Figure 5 is, however, only good for filtering "even" harmonics of the desired or band-pass frequency F1. All the "odd" harmonics (3*F1, 5*F1, 7*F1....) cannot be suppressed as easily as ALL the "even" harmonics are with a SINGLE tapped (L1)/4 distributed structure shown in Figure 5. This is due to the fact that F1 is, in a broad sense, an "odd" harmonic (1*F) and conflicts with the requirement that F1 be band-passed while the remaining "odd" harmonics (F3, F5, F7.....) be band-rejected. Thus to achieve this design constraint each "odd" harmonic requires one unique shunt (L1)/4 distributed structure tapped progressively closer to the open end of the transmission line the higher the "odd" harmonic frequency.

Figure 6 shows these structures graphically depicted to the 7th harmonic:

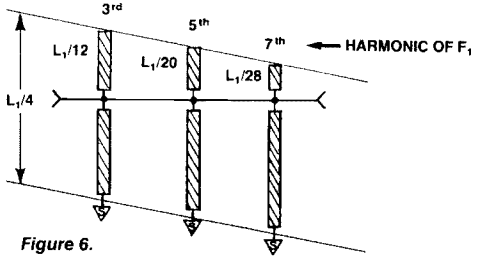


Figure 6.

The length of each of the "open" sections of the distributed structures must be L/4 (series resonance, Zoc = 0) at the desired "odd" harmonic frequencies. This open-stub length (Loc) translates to the fundamental wavelength (L1) using the following equation:

$$Loc = (L1)/(4*N) \qquad \text{(Eq.6)}$$

where: N = the "odd harmonic number (i.e. 3,5,7.....)

Combining the structure in Figure 5 with any or all of the tapped (L1)/4 structures in Figure 6 constitutes a filter that can be tailored to a prescribed harmonic suppression. The author used this technique to reduce the distortion in a 500 MHz SAW resonator oscillator. Only two (L1)/4 structures were required; the "even" one in Figure 5 and the 3rd harmonic "odd" one in Figure 6. A photograph of the transmission characteristics of this filter is shown in Figure 7.

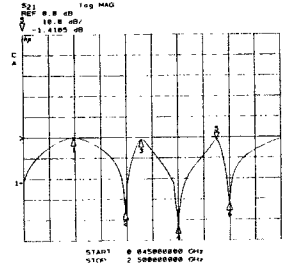


FIGURE 7.

Note the parallel resonance at the 500 MHz fundamental and the series resonance at the 2nd (1000 MHz), 3rd (1500 MHz), and 4th (2000 MHz) harmonics. Figure 8a shows the oscillator without the filter, and Figure 8b shows the oscillator with the filter. Thus, with a few shunt distributed elements, an effective yet

simple filter can be designed without complex synthesis and fabricated without tedious "tweaking" in manufacturing.

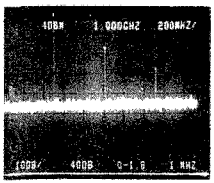


FIGURE 8a

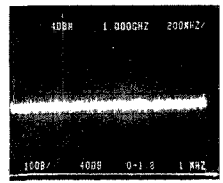


FIGURE 8b

From the filter response shown in Figure 7, it should be apparent that the harmonic attenuation (suppression) is finite (i.e. >30 dB), not infinite as predicted by Eq.2 or 3, where Zin = 0. Equations 2 and 3 are derived from Eq. 1 which assumed no loss (dissipationless line). Distributed quarter-wave (L/4) resonant lines have loss that can be calculated if the equivalent unloaded Q value is known.

The equation for the equivalent (lumped L/C) unloaded Q for an "open" L/4 resonant line can be derived by equating its derivative of impedance (with respect to angular frequency (2*Pi*F)) with the derivative of impedance of a lumped L/C series resonant circuit. The resultant of that mathematical computation divided by Rs (series resistance) yields:

$$Qu = (Pi/4)*(Zo/Rs) \qquad \text{(Eq.7)}$$

Eq.7 can be used to calculate Rs at any harmonic frequency (Fn) if Qu is known at Fn. The harmonic attenuation (An) at any Fn can be predicted by judicious use of the following equation:

$$An = Rs'/(Rs'+(Ro/2)) \qquad \text{(Eq.8)}$$

Where: Rs' = the equivalent series resistance of all the L/4 and multiple L/4 lines with series resistance at Fn.

Ro = Source and load resistance assumed equal (i.e. 50 ohms)

Applying a similar procedure as used to obtain Eq.8 an equation for insertion loss can be created as follows.

The equation for the equivalent (lumped L/C) unloaded Q for a "shorted" L/4 resonant line can be derived by equating its

derivative of susceptance (with respect to angular frequency) with the derivative of susceptance of a lumped L/C parallel resonant circuit. The resultant of that mathematical computation divided by G (parallel conductance) yields:

Qu = (Pi/4)*(Rp/Zo) (Eq.9)

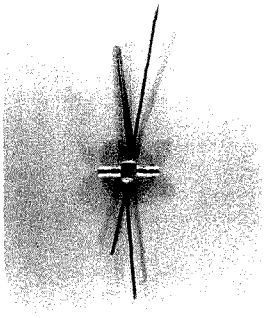
Where: Rp = 1/G = parallel resistance.

Eq.9 can be used to calculate Rp at the fundamental frequency (Fl) if Qu is known. The insertion loss (I.L.) can be predicted using the following equation:

I.L. = (Rp/m)/((Rp/m) + (Ro/2) (Eq.10)

Where: m = number of shunt (Ll)/4 resonators in the filter. (i.e. m=2 for the filter in Figure 7.)

The filter in Figure 7 was configured with .047 inch diameter semirigid coaxial cable with a dielectric constant Er = 2. Different transmission line media, whether coax, stripline, microstrip, etc. will have different Qu's. By configuring some (Ln)/4 "open" resonant lines in the desired transmission line media and making harmonic attenuation (An) measurements at each harmonic frequency (Fn), the unloaded Q's (Qu) can be calculated using Equations 7 and 8. Rs' reduces to Rs in a single (Ln)/4 resonant line. n = desired harmonic number (i.e. 1,2,3,4....).



World Radio History

RF-TECHNOLOGY FOR NMR IMAGING/SPECTROSCOPY

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INTRODUCTION:

Radio-Frequency (RF) technology has made an important contribution to the implementation of an exciting new medical diagnostics tool during the past couple of years: The NUCLEAR MAGNETIC RESONANCE IMAGING machine, which is able to look noninvasively inside the human body. This new technique alters the perspective of the radiologist and allows him to diagnose diseases with greater sensitivity. One of the main advantages of NMR images is their excellent soft tissue discrimination. NMR spectroscopy is now being evaluated for possible application to the non-invasive study of body chemistry. Many hospitals are in the process of installing such NMR imaging machines.

This paper reviews the NMR-system with emphasis not on the physics of the nuclear magnetic resonance effect but on the RF technology required to make it operate. Some special RF problems occurring in NMR will be discussed, especially the RF signal and kilowatt power processing.

PRINCIPLES OF NMR IMAGING:

The nuclei of certain atoms such as hydrogen and phosphorus possess both a magnetic moment and a spin angular momentum. When these nuclei are subjected to an external direct magnetic field, they align themselves in the direction of that field like compass needles. In addition, these nuclear micro-magnets are rotating or "spinning" like gyroscopes or tops with the so-called Larmor-frequency which is proportional to the magnetic field strength Bo. The proportionality factor is a physical constant, the gyromagnetic ratio, which differs greatly for various atoms. For hydrogen that ratio is 42.58 MHz/Tesla, and for phosphorus 17.23 MHz/Tesla. A magnet with a field strength of 15,000 Gauss or 1.5 Tesla operates therefore at a frequency of 63.87 MHz for hydrogen imaging. At the same field phosphorus nuclei can be detected at a frequency of 25.845 MHz. The relative sensitivity is fortunately very high for the diagnostically relevant hydrogen nucleus which is also available abundantly in the human body, mainly as part of the water and lipids (fat) in body tissue.

Magnetic resonance absorption occurs when radio frequency energy is applied at the Larmor frequency. The magnetic vector B1 of this RF field must be perpendicular to Bo, the static magnetic field, which aligns the spins and produces a macroscopic magnetic moment. B1 flips this magnetic moment vector by a certain angle depending on the magnitude and duration of the applied RF pulse. When the RF field is discontinued the transverse magnetization precesses around the axis of the external main Bo field. Hereby a RF signal is induced in the receiver coil located in the transverse plane. Spatial discrimination for the imaging process is obtained if one applies an additional, linearily varying magnetic field in the x, y and/or z-direction of a coordinate system

inside the magnet generating the main Bo field. These fields are produced by so-called gradient coils.(1,2).

THE NMR IMAGING SYSTEM:

A block diagram of a typical NMR imaging system is shown in Figure 1. At the left the computer related instruments are seen which carry out the image processing. Between the magnet at the right-hand side and the computer the necessary electronic components are indicated: spectrometer consisting of a transmitter and receiver, a multi-kilowatt RF power amplifier, noise suppression diodes, a transmitter/receiver switch, a kW matching network, low noise preamplifier, RF amplifier etc.

THE MAGNET:

The magnet has to be located inside a shielded room so that nearby radio stations do not interfere with the small NMR RF signals. The concept of superconductivity is commercially exploited on a large scale for the first time by most of these NMR magnets. Liquid helium at a temperature of about 4 degree Kelvin (-269 degree centigrade), imbedded in a tank of liquid nitrogen, cools the magnet coil wires so that they become superconductive. Their electrical resistance is zero and a DC current induced by a power supply once will continue to flow after the supply is disconnected generating a strong magnetic static field in the order of magnitude of 0.3 to 2.0 Tesla (3000-20000 Gauss). An important requirement for a whole-body magnet is that the magnetic field is highly homogeneous over a large volume to be imaged. Any inhomogeneity translates into a picture distortion. Therefore, all magnets have shimming coils in order to homogenize the field.They are fed by the shimming power supply. The trend to higher magnetic fields is dictated by the physics of the NMR experiment which says that the signal-to-noise ratio increases with increasing field strength.

An array of x,y and z gradient coils are mounted on a cylinder inside the magnet bore in which a whole-body or a head RF coil is also located. The gradient coil carrying cylinder is covered on its inside by a copper foil shield in order to generate a well-defined electrical environment for the RF coils and for the elimination of any interference between these coils. Resistive and permanent magnets are also used for NMR imaging, but only for lower field strength (0.15-0.3 Tesla). The former require 20 to 40 kilowatts of power and therefore costly cooling systems. (3).

GRADIENT POWER AMPLIFIERS:

In order to generate the gradient fields necessary for obtaining spatial resolution of the NMR signals DC pulse currents of 10-30 A must be injected into the gradient coils. They are delivered by the gradient PAs which are 1-2 kilowatt linear audio amplifiers with a frequency range of DC to 50 kHz. The magnetic forces on the gradient coil wires produce loud acoustic noise. Therefore, provisions for acoustic damping must be implemented. The philosophy behind the pulse trains used in different NMR experiments is a science for itself. After this short discussion of the apparatus generating the magnetic field environment necessary for NMR the RF signal path will be followed.

THE TRANSMITTER:

The pulse sequences necessary for the NMR experiment contain sinx/x or sinc-pulses which are used in order to excite a well-defined slice of the object to be imaged in such a way that the NMR signal is constant across that slice. These sinc-pulses require that the NMR transmitter as well as the RF power amplifier are linear. A block diagram of a NMR transmitter is given in Figure 2. It includes envelope feedback for linearity improvement. The NMR experiment requires the ability to change the phase of the carrier frequency in 90 degree steps which is accomplished by the multiplexer circuit shown.

A disadvantage of NMR imaging is the relatively long time required to take an image (several minutes) compared to x-ray tomography (seconds). The reason is that the nuclear spins in the samples have a relatively long relaxation time of several hundred milliseconds after excitation. One way to speed up the process is to image additional slices while waiting for the first ones to relax toward equilibrium. By applying a finite bandwidth RF pulse in the presence of a magnetic field gradient, a slice in a plane perpendicular to the gradient is excited. The modulating waveform required to produce an offset slice at a location Fl (frequency) of bandwidth Fo is a single-sideband signal which can be generated by the so-called Weaver method of SSB generation using a quadrature I-Q channel circuit arrangement. The modulating signals, generated by n-bit data words and converted to analog signals via DACs, are sine/cosine functions of the offset frequency Fl modulated by the sinc-function of the bandwidth Fo. They are applied at the corresponding PS-I and PS-Q ports of the SSB transmitter shown in the block diagram of the spectrometer in Figure 3.

THE RF POWER AMPLIFIER:

Most NMR imaging systems, especially at higher fields (1.5 Tesla), use tube power amplifiers because power levels of 5 to 15 kW are required for the excitation of the protons during whole-body imaging of heavy patients. These amplifiers are expensive, have a narrow bandwidth and require a change of the tubes after relatively short time intervals (1-2 years). Therefore, efforts are under way to replace them with solid-state amplifiers, a challenging task.

Typical pulse widths and duty cycles of NMR pulse sequences are in the range of 1-5 msec and 1-5 % respectively. Therefore, the average power levels stay relatively low. Transistor pulse amplifier design makes good use of the amazing ability of semiconductor devices to handle large power levels for short time intervals. For example a small PIN-diode in a glass package such as the Unitrode device UM-7201B has a power dissipation rating of 1.5 Watt in free air, but can handle a 20 kW pulse for 1 microsecond! Fortunately, a new technology has also arrived: The RF power MOSFET. Only this device was used because of its larger safe operating area and its higher input impedance compared to bipolar transistors.

Figure 4 shows the circuit diagram for a push-pull MOSFET power amplifier output stage for a 0.15 Tesla resistive magnet NMR system operating at 6.4 MHz. Transmission line BALUNs and 4:1 transformers have been used at input and output. With two low-cost MTM-15N45 MOSFETs (450 Volt, 15 A, 60 A peak) RF pulse power levels of 5-6 kW have been obtained in the 6 MHz frequency range with a power gain of 18 dB at 200 Vdc. In Figure 5 the output power as a function of the battery voltage is shown. These transistors (in a TO-3 can) produced still

2 kW at 13 MHz, the frequency of a 0.3 Tesla NMR system, and 1 kW at 22 MHz (0.5 T). The conclusion is that even MOSFETs designed for low-frequency applications such as switching type power supplies etc. are able to produce a lot of RF pulse power up to frequencies in the 20 MHz range.

The feasibility of kilowatt RF pulse generation for high field applications (20-85 MHz) was also explored. Figure 6 shows the circuit diagram of a 1.5-2 kW RF pulse power amplifier module using four MRF-150 MOSFETs. Combining four such modules with 4-way splitting and summing hybrids such as the one given in Figure 7 a 5-6 kW PA is obtained: PA-4. The output versus input power curve of Figure 8 demonstrates reasonably good linearity up to 4-5 kW at a frequency of 62 MHz. Figure 9 demonstrates a great advantage of transistor amplifiers compared to tube circuits; a much larger instantaneous bandwidth without retuning can be obtained. The 5-kW bandwidth extended from 40 to 70 MHz in this case. An interesting feature of the 4-way combiner hybrid of Figure 7 is the fact that the two input ports are operating in the push-pull mode providing all its known advantages. (Patent pending).

The number of components can be reduced drastically with the new Motorola RF power MOSFET MRF-154 which at present is expensive. A unique in-circuit combining technique was used in a 4-transistor amplifier: PA-1. Figure 10 shows the output power versus battery voltage curve demonstrating the generation of 5-6 kilowatt pulses at 62 MHz with only four transistors. This circuit delivered even 1 and 2 kW at voltages as low as 30 and 40 Vdc, a feature no tube circuit can perform. At each voltage the amplifier was driven into saturation. The same basic circuit produced 6-8 kW at lower frequencies (21 MHz, 12 MHz) with only minor changes in the input matching network and the drain-drain capacity. (Figure 11).

DIODE CIRCUITS:

High-gain wideband power amplifiers generate noise which disturbs the NMR experiment during the receiving time. In order to solve this problem the PAs are normally gated off after the end of the transmit pulse. In addition so-called noise suppression diodes can be inserted in the power cable connecting the PA to the NMR-coil. Diodes in both directions are put in parallel and series as shown in Figure 12. Their lead inductance has to be compensated by small capacitors parallel to input and output in order to avoid a power reflecting mismatch. As long as the noise voltages are less than the combined threshold voltages of these diodes the PA noise is suppressed.

If the NMR experiment is carried out in a single-coil system a transmitter/receiver T/R-switch is required. Such a circuit can be obtained by adding a parallel output connector to the arrangement of Figure 12. In order to handle the high power pulses one uses low on-resistance PIN diodes in combination with high-speed signal diodes. The third port of the T/R-switch is connected with a lambda/4 50-Ohm cable to the diode protection circuit necessary at the input of the low-noise preamplifier. This network simulates the cascade of two lambda/4 transmission lines with two CLC sections. (Figure 13). The input diodes are turned on at the beginning of a high-power RF pulse and their low impedance is then transformed into a very high impedance at the T/R-switch by the quarter wavelength transmission line. The same happens with the CLC sections.

NMR COILS:

The design of NMR coils is again a science in itself. The main problem to be solved is the generation of a very homogeneous RF magnetic B1-field orthogonal to the main direct Bo-field produced by the powerful superconductive magnet in a volume as large as necessary for whole-body imaging. Another problem occurs if one goes to higher field strengths in order to get better signal-to-noise ratios and therefore to higher frequencies where a more conventional design of a large whole-body coil becomes impossible due to self-resonance effects of the coil. The coils are normally forming a resonance circuit with some capacitors at the Larmor frequency (64 MHz for 1.5 Tesla) so that one obtains a well-defined real load impedance for the RF power amplifier after some impedance transformation. This impedance is usually 50 Ohm.

Since the dimensions of a whole-body or head coil are relatively large their inductance and therefore also their resonance impedance becomes very high too. This results in interference and detrimental coupling effects with the environment, especially the magnet and its many shimming and gradient coils. At high fields the self-resonance frequency of a coil may be even much lower than the NMR operating frequency. A solution to these problems has been found by splitting up the coil-wire in short pieces and connecting them with capacitors in such a way that each capacitor forms a series resonance circuit with its corresponding inductance piece. The conventional way to make an NMR transmit/receive antenna generating the orthogonal B1 field is to put a so-called saddle-coil pair with the associated capacitors on a plastic former which should have a low dissipation factor. A head coil has been made using this concept for carbon C-13 spectroscopy tuned to the Larmor frequency of 15.7 MHz. In order to enhance the very weak carbon signal the hydrogen protons are also excited. For this purpose a second saddle coil tuned to the frequency of 62.45 MHz was placed on the same former but mechanically shifted by 90 degrees so that its B1-field is orthogonal to that of the carbon coil. Figure 14 shows the circuit configuration of this double-coil and its matching networks. But saddle coils are not producing a magnetic field homogenity good enough for good imaging. More elaborate coil designs are described in the literature.(4).

The most important design parameter of a tuned NMR coil is its quality factor Q in the unloaded condition. It should be as high as possible, especially high compared to the loaded Q with a patient's body inside the coil. In other words, the coil losses should be determined by the unavoidable losses induced by the head or body to be imaged and not by those of the inductors and capacitors. The latter decrease drastically the signal-to-noise ratio of the NMR receiver system. Unloaded Q-factors of 300-600 have been obtained at low and high NMR frequencies. The ratio of unloaded to loaded Q is about 1.5 at 6.4 MHz and 4-6 at 64 MHz because induced body losses increase with frequency. The necessary high Q factors can be achieved by the selection of capacitors with very low dissipation factors. Teflon PC-boards have been used to implement successfully such capacitors which also must have a high breakdown voltage because RF pulses of many kilowatts are applied. Low-loss inductors are best implemented by 1/8" copper tubes. The signal-to-noise ratio can be improved drastically by using so-called surface coils for receiving the NMR-signal whereas the head or body coil is employed as transmitter for better B1-field homogenity. These surface coils are adaptively formed for different body parts and are located directly over the organ to be imaged, e.g. the eye, spine, knee etc.

Since the coil impedance is changing for different patients it is sometimes useful to place a matching network between power amplifier and coil. A LCL-circuit with a variable parallel capacitor and two stub-tuned series transmission line inductors was employed. It permits impedance matching over a large range. These RF circuits must be able to handle 1-15 kW pulses at 64 MHz. (Figure 15).

THE PREAMPLIFIER:

The NMR signals induced in the receive coils by the moving magnetic moment vectors are relatively small. Therefore low-noise preamplifiers are required which must be protected from the multi-kilowatt RF pulses by the protection circuits already discussed. Figure 16 shows a cascode circuit with two junction field-effect transistors at the input stage and a feedback damping arrangement for a low-field (0.12 Tesla, 5.1 MHz) NMR research system. The optimum source impedance was about 800 Ohm. This preamplifier was connected directly to the receive coil of a 2-coil T/R arrangement. The input impedance of the antenna was tuned to 800 Ohm. The noise figure as a function of the source resistance is shown in Figure 17 and as a function of the source admittance phase angle in Figure 18. A noise figure of 0.5-0.6 dB was obtained as minimum. The concept of feedback damping which was applied reduces the input impedance of the preamplifier so that the coil bandwidth is increased without increasing the noise considerably. This feature is not required at high fields where the body damping is much more pronounced.

The noise figure measurements have been carried out with the low-cost liquid-nitrogen method which is suprisingly accurate and permits measurements at source resistances different from 50 Ohm. The receiver output noise voltage is measured for the source resistor at room and then at liquid N2 temperature (77 degree K). The noise voltage ratio can be related directly to noise figure in dB with the curve of Figure 20. (Courtesy Dr.H.Hart, GE-CRD). This method has also the advantage that it can easily be applied to a whole system as well as for source resistances differing from 50 Ohm. For high-field systems preamplifiers with bipolar transistors have been designed in order to obtain a larger bandwidth. The design starts with the selection of a low-noise transistor which must have very high current gain, a large gain-bandwidth product and a low base bulk resistance. The optimum source resistance, the most important design parameter, can easily be determined by measuring with a receiver the relative output noise voltage for the conditions of short- and open- circuit at the preamplifier input. The ratio of the two noise voltages (short- over open-circuit voltage) multiplied with the input impedance of the input stage gives the optimum source impedance. In the frequency range of interest that impedance was about 100 Ohm. A noise matching network which degrades the noise figure can be avoided by paralleling two input transistors. This has also the beneficial effect of reducing the base resistance. A preamplifier designed with this procedure has a noise figure over a large frequency range of well below 1.0 dB and reaching 0.5 dB at some frequencies. Figure 19. (6,7).

NMR RECEIVER:

The preamplifier which may have a bandpass filter at its input in order to increase system stability is followed in the signal path by a variable gain

RF amplifier made with a Plessey IC SL-1550. It has a gain range of 10 to 36 dB. A block diagram of the receiver itself is shown in Figure 21. It uses the ZERO-IF I-Q channel quadrature detection concept due to the fact that the complex analog NMR signals have to be converted to the digital format by two A/D converters in order to permit image reconstruction by a computer. High frequency A/D converters are not available, certainly not at a low cost.

The RF-amplifier signal is split and fed to two quadrature mixers. Their low-frequency output signal are band-limited after amplification by two low-pass filters which have a variable bandwidth. (8,16,32 kHz). The main design challenge is the front-end mixer pair which must provide a large dynamic range as well as good linearity. The maximum overall gain of the receiver is about 70 dB.

QUADRATURE EXCITATION AND RECEPTION:

Normally the B1 RF-field in the transmit head or body coil is linearily polarized. Due to the fact that the human body is electrically conducting eddy currents are generated inside the body parts which increase with frequencies. These unwanted eddy currents cause image artifacts and distortions. Their detrimental influence can be eliminated or drastically reduced by producing a rotating RF B1-field. This is done by feeding a specially designed circular RF coil on two points wich are geometrically 90 degrees apart by two equal, but 90 degrees phase-shifted signals.(5). A linearly polarized field can be generated by the superposition of two rotating fields. One of these is now interacting with the magnetic moments and spins of the protons according to the physics of the NMR experiment. Therefore, only half the RF power is required using a rotating field compared to the case of a linear one. Figure 22 shows an RF block diagram of such a system with two power amplifiers. If only one big tube PA is available one can use a quadrature power splitter made with two lambda/8 50 Ohm transmission lines and two crosscoupling capacitors which must have a reactance of 50 Ohm at the operating frequency. The quadrature coil arrangement can also be used to increase the signal- to-noise ratio by a factor of 1.4 during the receive mode of operation. (5).

RESULTS:

The results obtained by such a NMR system with its many RF circuits are images of the inside of the human body in all possible cross-sections with a discrimination not available with other means.

ACKNOWLEDGEMENT:

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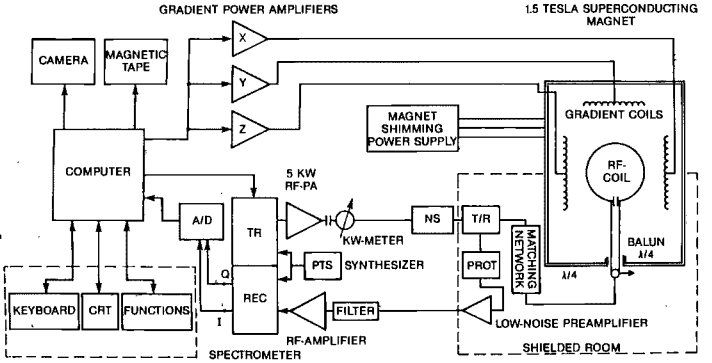
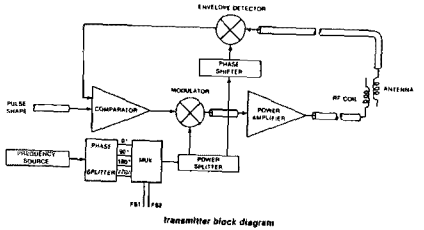


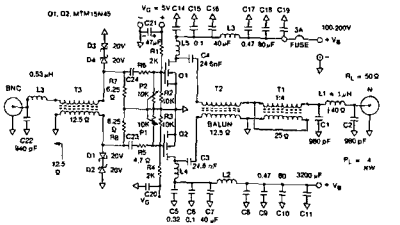
WHOLE-BODY MAGNETIC RESONANCE (MR) IMAGING/SPECTROSCOPY SYSTEM

FIGURE 1



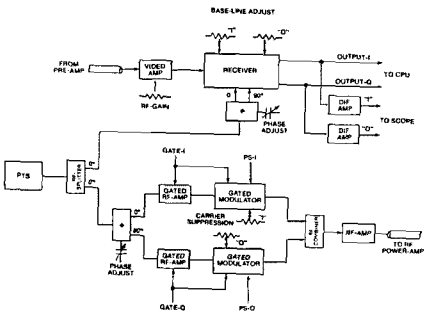
transmitter block diagram

FIGURE 2



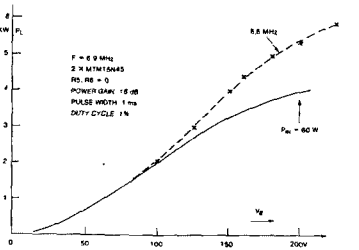
4 KW NMR RF POWER AMPLIFIER: 6.4 MHz (0.15 T)

FIGURE 4



SPECTROMETER BLOCK DIAGRAM FOR MULTISECTION MR IMAGING

FIGURE 3



NMR RF PULSE POWER VS BATTERY VOLTAGE

FIGURE 5

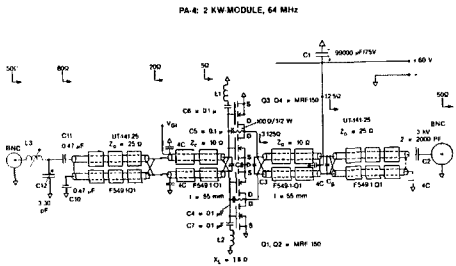
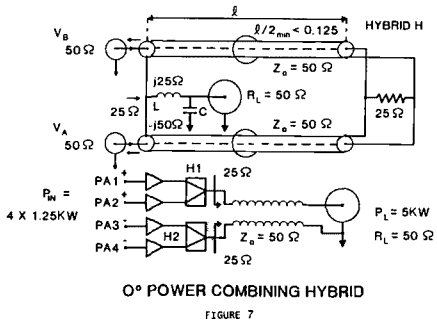
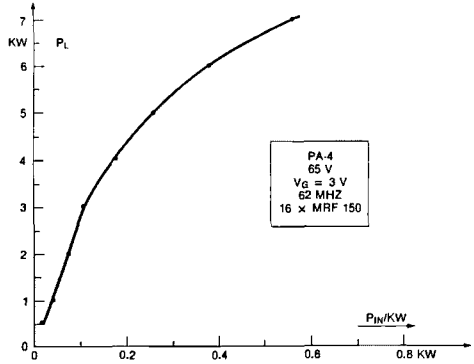


FIGURE 6



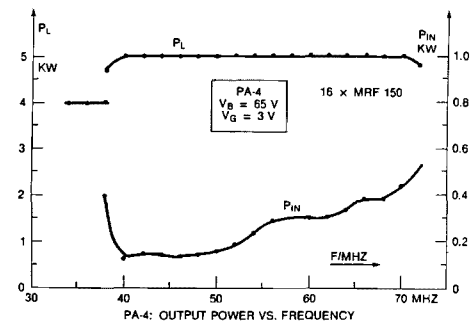
O° POWER COMBINING HYBRID

FIGURE 7



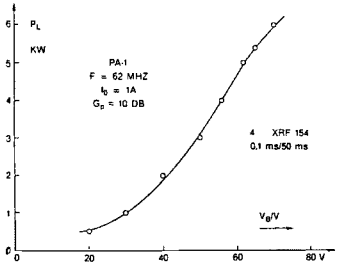
PA-4: OUTPUT VS. DRIVE POWER P_{IN}

FIGURE 8



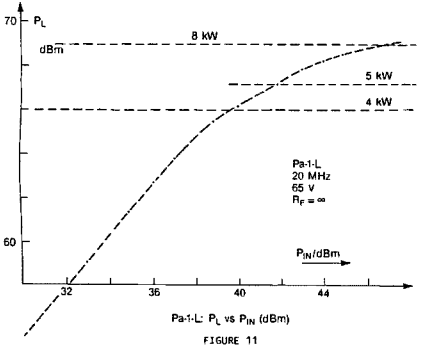
PA-4: OUTPUT POWER VS. FREQUENCY

FIGURE 9



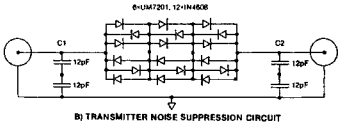
PA-1: OUTPUT POWER VS SUPPLY VOLTAGE (DC)

FIGURE 10



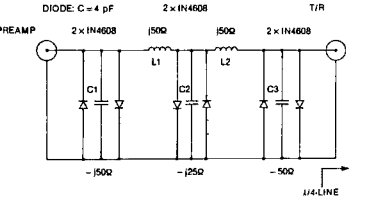
Pa-1-L: P_L vs P_{IN} (dBm)

FIGURE 11



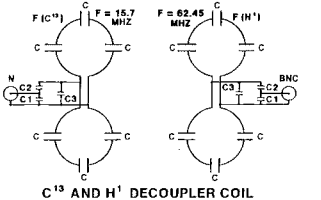
B) TRANSMITTER NOISE SUPPRESSION CIRCUIT

FIGURE 12



PREAMPLIFIER PROTECTION CIRCUIT

FIGURE 13



C^{13} AND H^1 DECOUPLER COIL

FIGURE 14

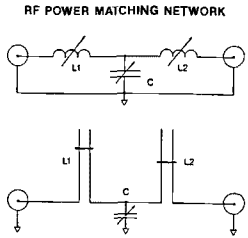


FIGURE 15: POWER MATCHING NETWORK

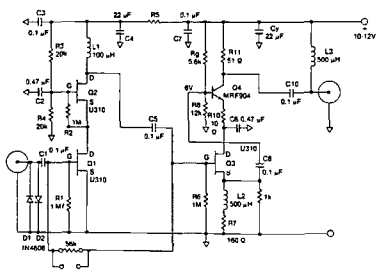
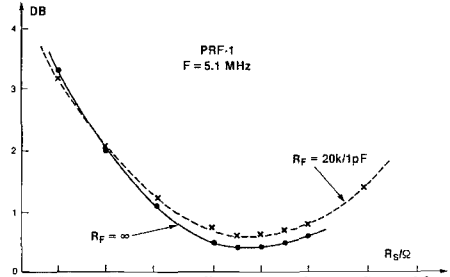
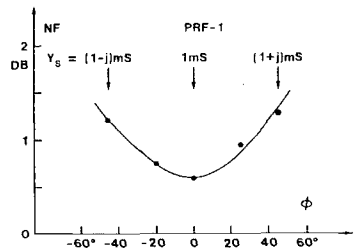


FIGURE 16



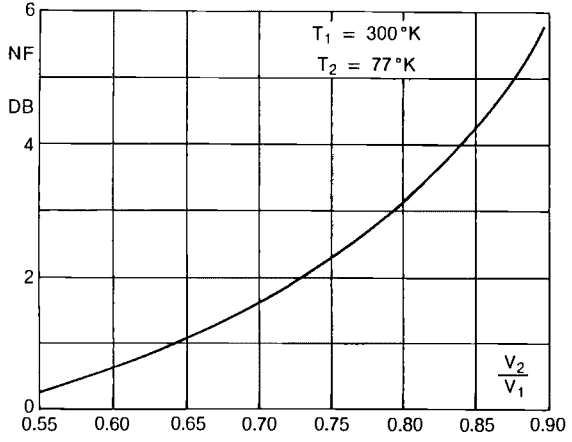
NOISE FIGURE VS SOURCE RESISTOR

FIGURE 17



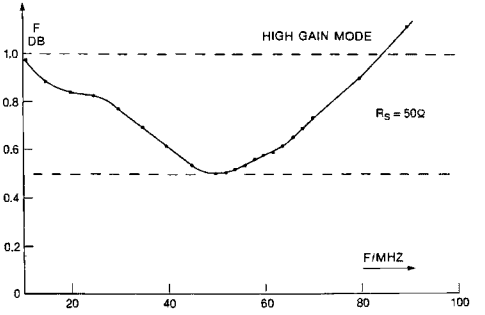
NOISE FIGURE AS A FUNCTION OF THE SOURCE ADMITTANCE PHASE ANGLE

FIGURE 18



LIQUID NITROGEN METHOD:
NOISE FIGURE AS A FUNCTION OF THE
NOISE VOLTAGE RATIO V_2/V_1.

FIGURE 20



LNA-V-1: NOISE FIGURE F VS FREQUENCY

FIGURE 19

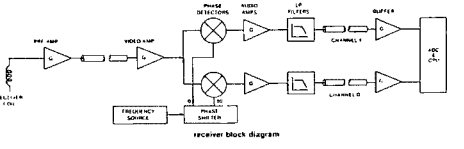
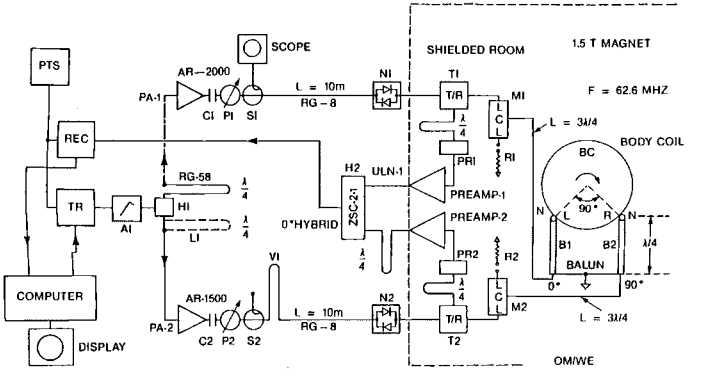


FIGURE 21: RECEIVER CIRCUIT FOR NMR



1.5 TESLA NMR IMAGING SYSTEM WITH QUADRATURE EXCITATION/RECEIVING

FIGURE 22

THE Q FACTOR OF MICROSTRIP MATCHING NETWORK IN RF CLASS C AMPLIFIER DESIGN

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ABSTRACT

The Q factor of an impedance matching network incorporating microstrips as inductances has a bounded value. This paper shows how strip lengths as a function of Q are evaluated numerically with greater accuracy compared to using graphical construction on a Smith chart. An example of a 162 MHz 100-watt class C amplifier is also given.

INTRODUCTION

Microstrip has long been associated with microwave passive or active circuit design since at such frequencies a certain length of strip can be made to behave as a capacitance or inductance according to its physical dimension with respect to the electrical wavelength (λ). When designed as a transmission line, it can also be used for impedance transformation or matching between an active device and its source and load impedances.

The expressions relating impedance variation along a line terminated by a load other than Z_0, its characteristic impedance are rather simple. But their numerical evaluation requires complex hyperbolic or circular function manipulations which are still performed graphically.

Now that pocket computers incorporated with high level programming facilities such as the BASIC Language are available, the time has come for every circuit designer to do the calculations by machine with greater accuracy and less time consuming effort.

In RF Class C power power amplifier design, one often encounters low input and output transistor impedances. The simple method using 2-element L, C components to match them to the 50 Ω source and load impedances results in poor harmonic rejection and power efficiency (Fig. 1a). General practice consists of increasing the Q of the matching network by adding an inductance in series with the transistor's input/output impedances as shown in Fig. 1b.

In high frequency operation, the required inductance is rather small and its precise value becomes difficult to achieve using a conventional coil. For this reason, most practical VHF, UHF amplifiers adopt microstrip to replace this lumped constant.

In the literature[1-4], the designers often choose a certain length of strip and then try to match the transistor to the source or load with the

aid of the Smith chart. This method is rather empirical and the Q of the network is either undefined or cannot be determined accurately. The following shows how the quality factor is related to the circuit parameters as well as strip lengths in a practical design.

DESIGN PROCEDURE

With reference to Fig. 1c, let the microstrip of length ℓ and characteristic impedance Z_O replace the lumped constant of reactance X_L of Fig. 1b. From the general low loss line equation, the normalized input impedance of the microstrip is :

$$z_{in} = \frac{z_T + j\tau}{1 + jz_T\tau} = r_{in} + jx_{in} \qquad (1)$$

where $\tau = \tan\beta\ell$, $\beta = 2\pi/\lambda$ and $z_T = (R_T + jX_T) / Z_O$

$= r + jx$

By definition,

$Q = x_{in} / r_{in}$.

We can then deduce the strip length as a function of x, r and Q, giving

$$\ell = \frac{1}{\beta} \arctan \frac{(1 - x^2 - r^2) \pm [(1 - x^2 - r^2)^2 - 4(Q^2 r^2 - x^2)]^{1/2}}{2\,(rQ + x)} \qquad (2)$$

Since ℓ is real, the expression under the square root must be positive, leading to the relation :

$$Q^2 < [(r - 1)^2 + x^2]\,[(r + 1)^2 + x^2] / 4r^2 \qquad (3)$$

or $$Q^2_{max} = [(r - 1)^2 + x^2]\,[(r + 1)^2 + x^2] / 4r^2 \qquad (4)$$

From the above expression it can be seen that the Q of a network using transmission lines as inductances has an upper bounded value. In practice, the input and output networks of a Class C power amplifier require a Q of the order of 10. This condition can generally be met without any difficulty.

AMPLIFIER DESIGN

The following example is taken from the design of a 100 Watt Class C amplifier operating at 162 MHz for ^{31}P NMR in-vivo imaging experiments. The power transistor MRF 317 has the following impedances at the rated output power :

$Z_T = 0.77 + j\ 1.4\ \Omega$ (Input)

$Z_T = 1.77 - j\ 1.0\ \Omega$ (output)

By choosing strip widths equal to that of the transistor base and collector leads, respectively 5.2 mm and 3.955 mm, and using a copper clad Teflon glass PC board with the following characteristics :

Dielectric constant $\varepsilon_r = 2.55$

substrate thickness $h = 1.52$ mm and

Copper thickness $t = 35\ \mu$

Z_O was first calculated as a function of the strip widths[6,7] then strip lengths vs Q as determined by relatin (2) were tabulated as shown in Tables I and II. For our amplifier, choosing Q = 13 for both the input and output networks led to strip lengths of 4.2 and 11.4 cm, respectively. The latter were etched on a PC board which was designed to accommodate the power transistor as well as the matching capacitors[8] [Fig. 2].

RESULTS AND DISCUSSION

The Class C amplifier constructed has a power gain of 10dB at 100 watts output and about 7 dB at 127 watts. The measured 3 dB bandwidth ΔF was 8.0 MHz, which is in very good agreement with the theoretical value of 8.1 MHz evaluated from the formula

$$\Delta F = F\ (\sqrt{2} - 1)^{1/2}\ /Q^{(9)}$$

where F is the operating frequency. The second solution for the strip length (ℓ_2) was discarded due to its impractical dimension. One means of reducing the required strip length consists in increasing Z_O, which implies the reduction of the strip width. As an example, halving the ouptput strip width leads to a required strip length of only 6.8 cm instead of the actual 11.4 cm. This can be achieved in detriment to the current handling capacity of the strip.

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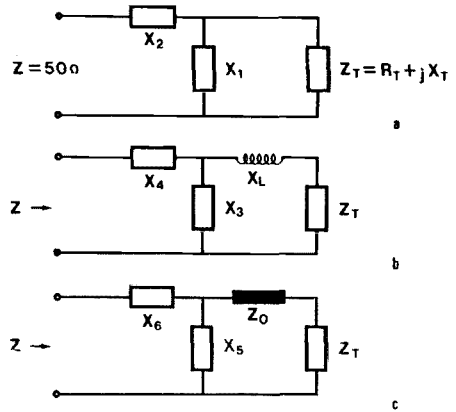


Figure 1. Basic network using X_1, X_2 to match the input/output impedance Z_T of a transistor to 50 Ω (a). Matching network incorporating an inductance to reduce harmonic frequencies (b). Inductance replaced by a microstripline with a well defined Q at high frequencies.

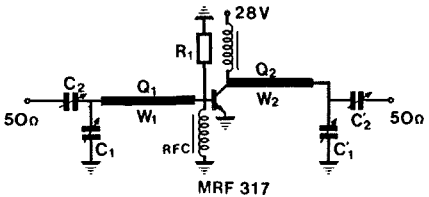


Figure 2. Typical Class C amplifier incorporating microstripline in the input and output matching network. Matching capacitors C are functions of the chosen Q of the network as tabulated in Tables I and II. R_1 (18 Ω) was inserted to improve transient response. It can be omitted for CW operation.

Q	ℓ_1(cm)	C_1(pF)	C_2(pF)	R_{in}	X_{in}
28_{max}	15.2	18.8	4.1	1.53	43.30
20	7.3	47.5	7.9	0.90	18.05
13	4.2	82.7	14.8	0.81	10.59
10	3.0	112.8	25.2	0.79	7.95
	ℓ_2(cm)				
20	23.1	6.4	3.1	5.2	103.7
13	26.2	2.7	2.9	13.6	176.1
10	27.4	1.3	2.9	23.4	233.8

Table I. Transistor Base Lead Width = 5.2 mm, Z_0 = 43 Ω

Q	ℓ_1(cm)	C_1(pF)	C_2(pF)	R_{in}	X_{in}
15_{max}	16.4	14.0	5.2	3.53	52
13	11.4	24.8	7.3	2.4	31.3
12	10.1	29.2	8.4	2.2	26.9
10	8.0	39.2	11.1	2.0	20.0
		ℓ_2(cm)			
13	21.3	7.3	4.2	6.6	86.3
12	22.6	5.8	4.1	8.4	100.4
10	24.7	3.6	3.9	13.2	131.8

Table II. Transistor Base Lead Width = 3.935 mm, Z_0 = 57 Ω

CAPTION. Tables I and II

Microstrip lengths (ℓ_1, ℓ_2) as a function of Q. R_{in} and X_{in} are the real and imaginary parts of the line input impedance. For Q less than Q_{max}, there existe two values of ℓ, R_{in} and X_{in}. C_1 and C_2 are the corresponding matching capacitances required to match R_{in} and X_{in} to the 50 Ω source or load impedance.

SORF - AN RF LOW POWER SMD ALTERNATIVE PACKAGE

A Paper for RF Technology Expo 86
by
Harry J. Swanson
Motorola Semiconductors

INTRODUCTION

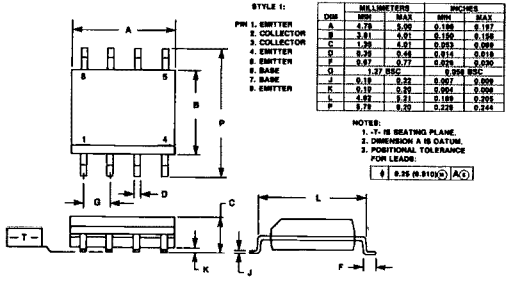
This paper introduces the SORF$_{TM}$ (Small Outline RF) package which has the same mechanical case outline as the familiar SOIC SO8 (see Figure 1). In this paper the SORF package is described and its performance is compared to the Macro-X $_{TM}$ package. Thermal performance is presented emphasizing the performance in a still air 25^{0} C ambient environment. Specific characteristics of the SORF package are discussed. These outstanding package characteristics offer the RF design engineer an alternative to the conventional RF packages (such as the TO39, TO-92, SOT89 and Macro-X) and provide a true SMT package for RF low power transistors.

PACKAGE DESCRIPTION

The SORF transistor is composed of the leadframe, the transistor die, the interconnect wires and the epoxy molded body (see Figure 2). The SORF leadframe is copper and it is designed to provide an excellent RF package. In order to enhance the RF gain and broadband performance, the corner leads are internally connected through the leadframe to provide low common lead inductance and to reduce package parasitics. On one side of the package the two middle leads are the input leads and on the opposite side the two middle leads are the output leads which extend to the collector pad of the leadframe where the transistor die is mounted by forming a gold-silicon eutectic die bond. The die is connected to the base and emitter leads using 1.5 mils diameter gold wire.

Symmetry of the layout allows for parallel wirebonding and for equal length base and emitter wires. To enhance the RF performance the wire loop lengths and loop heights are minimized. The leadframe strip is then epoxy molded to fully encapsulate each individual leadframe on the strip. After the mold process, the leadframe is tin plated. Next, the individual RF transistors are trimmed from the leadframe strip and the leads are formed in the gull wing format. Figure 1 details the SORF package dimensions and mechanical tolerances.

SORF and Macro-X are trademarks of Motorola, Inc.



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	4.78	5.00	0.188	0.197
B	3.81	4.01	0.150	0.158
C	1.35	1.01	0.053	0.089
D	0.36	0.46	0.014	0.018
F	0.67	0.77	0.026	0.030
G	1.27 BSC		0.050 BSC	
J	0.10	0.22	0.007	0.009
K	0.19	0.30	0.004	0.008
L	4.82	5.21	0.189	0.205
P	5.79	6.00	0.228	0.244

FIGURE 1 - SORF CASE OUTLINE DRAWING

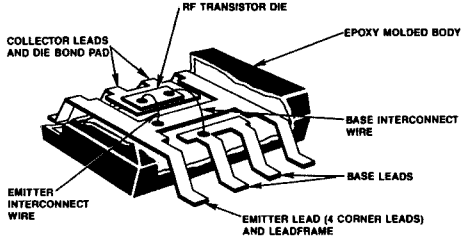


FIGURE 2 - CUTAWAY VIEW OF THE SORF TRANSISTOR

RECENT SORF INTRODUCTIONS

Two RF transistors introduced in 1Q86 are (1) the MRF8372, a 750 mW, 12.5 Vdc, 10 dB gain UHF/800 MHz Class C predriver amplifier and (2) the MRF5812, a 10 Vdc V_{CE}, 50mA I_C, 15 dB G_{NF}(typical), 2.0 dB NF(typical), 500MHz Class A low noise amplifier. These transistors' counterparts in the Macro-X are, respectively, the MRF837 and the MRF581. Table I compares the two transistors' performances in the SORF and the Macro-X packages. Note that the SORF package offers comparable performance to its Macro-X counterpart.

TABLE I - COMPARISON OF THE SORF TO THE MACRO-X

MRF8372 (SORF) VS MRF837 (MACRO-X)						
POWER DISSIPATION MRF8372 @ T_C = 75°C, DERATE ABOVE 75°C MRF837 @ TC = 50°C, DERATE ABOVE 50°C		Pout (f = 870 MHz, V_{CC} = 12.5 Vdc)	Opemin	Gpetyp	Ncmin	Nctyp
	WATTS	mW	dB	dB	%	%
MRF8372	1.5	750	8.0	10	50	60
MRF837	2.5	750	8.0	10	50	60

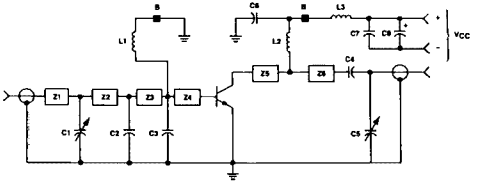
MRF5812 (SORF) VS MRF581 (MACRO-X)					
POWER DISSIPATION MRF5812 @ T_C = 75°C, DERATE ABOVE 75°C MRF581 @ TC = 50°C, DERATE ABOVE 50°C		Fl (f=500 MHz, V_{CE}=10 Vdc, I_C=50mA)	G_{NF}min	G_{NF}typ	NF max	NF typ
	WATTS	GHz	dB	dB	dB	dB
MRF5812	1.5	8.0	13	16	3.0	1.9
MRF581	2.5	5.0	13	16	3.0	1.9

MRF5812

The MRF5812 is fully characterized in a manner similar to the MRF581. The Transistor is RF guaranteed for 13 dB GNFmin (minimum gain at noise figure) and 3.0 dB NFmax (maximum noise figure) at 500 MHz. The transistor is characterized for S parameters and noise figure versus frequency and noise figure versus I_C (collector current). Typical noise figure performance and typical S parameters are listed in the transistor data sheet. These parameters are almost identical to the those of the MRF581.

MRF8372

The MRF8372 is tested to guaranteed RF performance at 870 MHz for 750 mW Pout (power output), 8 dB Gpe (common emitter power gain), and 50% Nc (collector efficiency) in a fixed tuned broadband test fixture which is pictured in the data sheet (see Figure 3 for the corresponding circuit schematic). Typical RF performance in the broadband test fixture is plotted in Figure 4. The test fixture demonstrates the ability to use the transistor in broadband applications with excellent performance. The MRF8372 is fully characterized in a manner similar to the MRF837 for typical performance and device impedance in the 800 MHz band (see Table II). Input and output impedance parameters show excellent low Q which enhances the ability to match the device for broadband operation.



C1, C5 — 0.8-9.0 pF JOHANSON GIGATRIM
C2, C3 — 16 pF CERAMIC CHIP CAPACITOR
C6 — 91 pF CLAMPED MICA, MINI-UNDERWOOD
C4 — 47 pF CERAMIC CHIP CAPACITOR
C7 — 91 pF CLAMPED MICA, MINI-UNDERWOOD
C8 — 1.8 μF 25 V TANTALUM
B — BEAD, FERROCUBE 56-590-65/3B

L1, L2 — 4 TURNS, #21 AWG, 5/32" ID
L3 — 7 TURNS, #21 AWG, 5/32" ID
Z1, Z3 — 1.0" x 0.079" MICROSTRIP, Z_0 = 50 Ohms
Z2 — 0.25" x 0.079" MICROSTRIP, Z_0 = 50 Ohms
Z4 — 0.15" x 0.079" MICROSTRIP, Z_0 = 50 Ohms
Z5 — 0.30" x 0.079" MICROSTRIP, Z_0 = 50 Ohms
Z6 — 1.63" x 0.079" MICROSTRIP, Z_0 = 50 Ohms
PCB — 1/32" GLASS TEFLON, ϵ_r = 2.56

FIGURE 3 - 800/900 MHz BROADBAND CIRCUIT SCHEMATIC

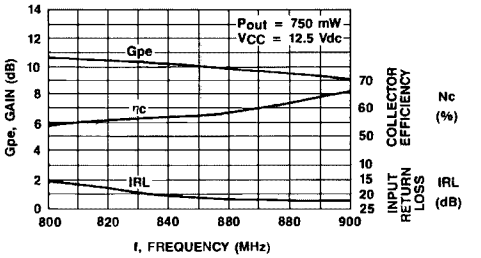


FIGURE 4 - 800/900 MHz BROADBAND PERFORMANCE

TABLE II - Z_{IN} AND Z_{OL} VERSUS COLLECTOR VOLTAGE, INPUT POWER AND OUTPUT POWER

f FREQUENCY MHz	Z_{in} OHMS		Z_{OL}* OHMS	
	V_{CC} = 7.5 V	V_{CC} = 12.5 V	V_{CC} = 7.5 V	V_{CC} = 12.5 V
	P_{in} = 150 mW	P_{in} = 100 mW	P_{out} 806 MHz = 820 mW P_{out} 870 MHZ = 635 mW P_{out} 960 MHz = 530 mW	P_{out} MM MHz = 1.05 W P_{out} 870 MHz = 955 mW P_{out} 960 MHz = 580 mW
806	8.0 + j1.9	4.0 + j1.2	24.7 - j19.2	20.9 - j31.0
870	5.2 + j3.5	6.0 + j1.9	36.9 - j20.5	32.1 - j28.9
960	6.8 + j4.0	6.1 + j2.5	39.3 - j18.5	96.3 - j25.7

*Z_{OL} = CONJUGATE OF THE OPTIMUM LOAD IMPEDANCE INTO WHICH THE DEVICE OUTPUT OPERATES AT A GIVEN OUTPUT POWER, VOLTAGE, AND FREQUENCY.

SORF THERMAL PERFORMANCE

The SORF package offers excellent thermal performance. Thermal analysis determined that the thermal resistance of the SORF package is almost as low as that of the Macro-X package. The IR scans are performed under RF operating conditions and mounted in a manner similar to a surface mount application in which a heatsink is not employed and no considerations are made to provide a good case to heatsink interface. The transistor sustains up to 1.5 watts P_D, power dissipation which raises the T_J, die junction temperature to 150 °C at T_A = 25 °C.

Summary of IR Scan Analysis

Table III shows that the Θ_{JL} ranges from 43.4 to 47.1 °C/W and Θ_{JA} ranges from 82.8 to 87.7 °C/W at P_D ~ 1.5 watts, T_L = 80 °C, and T_A = 25 °C.

TABLE III - SUMMARY OF SORF IR SCAN ANALYSIS

IR SCAN DESCRIPTION	FREQUENCY = 870 MHz; SEE RF FUNCTIONAL CIRCUIT SCHEMATIC												
	POUT	PIN	VCC	IC	PD	TJ HS	TJ AV	TL	TA	θJL HS	θJL AV	θJA HS	θJA AV
	W	mW	Vdc	mA	W	°C	°C	°C	°C	°C/W	°C/W	°C/W	°C/W
SCAN #2 BIAS COND. 3	1.1	405	15	135	1.33	142	139.7	77	25	48.9	47.1	88	86.2
SCAN #2 BIAS COND. 4	1.18	460	15	146	1.47	153.5	150.8	82	25	48.6	48.8	87.4	85.6
SCAN #3 BIAS COND. 2	1.11	415	15	135	1.33	144	141.7	84	25	45.1	43.4	99.5	87.7
SCAN #4 BIAS COND. 1	1.14	410	15	142	1.4	147	145.3	83	25	45.7	45.2	87.1	86.8
SCAN #5 BIAS COND. 1	1.13	415	15	142	1.42	142	141.5	80	24	43.7	43.4	83.1	82.8

The following thermal resistances can be justified for the SORF transistor:

Θ_{JL} = 45 °C/W at T_L = 80 °C

Θ_{JA} = 85 °C/W at T_A = 25 °C

where P_D = 1.5 watts and T_J = 150 °C.

Power derating curves are shown for Θ_{JL} and Θ_{JA}, respectively (see Figures 5 and 6).

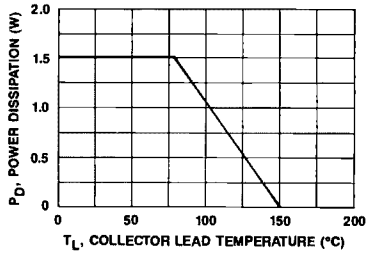


FIGURE 5 - POWER DERATING, θ_{JL}

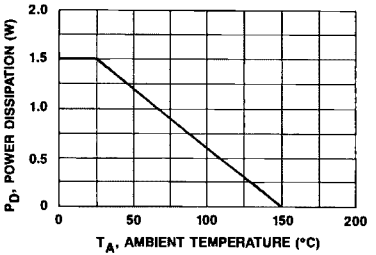


FIGURE 6 - POWER DERATING, θ_{JA}

IR Scan Setup

The IR scan setup consisted of the following:

1. Radiometric Microscope Model RM-2A, Barnes Engineering,
2. Regulated Power Supply Model LK 342A FM,
3. Voltmeters and Current Meters to monitor bias conditions,
4. Doric Trendicator 400 Type J/°C,
5. RF Functional System (see Figure 7).

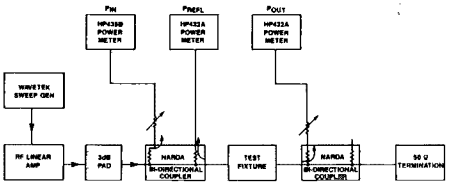
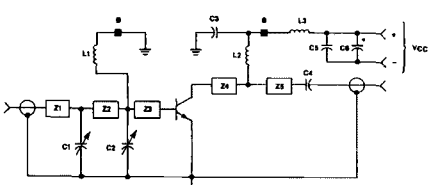


FIGURE 7 - RF FUNCTIONAL TEST SYSTEM BLOCK DIAGRAM

Preparation of Samples for IR Scan

The devices are decapsulated using a Jet Etch machine. Details on this machine can be found in AN938 (Motorola, Inc. Application Note). The epoxy mold is removed to expose the surface of the transistor die while the wires and package leads are kept intact and not disturbed. The package is soldered into the RF functional circuit. The circuit schematic and parts list are shown in Figure 8. The circuit employs a 2 inch x 2 inch piece of 31 mil Glass Teflon$_{TM}$ printed circuit board. The samples are mounted to the PC board as a surface mounted component. In other words, no heat sink is used and the board is subject to free air heat transfer.



C1, C2 — 0.8 - 8.0 pF JOHANSON GIGATRIM
C3 — 91 pF CLAMPED MICA, MINI-UNDERWOOD
C4 — 1000 pF CERAMIC CHIP CAPACITOR
C5 — 68 pF CLAMPED MICA, MINI-UNDERWOOD
C6 — 1.0 μF 25 V TANTALUM
B — BEAD, FERROXCUBE 56-590-65/3B
L1, L2 — 4 TURNS, #21 AWG, 5/32" ID
L3 — 7 TURNS, #21 AWG, 5/32" ID
Z1 — 0.3" x 0.079" MICROSTRIP, Z_0 = 50 Ω
Z2 — 0.47" x 0.079" MICROSTRIP, Z_0 = 50 Ω
Z3, Z4 — 0.2" x 0.079" MICROSTRIP, Z_0 = 50 Ω
Z5 — 0.5" x 0.079" MICROSTRIP, Z_0 = 50 Ω
PCB — 1/32" GLASS TEFLON, ϵ_r = 2.56

FIGURE 8 - IR SCAN 870 MHz CIRCUIT SCHEMATIC

Glass Teflon is a trademark of Dupont Corporation.

The collector leads are painted with flat black paint to provide a good emissivity surface. A reference line is marked on the collector leads to indicate the place where they contact the PC board on the collector microstrip line. The ability to identify this reference point is essential in acquiring accurate and consistent T_L data.

Measurement Techniques

The measurement techniques and considerations are outlined below:

T_L is measured at a point on the collector lead where it first contacts the printed circuit board closest to the package. The T_J measurements are made at three points on the active area of the die. $T_{J\,AV}$, die junction temperature average and $T_{J\,HS}$, die junction temperature hot spot are recorded in Table III. In all cases, the temperatures across the die active area are uniform (i.e. no significant hot spotting was found which indicates good die bonds and proper RF operation of the die in the SORF package). The total power dissipation of the device under steady state operating conditions is defined in the equation below:

$$P_D = P_{IN} + (V_{CC})(I_C) - P_{OUT}$$

The input return loss is greater than 20 dB; thus, it is omitted from the power dissipation equation. The data for the above parameters is in Table III. The thermal scans were done in free air or, in other words, with no forced air over the part and the printed circuit board.

Conclusions

The data demonstrates that the SORF package has nearly equivalent thermal performance to the Macro-X package. The surface mounted technique utilized in this thermal analysis makes convection and radiation the predominant heat transfer mechanisms. In a more comprehensive thermal study of surface mounted techniques, it would be desirable to evaluate the effects of air flow on the heat transfer mechanisms of convection and radiation. In a further study it would be beneficial to also evaluate the heat transfer mechanism of conductivity via a good case to heatsink interface at the collector leads.

Characteristics of the SORF Package

The preceding discussion has demonstrated that the SORF package has excellent RF properties and is a proven surface mount component (SMC) with power dissipation capability of 1.5 watts. When RF performance and a SMC is mandatory, the SORF package offers an excellent alternative to the Macro-X, TO-39, TO-92 and the TO-89.

In Table IV the RF and thermal characteristics and other noteworthy characteristics are summarized. The SORF package offers other specific characteristics which provide a more versatile package. Allowing for a maximum die size of 40 mils x 60 mils the SORF package can accomodate die that fit only in other larger and more conventional non-SM packages. This will provide the RF design engineer with an RF SMD to utilize in new designs or to upgrade to SMT in older designs.

In addition , the SORF package has an additional leadframe style in which the collector and the base pads are split; thus, it provides a package in which there are isolated collector and base pinouts. This modification of the SORF leadframe makes it feasible to assemble more than one transistor die in the same package. With an eight pin leadframe layout various applications are possible such as, complementary push-pull, push-pull (using separate but similar geometries), differential and cascade -cascode amplifiers.

TABLE IV - SORF PACKAGE CHARACTERISTICS

Excellent RF Properties:
Low Common Lead Inductance and Package Parasitics
Symmetrical Leadframe Layout
Copper Leadframe for Excellent Conductivity
Excellent Thermal Properties:
Copper Leadframe for excellent Thermal Conductivity
Symmetrical Leadframe Layout
Large Collector Pad
Relativity Large Package Molded Periphery Around the Collector Pad
Accomodate Large Transistor Die that Fit in Other Larger Conventional Packages
Wide Common Lead Bridge for MOS Input Matching Capacitor
Modified Leadframe Available with Split Collector and Base Pads for Special Applications Utilizing Multiple Die

Another characteristic of the SORF which has creative and somewhat tantalizing possibilities is that the portion of the leadframe which interconnects the corner leads of the package is wide enough to accomodate a MOS capacior for input CQ matching (means Control Q - a terminology defined by Motorola, Inc.) . Input CQ matching is accomplished by selecting the proper shunt MOS capacitor value and series inductance interconnect wire loops to raise the device's input impedance to a higher real part while minimizing the device's input circuit Q. This aids broadband matching by reducing the number of external circuit components necessary to achieve a desired broadband performance.

Summary

The SORF package offers an excellent alternative to the many low power packages that are now being used in RF applications which are not SMC. Not only is this package a popular SM package but it also has excellent RF and thermal performance comparable to the Macro-X package. The newly introduced MRF8372 and MRF5812 are excellent examples of the capabilities of this RF low power plastic SMD. The SORF package will lead the way as SMD replaces the more conventional RF low power packages of the past and adds exciting new dimensions to RF SMT.

UNEQUAL POWER SPLIT HYBRID COUPLER

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ABSTRACT

Presented in this paper are the design techniques for unequal power splitting hybrid branch line couplers. Nomograms are presented for different output coupling levels. The typical application of these devices is in the realisation of UQPSK modulators for high-bit-rate data transmitters.

****

INTRODUCTION

Branch line quadrature hybrids are familiar for their simplicity and multiuse. These hybrids are suitable as power splitters and combiners while maintaining isolation and matching at the input/output ports.

When a 3 dB quadrature hybrid is powered at input port 1 (Fig.1) and the output ports 3 & 4 are terminated in identical reflection type devices, power is delivered at isolated port 2. This property eliminates the requirement of a circulator for applications like PIN diode phase shifters and diode amplifiers (e.g. trapatt and tunnel diode amplifiers).

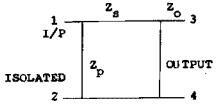

Fig.1 Quadrature hybrid

In general, hybrids for the above applications are 3 dB quadrature type, where power fed at port 1 will be divided equally with 90° phase shift. A typical example utilising the property is a balanced QPSK modulator.

When data rates of the two streams modulating the carrier in the QPSK modulator are different, the carrier power levels are unbalanced so as to maintain equal E_b/No of the two orthogonal carrier components for effective use of RF power. An attenuator and phase shifter to compensate for the phase introduced by the attenuator are used in the two output branches respectively as shown in Fig.2.

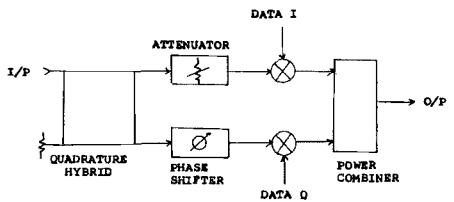

FIG.2 UQPSK MODULATOR

This arrangement increases the complexity of the circuit and is not desirable for space applications. A hybrid with unequal power division properties is a valuable tool in such applications.

The design of an unequal quadrature power divider is explained in the following paragraphs.

D E S C R I P T I O N:

The normalised voltage scattering matrix of ideal lossless hybrid with unequal power outputs, maintaining the 90° phase difference, can be represented by equation 1, where ports 1 and 2 are input and isolated ports respectively.

$$[S] = \begin{bmatrix} 0 & 0 & -jK_3 & -K_4 \\ 0 & 0 & -K_4 & -jK_3 \\ -jK_3 & -K_4 & 0 & 0 \\ -K_4 & -jK_3 & 0 & 0 \end{bmatrix} \quad \ldots\ldots\ldots 1$$

K_3 and K_4 are the normalised voltages available at ports 3 and 4 respectively, such that power available at port 3 is

$$P_3 = K_3^2 \quad \ldots\ldots\ldots 2$$

and power available at port 4 is

$$P_4 = K_4^2 \quad \ldots\ldots\ldots 3$$

For a lossless hybrid

$$K_3^2 + K_4^2 = 1 \quad \ldots\ldots\ldots 4$$

All the four branches/lines are quarter wavelength, whose impedance/admittance values are derived from the scattering matrix (1).

The admittance matrix for this unequal power split quadrature hybrid can be obtained using the transformation shown in equation 5.

$$[Y] = ([1] - [S]) ([1] + [S])^{-1} \quad .....5$$

By substituting S-matrix and solving equation 5 we get the admittance matrix as

$$[Y] = \begin{bmatrix} 0 & jK_4/K_3 & jY_3/K_3 & 0 \\ jK_4/K_3 & 0 & 0 & jY_3/K_3 \\ jY_3/K_3 & 0 & 0 & jK_4/K_3 \\ 0 & jY_3/K_3 & jK_4/K_3 & 0 \end{bmatrix} \quad ....6$$

The voltage ratios shown in equation 6 can be expressed in terms of power ratios as

$$r = P_4/P_3 = K_4^2/K_3^2$$

The admittance matrix is expressed in terms of power ratios as

$$[Y] = \begin{bmatrix} 0 & j\sqrt{r} & j\sqrt{1+r} & 0 \\ j\sqrt{r} & 0 & 0 & j\sqrt{1+r} \\ j\sqrt{1+r} & 0 & 0 & j\sqrt{r} \\ 0 & j\sqrt{1+r} & j\sqrt{r} & 0 \end{bmatrix} \quad .....7$$

The hybrid constructed from equation 7 divides the power fed at port 1 into the required proportions at port 3 & 4.

The nomograms constructed from equation 7 for obtaining the impedances of series and shunt quarter wavelength of the hybrid in an easy way are given in Fig.3.

PROCEDURE TO USE NOMOGRAMS:

The impedances obtained for a 50 ohm hybrid with +2 dB imbalance in output power levels using the nomograms is explained to illustrate the procedure for the use of the nomograms.

Mark the characteristic impedance of 50 ohms on the centre scale Zo (point A). For calculation of shunt arm impedance, make point B on the left r scale at +2 dB. Intersection point C of the Z_p scale with the line

joining points AB gives the shunt impedance. The same procedure is followed for finding series arm impedance with the right r scale.

The values obtained for Z_p and Z_s are 39.7 and 31.1 ohms respectively.

CONCLUSIONS

A set of nomograms are presented for finding series and shunt impedances directly. A hybrid with different output power levels is constructed from these nomograms and verified practically. The necessity of an unequal power divider maintaining 90° phase is explained.

ACKNOWLEDGEMENT

The authors gratefully acknowledge the encouragement from Col. N. Pant, Director, I.S.R.O. Satellite Centre and Dr.S. P. Kosta, Dy. Director (Spacecraft Electronics Group) I.S.R.O. Satellite Centre and thank other colleagues for their valuable suggestions.

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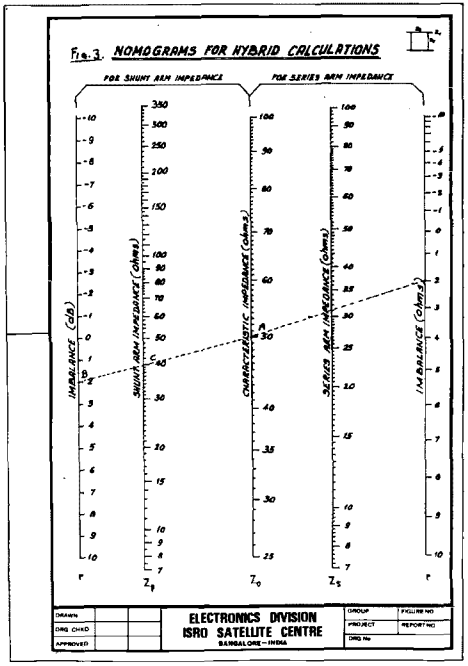

SPHERICAL DIELECTRIC ANTENNA

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A B S T R A C T

Presented in this paper is a study of near field and far field characteristics of s dielectric sphere antenna excited by a circular cylindrical metal waveguide operating in its dominant TE_{11} mode. Many interesting results as a outcome of this study are included. The system can be used as a microwave applicator, a spotbeam antenna and as a feed for a cassegrain reflector.

****

Dielectric antennas are an important class of microwave antennas. These are quite small and capable of giving directive radiations. Various forms of dielectric antennas like the solid rods, hollow tubes, horns and spherical antennas have been studied (in parts) by many researchers. Dielectric spheres in particular have been of great interest to many researchers [1,2,3, 4,5,6 & 8], owing to the simplicity of the shape and many practical applications. Most of the researchers have examined the subject with approximate near field or far field theoretical analysis and tried to compare the results with experimental ones. This paper is an outcome of an extensive theoretical study as well as experimental studies carried out on a dielectric sphere excited by a circular cylindrical metal waveguide operating in its TE_{11} mode. The subject is divided into two categories, namely:

(1) THE SOURCE FIELD OR NEAR FIELD

(2) THE FAR FIELD OR RADIATION FIELD

1.0 SOURCE FIELD STUDIES:

The far field radiation characteristics of an antenna can be deduced from the knowledge of source field distribution. The source field can be determined by solving the electromagnetic boundary value problems over the antenna. The spherical dielectric antenna considered is made of a homogeneous lossless dielectric material and

is excited by the TE_{11} mode fields of a circular cylindrical metal waveguide [7]. In order to ensure some degree of matching between the antenna and the waveguide and also to suppress the generation of higher order modes (to the extent possible), the interior of the circular cylindrical metal waveguide is filled over a short distance by the dielectric of which the sphere is composed. The generator end of the circular cylindrical dielectric rod thus formed inside the waveguide is conically tapered to a point (as illustrated in Fig.1) to take care of the matching between the waveguide and the dielectric structure (It has been experimentally seen that such a tapering [10] does improve the return losses). However, for the theoretical analysis and to simplify the analysis for the first degree of approximation, the higher order mode generation at the end of the waveguide is neglected and the propagating mode inside the waveguide is assumed to be only TE_{11}. The theoretical analysis for the source field components over the sphere is done by [6, 10] expressing the TE_{11} mode components of the cylindrical waveguide in spherical co-ordinates at the interface between the waveguide and the spherical geometry of the antenna, keeping the sense of 'ϕ' co-ordinate the same. These field components are further expressed in terms of spherical harmonics. Their respective amplitude-coefficients at the interface are determined using 'Fourier Legendre Series' [6, 9, 10], and the TE_{11} field components are expressed in a spherical co-ordinate system.

These fields at the interface are assumed to be the impressed fields in the sphere due to the waveguide excitation.

The fields internal to the sphere will consist of the fields due to the waveguide and the fields internal to the sphere obtained by solving the source free Vector wave equations [Straton-8].

The boundary conditions are matched at the surface of the sphere (r=a) for the field components internal to the sphere and the external field components obtained by solving the source free Vector wave equation [Straton-6] external to the sphere.

It is seen that during the various field matchings over the surface of the sphere (at r=a) on both sides of the equations, terms containing constants of

$$(m,\ n^{th}\text{order}) \text{ and } \frac{P_n^m(\cos\theta)}{\sin\theta} \text{ and } P_n^m(\cos\theta) \text{ do}$$

appear. Here $P_n^m(\cos\theta)$ is the Associated Legendre's Polynomial of first kind of degree 'n' and order 'm'. It is observed that for the six field components, six simulataneous equations are obtained.

From the six equations we see that the lowest [8,10] field mode which can exist is m=n, while for a given m,

there are 12 field amplitude coefficients of (m,n),(m,n+1) (m,n-1)th order, which indicates that the boundary conditions are satisfied not for a single value of n but for n-1, and n+1 combined together. This shows that for any particular value of 'm', the electric and magnetic field components consist of an infinite number of terms for values of 'n' varying from m to∞, thus indicating that for each value of m, there exist many corresponding hybrid modes.

However, the boundary conditions are matched for n=n, n=n-1, n+2 and a total of 16 equations are obtained for internal field amplitude coefficients. The coefficients are of (m,n), (m,n-1) (m,n+1) and (m,n+2) order. Sixteen simultaneous equations are solved for the 16 amplitude coefficients, which are in general complex. Knowing the m, nth order amplitude coefficients one can determine the internal and external (surface) source fields, which are used for far field computations. From the above treatment, it is inferred that a homogeneous dielectric sphere excited by a circular cylindrical metallic waveguide operating in its dominant TE_{11} mode can support an infinite number of hybrid modes which have all the six components of EM field, namely E_r, EΘ, EØ, Hr, HΘ & HØ. Representative near field patterns are given in Figs. 2-1 to 2-4.

2.0 FAR FIELD STUDIES:

Having obtained the source field distribution, the radiation or far field of the spherical dielectric antenna excited by a circular cylindrical metal waveguide is obtained using the famous - Schelkunoff's Equivalence Principle. An analysis of the radiation pattern and gain as a function of various parameters, viz. diameter of the sphere, frequency of excitation and relative permittivity of the material has been done. The studies are limited to X-band for experimental verification purposes.

3.0 NUMERICAL COMPUTATION & OBSERVATIONS:

SOURCE FIELD:

The source field components have been evaluated [6, 10]. The computation has been done for different diameters and relative permittivities of the dielectric sphere for various frequencies of excitation at X-band, for a lossless homogeneous sphere. The computations have been carried out for the first seven primary modes i.e. m=1 to 7 and n=1 to 7 (except m$\geq$n). While normalizing with respect to the maximum value of the mode out of a large number of m, n combinations, the amplitudes of the coefficients and field components for

the orders m=2 and more for all values of 'n' are almost two orders less in magnitude than those of m=1. Hence, the computation for further processing was restricted for m=1, and n=1 to 7. From the computation results, it is observed that:

(a) For all modes the external field components Er, EΘ, HØ show a cosine variation and E_{ϕ}, Hr, and H_{θ} show a sine variation with respect to 'ø' for 'ø' varying between $\pm$ 180°. This behaviour is independent of sphere diameter, frequency of excitation and dielectric constant.

(b) The variation with respect to 'Θ' for a fixed 'ø' shows that for |Er| & |Hr| there exists a null at Θ = 0, i.e. no axial radial component of E & H fields exists.

For other field components it is observed that all the modes except (1,1) show an oscillatory behaviour. |EΘ| is the strongest component.

3.2 RADIATION FIELD:

The radiation field patterns, directivity and gain have been computed for the dielectric sphere antenna using the source field components, since from the source field studies [10] it is clear that no single mode will characterise the complete source field components. Hence, the far field calculation have been carried out for the vectorial summation of even, odd and all modes of the source fields. Calculations have seen done for spheres of 100, 75 & 50mm diameters at X-band for ϵ_r=2.1, 5,7, 10 & 15. For all mode combinations of the source field, the radiation patterns for representative cases are given in Figs. 3(a), (b) and (c).

4.0 EXPERIMENTAL STUDIES:

The experimental investigations have been undertaken in order to validate the theoretical studies. The experimental work is extended to investigate some of the practical applications of the dielectric sphere antenna under investigation. The investigation has been carried out mainly for X-band frequencies (8.2 GHz) and sphere diameters: 30, 50, 75 and 100mm and the ϵ_r= 2.1.

The source field components at the surface of the sphere have been measured using near field pickup probes. The variation of these source field components as a function of Θ & ø co-ordinates is reported. The radiation field patterns have been plotted for both E&H planes. The results are reported as $|E_T|$ & $|E_p|$ patterns as a function of 'Θ' co-ordinate. Gain measure-

ment have been done using standard gain antenna substitution method, and axial ratio studies using a rotating dipole for a circularly polarized wave excited sphere antenna have also been carried out. The return loss or VSWR measurements of the antenna system is done over 7-12 GHz frequencies, using an HP8410 network analyzer. The near and far field test setups are shown in Figs. 4(a) & 4(b). The circular polarization is achieved using a septrum polarizer [10, 11].

5.0 DESIGN & CONFIGURATION OF THE ANTENNA:

A dielectric sphere of diameter > 30mm (at X-band) is excited by a circular cylindrical metallic waveguide operating in its dominant TE_{11} mode. The mode generation is achieved by two methods: (a) a coaxial to waveguide adapter changes TEM mode to TE_{10} mode. The rectangular to cylindrical waveguide gradual transition changes the TE_{10} mode to TE_{11} mode, (b) the other method of exciting TE_{11} mode inside the circular cylindrical waveguide is to adjust the depth of a coaxial connector centre pin mounted on a circular cylindrical metal waveguide and adjust the close end of the guide with a short circuit plunger such that the input VSWR is less than 1.1. One can measure the E field configuration at the open end to make sure of the existence of the TE_{11} mode.

In both systems, the waveguide at the open end is loaded with a dielectric sphere. In order to have a smooth transition between the waveguide and the sphere, at one end of the sphere there is a dielectric cylindrical rod (the same material as that of the sphere), tapered at the end, with its outer diameter equal to the internal diameter of the circular cylindrical waveguide. The length of the rod is experimentally adjusted such that no high VSWR is observed. The cylindrical dielectric rod length is less than λ. The tapered portion is $\simeq 0.68\lambda$. This configuration is almost analogous to the situation where the waveguide is filled with the dielectric material of which the sphere is made, such that the dominant mode is TE_{11} and there are no discontinuities due to dielectric mismatches.

The near field studies have been conducted using small pickup probes [10, 12], a monopole for $|E_r|$, a small dipole for E_θ & E_ϕ and a small magnetic loop for H-components. The far-field radiation studies have been conducted under the normal far field conditions. The gain is determined by comparing with a standard gain antenna while the axial ratio studies have been done using a rotating dipole. The circular polarization is achieved using a septum polarizer [10,11]. The effect of a corrugated flange at the back of the antenna has

been studied for gain and axial ratio properties. Some of the experimental results compared with the theoretical results for near field as well as far field are shown in Figs.(5) & (6), while far field experimental curves for various diameter spheres for pattern as well as axial ratio studies are shown in Figs.(7) & (8). A derived gain V/S diameter/λ curve is also given in Fig.9.

6.0 CONCLUSIONS AND POTENTIAL APPLICATIONS:

From the theoretical analysis the following observations can be made:

6.1 SOURCE FIELD:

It is possible to solve the boundary value problem for a dielectric sphere excited by a circular cylindrical metal waveguide operating in TE_{11} - mode. The theory evolved out here can be used for other popular cases, such as a dielectric sphere excited by a structure having HE_{11} - mode. The same method can be used for solving boundary value problems in ferrite spheres.

A dielectric sphere excited by a circular cylindrical metal waveguide operating in its dominant mode can sutain an infinite number of hybrid modes over its surface. The relative amplitude and phases of the modes will be different depending upon the sphere diameter, dielectric constant and frequency of excitation.

From the numerical calculations it is inferred that higher order modes are negligible in amplitude as compared to the first few primary modes.

The six source field components over the surface of the sphere show a sinusoidal variation with respect to ϕ. Er, Eθ & Hϕ show cosine variation while Eϕ, Hr and Hθ show sine variation. All the field components and their different modes except mode (1,1) show an oscillatory behaviour with respect to θ.

It is difficult to draw a general conclusion. However, it is seen that the dielectric sphere antenna excited by a circular cylindrical metal waveguide operating in TE_{11} - mode, will sustain an infinite number of hybrid modes. The relative amplitudes and phases of these modes will be diffarent depending upon the sphere diameter, dielectric constant and frequency of excitation.

6.2 RADIATION FIELD:

From the radiation field studies it is observed that the dielectric sphere loading increases the gain

of a simple cylindrical waveguide and provides an E and H - plane pattern symmetry with a circular beam cross section. With increase in dielectric constant the main lobe width increases and the directivity reduces. It is seen that for a given sphere diameter and frequency of excitation there is an optimum dielectric constant for which maximum gain is obtained. Just as with increase in dielectric constant or relative permittivity, the directivity does not increase. For $\frac{d}{\lambda} \simeq 2$ to 2.1, for maximum directivity the ε_r should be $\simeq$ 2.1 - to 5.0, beyond which the main lobe width will start increasing. The sphere for a given diameter shows a resonance phenomena. The increase in frequency does not increase the gain proportionately.

6.3 EXPERIMENTAL STUDIES:

From the experimental investigations the following was found:

6.3.1 SOURCE FIELD:

Over the surface of the sphere all six EM - field components exist. All six source field components show a sinusoidal dependence on ϕ (FIG.10).

There is a good agreement between the theoretical and experimental source field plots for spheres of diameters $>$ 2X waveguide diameter. The agreement is for a combination of certain modes and not for an individual mode. The agreement appears to be there even without probe compensation.

6.3.2 RADIATION FIELD:

There is an agreement between the theoretical [for all mode combination] and experimentally obtained radiation field plots as far as over-all pattern shape is concerned. The theoretical plots show higher side lobes and slightly wider main lobe compared to the experimental. The theoretical gain is less than the experimental.

From the experimental radiation field plots, it is seen that the main beam has a circular cross section with an approximate E - and H - plane pattern symmetry compared to the waveguide alone. The sphere increases the gain and compresses the beam of the waveguide pattern. Even a hemisphere compresses the waveguide pattern and increases the gain by almost 3 dB. For $\frac{d}{\lambda} = 2.1$ or more the radiation field patterns appear to be Gaussian beam pattern.

It is seen that the dielectric sphere antenna gives 1-3 dB increase in gain over a uniformly illuminated equivalent aperture, depending upon the d/λ. Optimum

gain is obtained for $\frac{d}{\lambda} \simeq 2.1$ to 2.5 [Tables & Fig.9].

There is good VSWR matching for all the spherical antennas studied here over the frequency band 7 - 12.4GHz. The VSWR or return loss shows some type of resonance phenomena. The minimum VSWR $\simeq$ 1.1 while the maximum $\simeq$ 1.6 (Fig.11).

The sphere does not disturb but slightly improves the axial ratio, if excited by a waveguide with a circularly polarized signal. A choked flange at the back of the sphere reduces the side lobes, increasing the gain. The position of the flange from the open end of the waveguide can be experimentally adjusted for minimum axial ratio and maximum gain.

7.0 POTENTIAL APPLICATIONS:

The good E- and H- plane pattern symmetry with circular beam cross section, low side lobes, Gaussian beam, excellent VSWR matching with the excitor, good axial ratio for circular polarized exciting signal, focusing of the beam, small and compact size make the antenna under discussion a potential candidate for many applications as a primary antenna, secondary antenna and also a microwave applicator. A few of the applications are:

SPOT/GLOBAL BEAM ANTENNA FOR COMMUNICATION SATELLITES

The antenna can be used to provide spot and global beams for geosyncronous communication satellites, with good axial ratio and low cross polar component with E- and H-plane pattern symmetry. With the use of a proper septum the antenna can be used for orthogonal polarization transmission/reception of signals with isolation better than or $\simeq$ 30 dB. This would be a typical example of the antenna being used as a primary antenna. The small size of the antenna makes it quite attractive, especially for dual polarized global beam coverage, for $\epsilon_r = 2.1, \frac{d}{\lambda} \simeq$ 2.5 is suitable for a global beam.

SHAPED WIDE BEAM ANTENNA:

The inherent E- and H- plane pattern symmetry, good axial ratio for circularly polarized signal and excellent VSWR matching with the exciting structure properties of the dielectric sphere antenna, are used in achieving a wide beam antenna with a dip in the centre of the pattern and gains at the beam edge. The pattern is such that for a 900 KMS orbiting spacecraft the antenna gain compensates for the path loss variations. Such an antenna has been developed for onboard use on the Indian Remote Sensing Satellite for transmitting data at

X-band. The antenna developed is a dielectric sphere (hemisphere) excited in two orthogonal circular polarizations generated using a septum polarizer. On the dielectric sphere antenna six metallic diffraction strips have been symmetrically placed. The width of the strips is experimentally adjusted such that we get around $\pm$ 65° beam width with maximum gain $\simeq$ +5 dBi at $\simeq \pm$ 65° and a null at the centre ($\simeq$ -7dB). A corrugated reflector flange has been used to shape the beam at the edges. The diffraction strips widen the beam and give a null at the centre and gain at $\pm$ 65°. The dielectric sphere maintains the E- and H- plane pattern symmetry. Since the strips are symmetrically placed the circular polarization remains unchanged. The antenna has been successfully developed. The practical antenna alongwith the pattern and the IRS Spacecraft is shown in Fig.12.

DIELECTRIC SPHERE ANTENNA AS A FEED FOR A REFLECTOR:

The antenna under discussion can be used as a prime focus feed for a reflector or a feed for a Cassegrain reflector antenna. The dielectric sphere antenna, with its good axial ratio, E- and H- plane pattern symmetry and low side lobes, can easily replace the conventional horn feed for Cassegrain reflectors.

The other applications of the dielectric sphere antenna can ba as a feed for a Compact Range Reflector and probes for near field measurements.

AS MICROWAVE APPLICATORS FOR MEDICAL USES:

Since the dielectric sphere antenna provides a focussed beam of circular cross-section with side lobes suppressed, the system can be used effectively as a microwave applicator for clinical/medical uses. A few of the applications are:

1) Applicator for diathermy (non-contact type) - the clinical technique used to achieve 'deep heating', that is inducing heat in tissues beneath the skin and subcutaneous fatty layers.

2) The system can be easily used for selective heating (re-warming) of cancer tumors in deeply cooled animals to enhance the effectiveness of tumor chemotherapy treatment. This technique is called differential hyperthermia.

3) These antennas can also be used for diagnosing and monitoring pathological cardio - pulmonary conditions.

The antenna system can be very effectively used in cases where focusing of electromagnetic energy for

irradiation of biological organs is required. The comparative small size of the antenna makes it an excellent microwave applicator for clinical uses.

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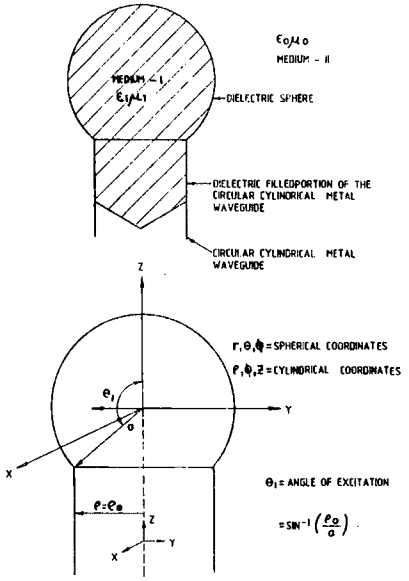
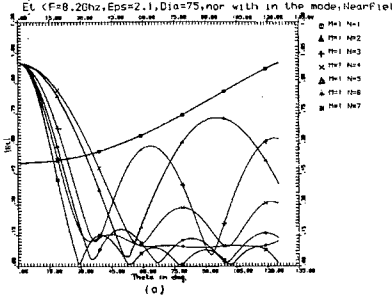


FIG. 1 ANTENNA GEOMETRY

...3



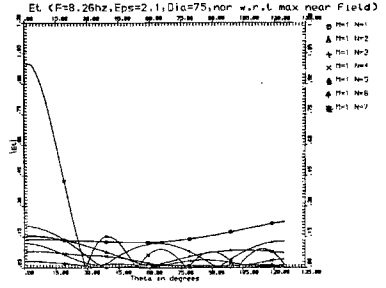
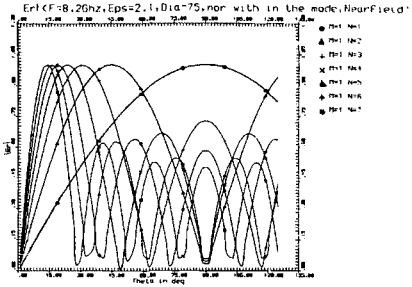
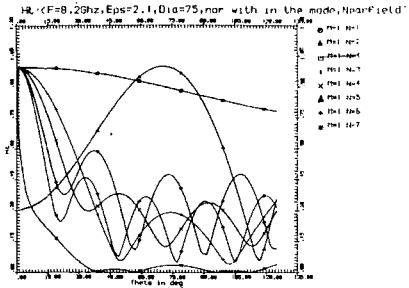
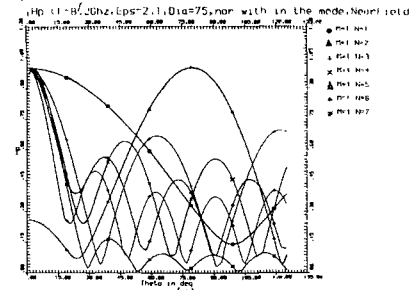


FIG 2-1







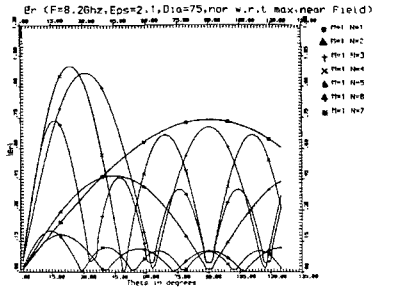


FIG 2-2

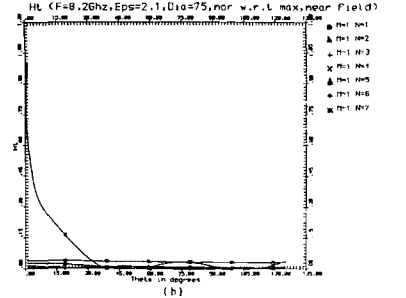


FIG 2-3

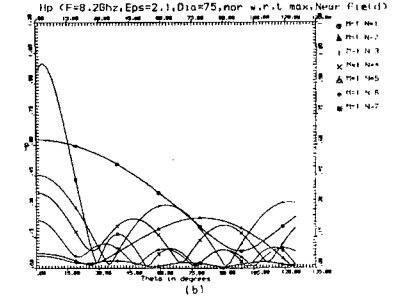
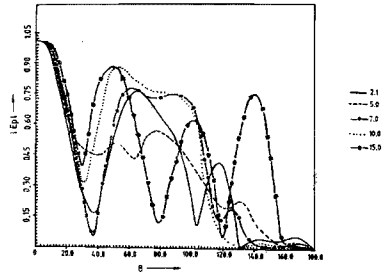
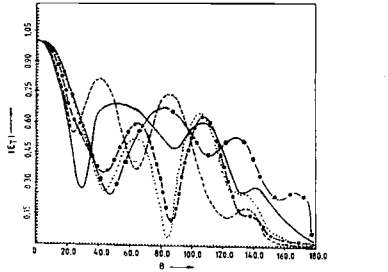


FIG 2-4

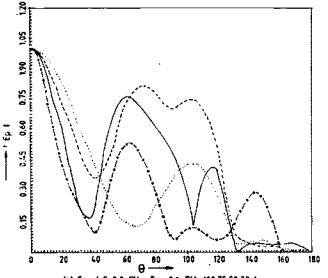


(a) Eφ (F = 8.2 GHz, DIA= 75, Eps = 2.1, 5, 7, 10, 15)

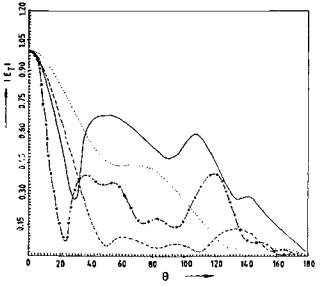


(b) Eθ (F= 8.2, DIA= 75, Eps = 2.1, 5, 7, 10, 15)

FIG.3a RADIATION PATTERNS/FAR FIELD (THEORETICAL)

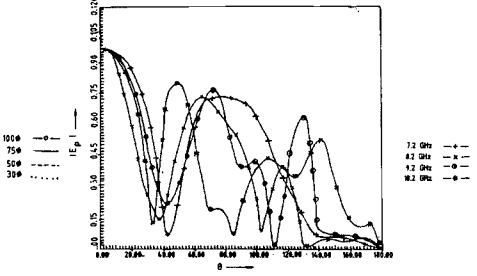


(a) Eφ (F=8.2 GHz, Eps=2.1, DIA=100,75,50,30)

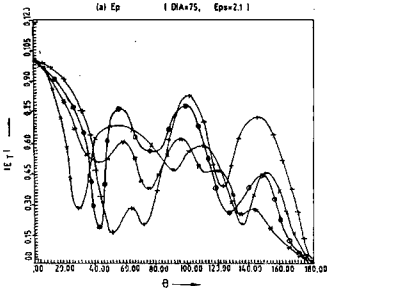


(b) Eθ (F=8.2 GHz, Eps=2.1, DIA=100, 75,50,30)

FIG. 3c FAR FIELD RADIATION PATTERNS (THEORETICAL)



(a) Eφ (DIA=75, Eps=2.1)



(b) Eθ (DIA=75, Eps=2.1)

FIG.3b FAR FIELD RADIATION PATTERNS - THEORITICAL)

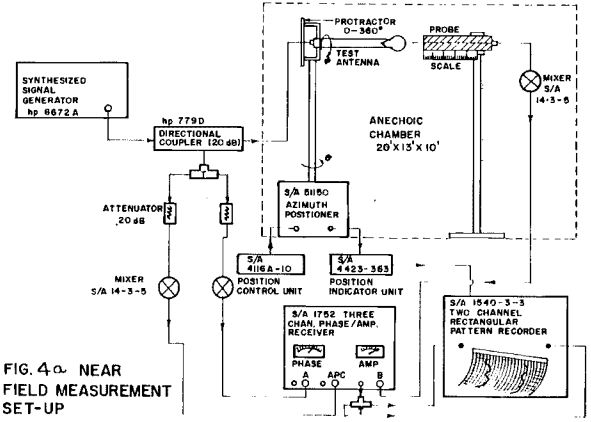


FIG. 4a NEAR FIELD MEASUREMENT SET-UP

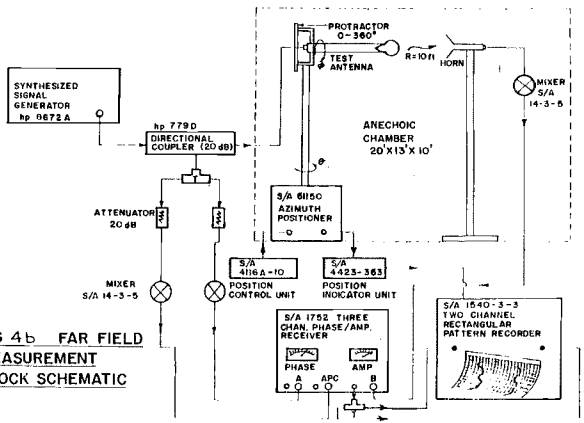
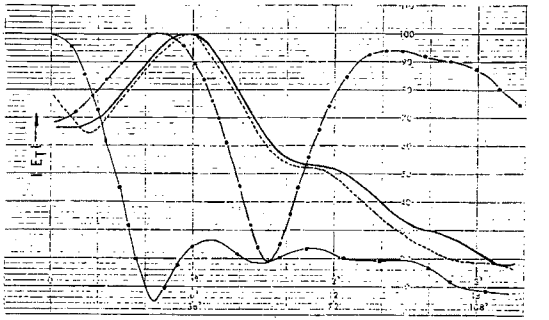
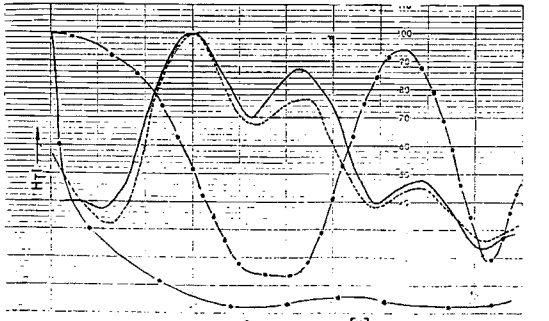


FIG 4b FAR FIELD MEASUREMENT BLOCK SCHEMATIC

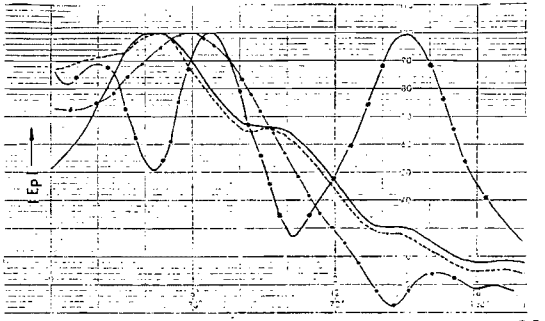


a) E_T (F= 8.2 GHz, Eps=2.1, DIA=75)

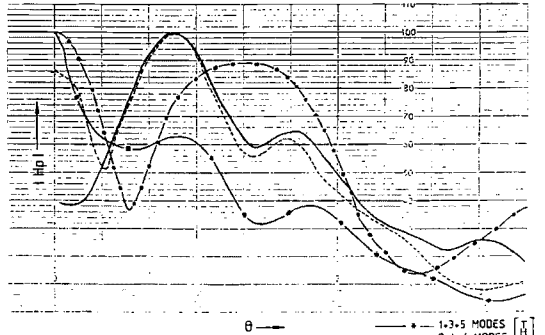


(b) H_T (F=8.2 GHz, Eps=2.1, DIA=7.5)

FIG. NO. 5 a

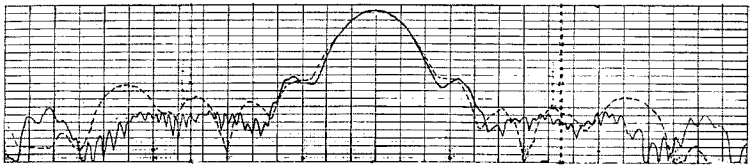


(a) Ep (F=8.2 GHz, Eps=2.1, DIA=75)

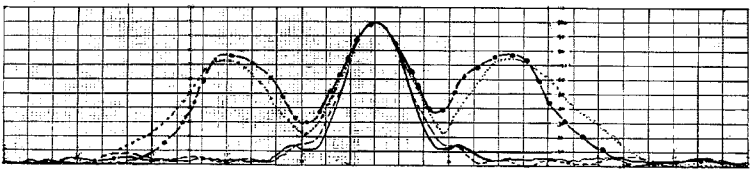


(b) Hp (F=8.2 GHz, Eps=2.1, DIA=75)

FIG. NO. 5 b

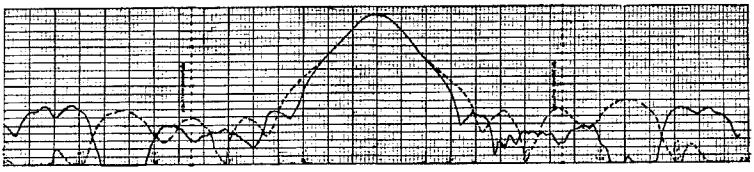


FREQ. 8·2 GHz DIA = 75 Eps = 2.1

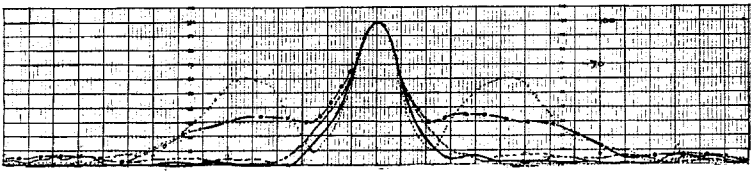


—— E - PLANE
--- H - PLANE
EXPERIMENTAL
···· E - PLANE
—·— H - PLANE
THEORETICAL

FIG. 6(a) FAR FIELD RADIATION PATTERN - EXPERIMENTAL / THEORETICAL



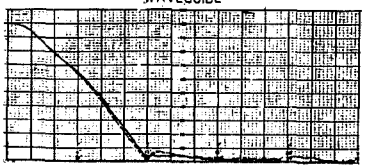
FREQ= 8.2 GHz DIA = 100 Eps = 2.1



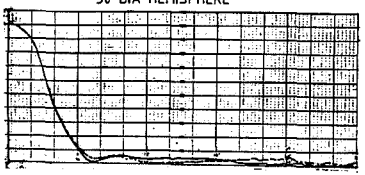
—— E - PLANE
---- H - PLANE
EXPERIMENTAL
····· E - PLANE
—·—H - PLANE
THEORETICAL

FIG. 6(b) FAR FIELD RADIATION PATTERN - EXPERIMENTAL / THEORETICAL

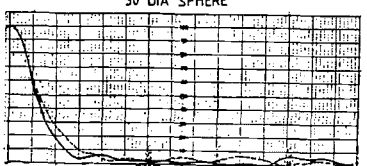
WAVEGUIDE



30 DIA HEMISPHERE



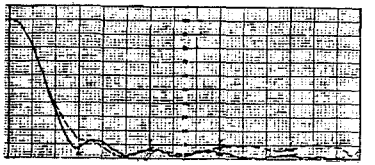
50 DIA SPHERE



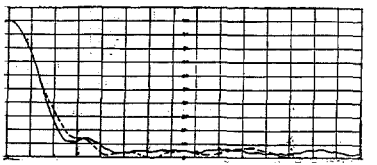
100 DIA SPHERE

E PLANE ——
H PLANE ----

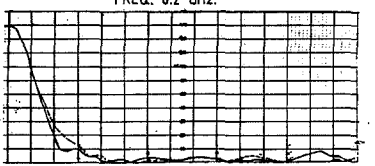
FIG.NO. 7(a) FAR FIELD RADIATION PATTERNS EXPERIMENTAL
FREQ.= 8.2 GHz Eps=2.1



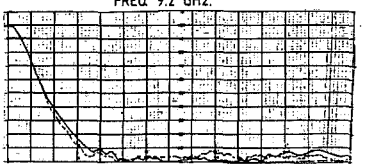
FREQ. 7.2 GHz.



FREQ. 8.2 GHz.



FREQ 9.2 GHz.



FREQ. 10.2 GHz.

E PLANE ——
H PLANE ----

FIG. NO. 7(b) FAR FIELD RADIATION PATTERNS – EXPERIMENTAL
DIA=75 Eps=2.1

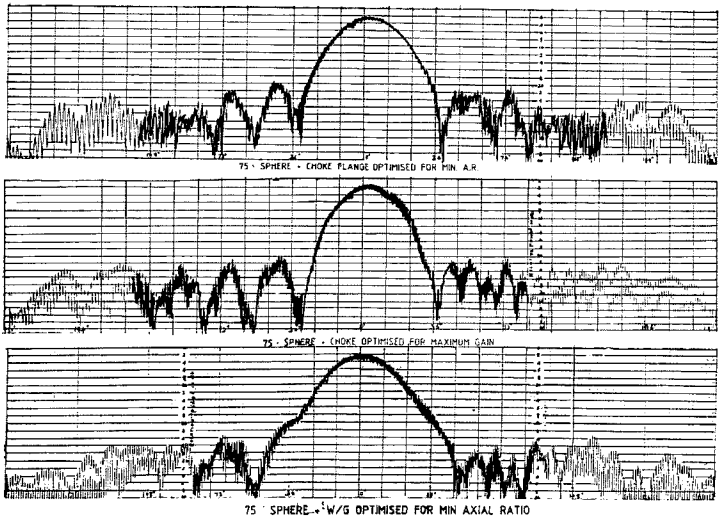

75 · SPHERE · CHOKE FLANGE OPTIMISED FOR MIN. A.R
75 · SPHERE · CHOKE OPTIMISED FOR MAXIMUM GAIN
75 · SPHERE · W/G OPTIMISED FOR MIN AXIAL RATIO

FIG. 8(a) ROTATING DIPOLE PATTERN (FREQ. 8.2 GHz)

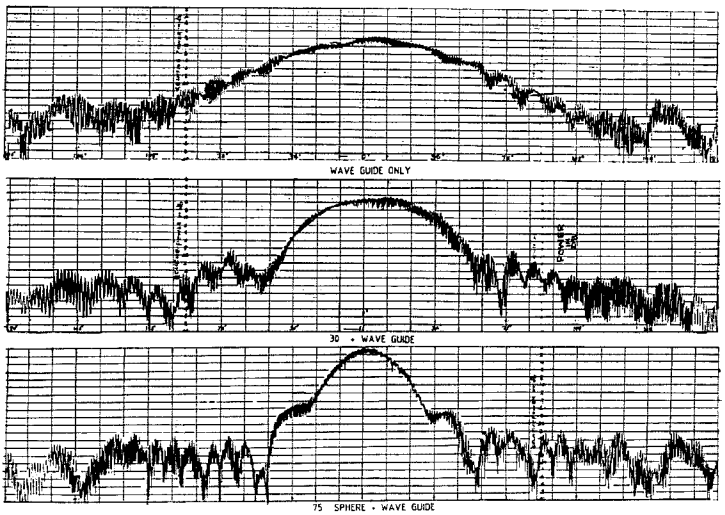


FIG. 8(b) ROTATING DIPOLE PATTERN (FREQ. 8.25 GHz)

TABLE - I

Sl.No.	DESCRIPTION	7.2 GHz	8.2 GHz	9.2 GHz	10.2 GHz
1.	WAVEGUIDE - GAIN IN DB				
	a) MEASURED	6.7	10.2	9.5	10.6
	b) UNIFORM APERTURE	7.08	8.24	9.2	10.1
2.	30mm dia - GAIN IN DB				
	a) MEASURED	10.7	13.4	10.5	12.3
	b) OPTIMISED	11.7	14.6	-	-
	c) UNIFORM APERTURE	7.08	8.24	9.2	10.1
	d) THEORETICAL	-	14.48	-	-
3.	50mm dia - GAIN IN DB				
	a) MEASURED	12.5	14.4	14.8	12.6
	b) OPTIMISED	14.5	16.4	15.4	13.7
	c) UNIFORM APERTURE	11.5	12.7	13.7	14.6
	d) THEORETICAL	-	13.25	-	-
4.	75mm dia - GAIN IN DB				
	a) MEASURED	16.0	17.6	18.0	16.3
	b) OPTIMISED	16.7	18.3	18.6	17.0
	c) UNIFORM APERTURE	15.0	16.2	17.2	18.9
	d) THEORETICAL	-	14.28	-	-
5.	100mm dia - GAIN IN DB				
	a) MEASURED	16.5	17.3	16.8	16.3
	b) OPTIMISED	18.9	17.7	17.9	16.6
	c) UNIFORM APERTURE	17.5	18.7	19.6	20.6
	d) THEORETICAL	-	16.89	-	-

T A B L E - II

Sl.No.	SPHERE DIAMETER	AXIAL RATIO IN dB		GAIN IN dB	
		WAVEGUIDE & SPHERE	WAVEGUIDE CHOKE & SPHERE	SPHERE & W/G	W/G + SPHERE & CHOKE POSITION OPTIMISED
1.	30mm dia	1.5	1.0	13.4	14.8
2.	50mm dia	1.0	0.8	14.4	16.9
3.	75mm dia	1.0	0.5	17.6	18.6
4.	100mm dia	2.0	1.8	17.3	17.9

FREQUENCY : 8200 MHz

ε_r : 2.1

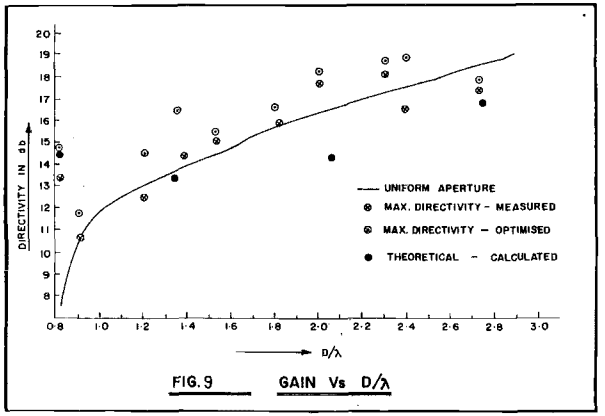


FIG. 9 GAIN Vs D/λ

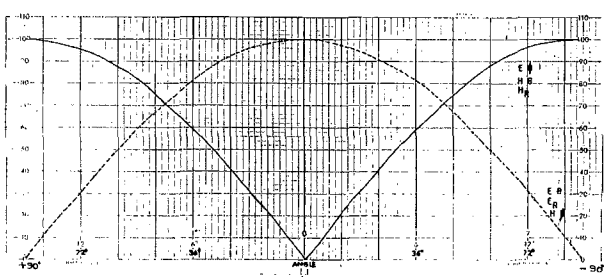


FIG. 10 VARIATION OF SOURCE FIELD COMPONENTS WITH φ

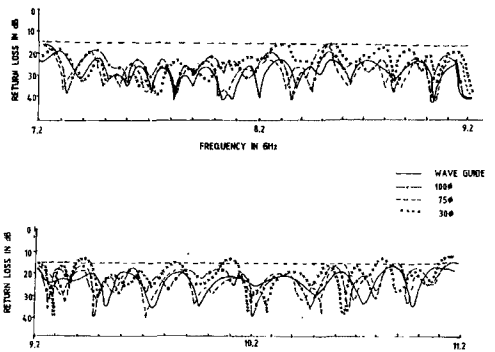
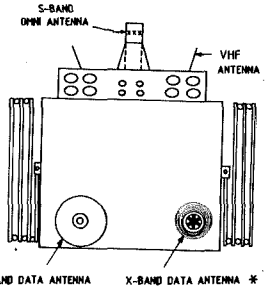
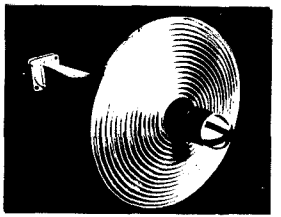


FIG. 11 RETURN LOSS OF THE ANTENNA SYSTEM

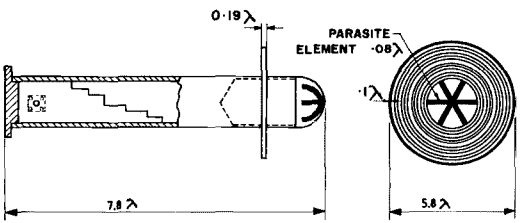
FIG 12.ANTENNA SYSTEM OF IRS



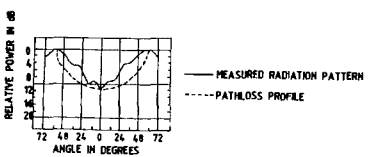
a) ANTENNAS MOUNTED ON THE EARTH VIEWING FACE OF IRS.



b) PRACTICAL X-BAND DATA TRANSMITTING ANTENNA



* c) SCHEMATIC OF X-BAND DATA TRANSMITTING ANTENNA



d) X - BAND ANTENNA PATTERN

Average Efficiency of Power Amplifiers

by
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ABSTRACT

Accurate prediction of the heat dissipation and power consumption of power amplifiers and transmitters requires knowledge of their average efficiency. Since the instantaneous efficiency of a PA depends upon the signal amplitude relative to the peak-envelope power (PEP), the average efficiency depends upon both the type of power amplifier and the type of signal being amplified. This paper relates average power input, power output, and efficiency to the characteristics of the PA and the probability-density functions (p.d.f.s) of the signal. The p.d.f.s for a variety of commonly used signals, including two-tone SSB/SC, single-tone AM, uniform, QAM, Rayleigh, Laplacian, Gaussian, Gaussian AM, and Laplacian AM are presented. The average efficiencies of class-A, -B, and -D PAs are then derived for two-tone and Rayleigh-envelope signals.

1. INTRODUCTION

Accurate prediction of the average efficiency and/or power consumption of a power amplifier (PA) or transmitter is required in many applications. Some examples of radio-system components and parameters that depend upon the efficiency and power consumption are:

- Battery life,
- Solar-cell, battery, or generator capacity,
- Heat-sink size and weight,
- Ancillary cooling requirements, and
- Operating costs.

Knowledge of the average-efficiency characteristics allows the designer to make intelligent decisions based upon the costs and benefits of different system approaches. For example, class-D RF PAs and class-S AM modulators have better efficiencies than do class-C RF PAs and class-B series-pass AM modulators, but are also more complex and expensive [1, 2]. Knowledge of the average-efficiency characteristics of class-G PAs, envelope-tracking systems, outphasing systems, and Doherty systems is necessary to set their parameters for maximum-efficiency operation.

The efficiency of a PA generally varies with the amplitude of the signal, and usually increases to a maximum value at the peak envelope power (PEP) or maximum signal voltage. Efficiency curves for typical class-A, -B, and -D PAs are shown in Figure 1a.

Since FM and CW signals have only one amplitude level, knowledge of the efficiency and input power at PEP is sufficient. Inspection of the curves in Figure 1a shows that modest improvements in efficiency are achieved by changing the class of amplification.

In contrast, amplitude-modulated signals (including SSB, television, and

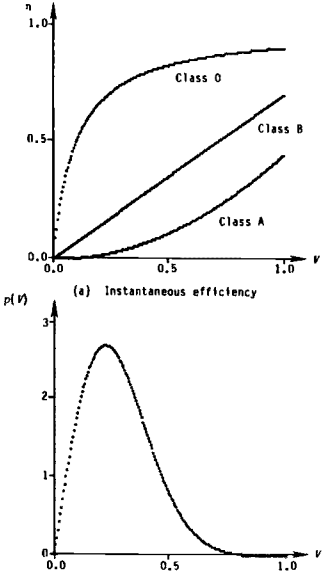

Figure 1. Efficiency and p.d.f. curves.

multicarrier relay) and wideband signals contain a variety of different amplitudes that produce a variety of different instantaneous efficiencies. The p.d.f. for a typical multitone SSB or multicarrier envelope (Figure 1b) shows that low- and middle-level amplitudes are far more prevalent than amplitudes near PEP. At the most likely amplitude, the efficiencies of the class-A, -B, and -C PAs of Figure 1a differ considerably, hence significant improvements in the average efficiency can be expected by changing the class of amplification.

It would be natural to define *average efficiency* as the average of the instantaneous PA efficiency. However, average efficiency thus defined is an interesting indicator of PA performance but otherwise useless. A preferable definition is the ratio of the average output and average input powers; that is

$$\eta_{AVG} = \frac{P_{oAVG}}{P_{iAVG}} \quad . \tag{1}$$

Inspection of the amplifier-efficiency and signal-p.d.f. curves of Figure 1 shows that average efficiency depends upon both PA characteristics and signal characteristics. This paper develops the relationships that can be used to predict average efficiency, and gives the p.d.f.s for a variety of commonly used signals. Example calculations are performed for class-A, -B, and -C PAs.

2. CHARACTERISTICS OF SIGNALS

Signals can be classified as either wideband or narrowband. Instantane-

ous PA efficiency and input power are generally related to the instantaneous amplitude (voltage) of a wideband signal, or to the instantaneous envelope of a narrowband signal [1].

The statistical characteristics of the signal amplitude are described by its probability-density function (p.d.f.). Integration of a p.d.f. over a particular range of amplitudes gives the probability that the signal amplitude is within that range [5]; i.e.,

$$P(V_1 < V < V_2) = \int_{V_1}^{V_2} p(V)\, dV \quad . \tag{2}$$

The relationship of the p.d.f. to a signal voltage or envelope is illustrated in Figure 2. The full-wave rectified sinewave is, of course, a deterministic (rather than random) signal. Nonetheless, the p.d.f. is an appropriate means of describing the amount of time spent at each amplitude.

The p.d.f. can be derived from the waveform or envelope by using the definition of the p.d.f. to equate corresponding areas under the two curves, as illustrated in Figure 2. The "probability" of the angular-time variable θ being in an interval of width $d\theta$ is $d\theta/2\pi$. If only one of the points at which the waveform has voltage V is considered, then

$$p(V)\, dV = d\theta/2\pi \quad , \tag{3}$$

Taking the limit as $d\theta \to 0$ and rearranging produce

$$p(V) = |d\theta/dV|/2\pi \quad . \tag{4}$$

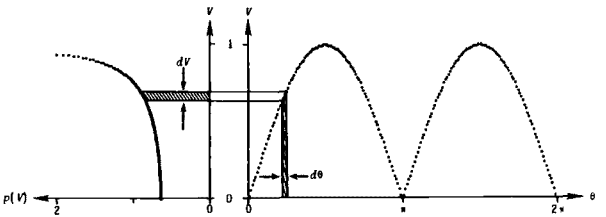

Figure 2. Derivation of p.d.f. from waveform.

The full-wave rectified sinusoid is represented by

$$V(\theta) = |\sin \theta| \quad , \tag{5}$$

hence

$$\theta = \pm \arcsin V \pm n\pi/2 \quad , \tag{6}$$

and

$$|d\theta/dV| = (1 - V^2)^{-1/2} \quad . \tag{7}$$

Since there are four intervals in θ that make equal contributions to $p(V)$, the p.d.f. is

$$p(V) = (2/\pi)(1 - V^2)^{-1/2} \quad . \tag{8}$$

The average values of desired parameters are computed by integrating the product of the parameter and the p.d.f. of the signal envelope or voltage over the appropriate range. The average input power is therefore given by

$$P_{iAVG} = \int_0^{V_{max}} P_i(V)\, p(V)\, dV \quad , \tag{9}$$

where $P_i(V)$ is the instantaneous input power. In the absence of an analytical form for input power, interpolation in a table of measurements can be used.

Power output is proportional to the square of the instantaneous voltage or envelope. The average power output with a wideband signal is therefore

$$P_{oAVG} = \int_0^{V_{max}} V^2\, p(V)\, dV \quad . \tag{10}$$

Since the envelope of a narrowband signal modulates a sinusoidal carrier, and integration of the square of that carrier over one cycle produces a factor of 1/2, the average power output with a narrowband signal is

$$P_{oAVG} = \frac{1}{2} \int_0^{V_{max}} V^2\, p(V)\, dV \quad . \tag{11}$$

3. PROBABILITY-DENSITY FUNCTIONS

This section presents a number of p.d.f.s that are useful in the analysis of the average efficiencies of power amplifiers. As discussed subsequently, a particular p.d.f. may apply to the instantaneous voltage of a wideband signal, the envelope of narrowband signal, or both.

The p.d.f.s presented below are based upon the normalization

$$V = V_{om}/V_{omPEP} \tag{12}$$

for narrowband signals or

$$V = |v_o|/v_{omax} \tag{13}$$

for wideband signals. These normalizations conveniently limit the range of

values to

$$0 \leq V \leq 1 \quad . \tag{14}$$

The second normalization requires the efficiency of wideband PAs to be expressed in terms of the absolute value of the instantaneous output voltage.

The first and second moments are defined by

$$\mu_1 = \int_0^1 V\, p(V)\, dV \tag{15}$$

and

$$\mu_2 = \int_0^1 V^2\, p(V)\, dV \quad . \tag{16}$$

These quantities are the average voltage and average squared voltage, and appear frequently in average-efficiency analyses.

The *peak-to-average ratio* ξ is defined as the ratio of the peak output power or peak envelope power (PEP) to the average output power. For both wideband and narrowband signals, the normalizations produce

$$\xi = P_{o\max}/P_{o\mathrm{AVG}} = 1/\mu_2 \quad . \tag{17}$$

For full-carrier amplitude-modulated (AM) signals, the modulation peak-to-average ratio is also of interest. Since the normalized modulating voltage is limited by (11) to 1/2 (for a carrier level of 1/2), $P_{m\max} = 1/4$ and

$$\xi_m = P_{m\max}/P_{m\mathrm{AVG}} = 1/(4P_{m\mathrm{AVG}}). \tag{18}$$

Two-Tone Envelope

The full-wave rectified sinewave given by (4) and shown in Figure 2 occurs for

- Wideband amplification of a constant-amplitude sinusoid,
- Narrowband amplification of a DSB/SC signal with single-tone modulation,
- Narrowband amplification of an SSB/SC signal resulting from two equal-amplitude tones, and
- Certain types of data signals employing two-tone AFSK modulation.

The third case is the commonly used *two-tone* test signal, as is easily shown by trigonometric substitutions.

The p.d.f. of the two-tone envelope is given by (7) and shown in Figures 2 and 3. It is apparent that the amplitudes near PEP are more likely than those near zero. For deterministic signals such as this, most calculations are more easily performed in the time domain. However, the p.d.f. is useful for inclusion in numerical-evaluation programs that incorporate other p.d.f.s. Time-domain integration yields $\mu_1 = 2/\pi$ and $\mu_2 = 1/2$, hence the peak-to-average ratio is

$$\xi = 1/\mu_2 = 2 + 3 \text{ dB} \quad . \tag{19}$$

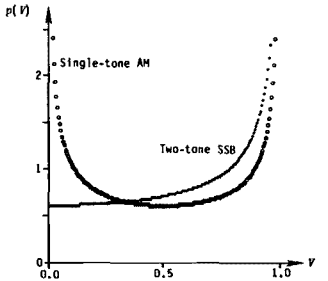

Figure 3. P.d.f.s for two-tone envelope and single-tone AM.

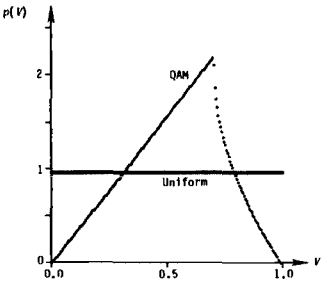

Figure 4. P.d.f.s for uniform and QAM envelopes.

Single-Tone AM

A full-carrier AM signal with 100-percent modulation by a single tone is described by

$$V(\theta) = (1/2)(1 + \sin \theta) \quad , \tag{20}$$

hence application of the method of Section 2 produces

$$p(V) = (2/\pi)[1 - (2V - 1)^2]^{-1/2} \quad . \tag{21}$$

Time-domain integration of (20) yields $\mu_1 = 1/2$ and $\mu_2 = 3/8$, hence the peak-to-average ratio

$$\xi = 1/\mu_2 = 8/3 = 4.3 \text{ dB} \quad . \tag{22}$$

Uniform

When all signal amplitudes are equally likely, they are said to be uniformly distributed and have the p.d.f.

$$p(V) = 1 \quad , \tag{23}$$

which is shown in Figure 4. This p.d.f. occurs for

- The limiting case for certain amplitude companders,
- Full-carrier AM with triangular or sawtooth modulation, and
- Wideband amplification of triangular or sawtooth waveforms.

Integrals (15) and (16) yield $\mu_1 = 1/2$ and $\mu_2 = 1/3$, hence the relatively

low peak-to-average ratio

$$\xi = 1/\mu_2 = 3 \div 4.8 \text{ dB} \quad . \tag{24}$$

Because the uniform p.d.f. is often amenable to analytical evaluation of averages, it can be a useful means of checking for proper operation of numerical-evaluation programs.

Quadrature-Amplitude Modulation

Quadrature-amplitude modulation (QAM) is an efficient means of maximizing data-transmission capability by separate amplitude modulation of the I and Q components of the signal. For example, sixteen-symbol QAM transmits four bits of information per data symbol.

In contrast to FSK, PSK, and QPSK, QAM produces a number of different signal amplitudes. For a small number of symbols, the average power and efficiency are easily evaluated by determining the specific amplitudes and their probabilities. Results for 16-, 64-, and 256-symbol QAM are given in [6].

As the number of symbols in QAM increases, the signal space becomes a uniformly filled rectangle with the peak-envelope power occuring at the corners of the rectangle. The p.d.f. (Figure 4), of this *infinitely packed QAM* signal is

$$p(V) = \begin{cases} \pi V & , 0 \le V \le 1/2^{1/2} \\ \pi V - 4 V \arctan(2 V^2 - 1)^{1/2}, & 1/2^{1/2} < V < 1 \end{cases} \quad . \tag{25}$$

The first and second moments of this p.d.f. are (from numerical integration) $\mu_1 = 0.5411$ and $\mu_2 = 0.3333$. The peak-to-average ratio is therefore

$$\xi = 1/\mu_2 = 3 \div 4.8 \text{ dB} \quad . \tag{26}$$

Gaussian

The sum of a large number of well behaved, independent random variables tends to have a Gaussian p.d.f. [5]. Broadcast sound [7], certain radar and sonar pulses [7], music [8], and other signals can be assumed to be Gaussian in the absence of other statistical data. The envelope of a DSB/SC signal modulated by such sounds is also Gaussian.

Since most PAs are characterized in terms of the absolute value of the instantaneous output voltage or the envelope, it is convenient to use the single-sided Gaussian p.d.f. If the small area above $V = 1$ is ignored (which is reasonable for $\xi > 5$ dB), the average output power for a wideband signal is $\sigma^2 = \mu_2$, hence

$$\xi = 1 \; / \; \sigma^2 \quad . \tag{27}$$

The p.d.f. can now be written as

$$p(V) = (2\xi/\pi)^{1/2} \exp(-V^2 \xi/2) \quad . \tag{28}$$

The integral (14) is evaluated by converting $2VdV$ into dV^2, which produces

$$\mu_1 = (2/\pi)^{1/2} \sigma = (2\xi/\pi)^{1/2} \quad . \tag{29}$$

As shown in Figure 5, increasing the peak-to-average ratio makes low ampli-

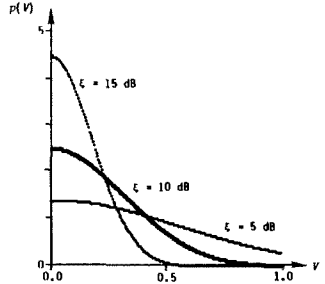

Figure 5. Gaussian p.d.f.s.

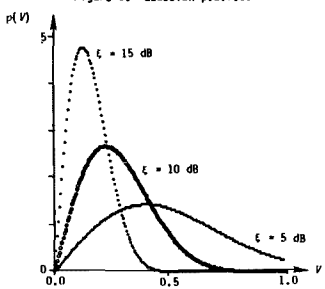

Figure 6. Rayleigh p.d.f.s.

tudes more likely. Peak-to-average ratios in the range of 10 to 15 dB are typical [8].

Rayleigh

Independent Gaussian I and Q components of equal power produce a Rayleigh-distributed envelope and a uniformly-distributed phase. The sum of independent Rayleigh phasors is itself a Rayleigh phasor, and the sum of a large number of well behaved independent phasors tends toward a Rayleigh phasor [5]. The Rayleigh p.d.f. is therefore appropriate [1, 6, 9] for the envelope of a narrowband signal in applications such as

- SSB/SC signals resulting from noise-like modulation,
- Multiple-carrier relay signals, and
- Independent-sideband (ISB) transmissions.

It is convenient to write the p.d.f. as

$$p(V) = 2V\,\xi\,\exp(-V^2\,\xi) \quad . \tag{30}$$

If the area above $V = 1$ is included, integration produces $\mu_2 = 1/\xi$. From [5] or standard integral tables,

$$\mu_1 = (\pi\,\alpha)^{1/2}/2 = (\pi/4\xi)^{1/2} \quad . \tag{31}$$

The effect of the peak-to-average ratio upon the p.d.f. is shown in Figure 6. In multicarrier-relay applications, ξ is easily related to the amplitudes and/or number of the carriers [1]. The average output power is simply the sum of the powers of the individual carriers, since they are of different

frequencies and therefore mutually orthogonal. However, the peak power is proportional to the square of the sum of the peak voltages, since at some point in time all carriers add in phase. Given N carriers of equal amplitudes, the peak-to-average ratio is therefore

$$\xi = P_{oPEP}/P_{oAVG} = N^2/N = N \quad . \tag{32}$$

Flat-Topped Rayleigh

The probability of flat topping by a signal with a Rayleigh-distributed envelope is

$$P_{FT} = \int_1^\infty p_R(V)\, dV = \exp(-\xi_R) \quad , \tag{33}$$

where p_R and ξ_R represent the p.d.f. and peak-to-average ratio, respectively, of the original signal. The probability of flat topping is only 4.2 percent for $\xi_R = 5$ dB, and drops rapidly to 0.005 percent at $\xi_R = 10$ dB.

In most applications, satisfactory accuracy can be obtained by using the standard Rayleigh p.d.f. and ignoring the small contributions due to $V > 1$. However, when the peak-to-average ratio is very low the effects of flat topping cannot be ignored. A flat-topped Rayleigh p.d.f. [10] can then be formed from the standard Rayleigh p.d.f. and the Dirac delta function:

$$p_F(V) = p_R(V) + P_{FT}\, \delta(V - 1) \quad . \tag{34}$$

The moments of this p.d.f. must be computed numerically. In addition, special handling of this p.d.f. is required in numerical-evaluation programs to ensure accurate accommodation of the contributions of the delta function.

Laplacian

The Laplacian (also called one-sided exponential) p.d.f. (Figure 7) applies to

- Speech waveforms [11] and
- SSB/SC envelopes produced by speech modulation [9].

The gamma p.d.f. is said to be a better approximation to the true p.d.f. of speech [12], but its additional complexity is not warranted for PA average-efficiency analysis.

The Laplacian p.d.f. has the form

$$p(V) = (2\xi)^{1/2} \exp[(2\xi)^{1/2}\, V] \quad , \tag{35}$$

which produces $\mu_2 = 1/\xi$ if the area above $V = 1$ is included. The first moment is then

$$\mu_1 = \sigma/2^{1/2} = (2/\xi)^{1/2} \quad . \tag{36}$$

Gaussian AM

Full-carrier amplitude modulation by a Gaussian signal produces an RF signal with a Gaussian-AM envelope. The envelope p.d.f. is a Gaussian p.d.f. whose mean is the amplitude of the unmodulated carrier. By analogy to (28),

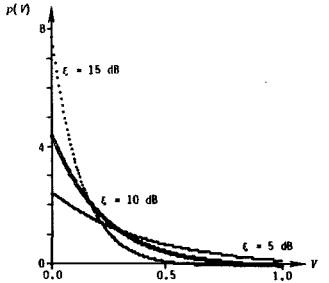

Figure 7. Laplacian p.d.f.s.

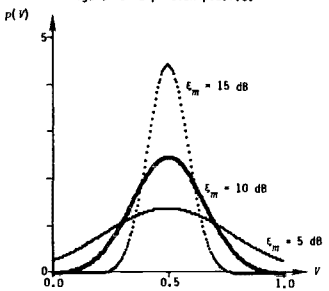

Figure 8. Gaussian-AM p.d.f.s.

$$p(V) = (2\xi_m/\pi)^{1/2} \exp[-2\xi_m(V - 1/2)^2] \quad . \tag{37}$$

The first moment is simply the carrier level; i.e., $\mu_1 = 1/2$. If the areas for $V < 0$ and $V > 1$ are included, the second moment is easily obtained by summing the carrier and modulation powers:

$$\mu_2 = 1/4 + 1/4\xi_m. \tag{38}$$

The RF peak-to-average ratio is therefore related to the modulation peak-to-average ratio by

$$\xi = 4\xi_m/(\xi_m + 1) \quad . \tag{39}$$

Gaussian-AM p.d.f.s for several modulation peak-to-average ratios are shown in Figure 8.

Laplacian AM

Full-carrier amplitude modulation by a Laplacian signal produces an RF signal with a Laplacian-AM envelope. The p.d.f. is, by analogy to (37),

$$p(V) = (2\xi_m)^{1/2} \exp[-2(2\xi_m)^{1/2} |V - 1/2|] \quad . \tag{40}$$

Laplacian-AM p.d.f.s for several modulation peak-to-average ratios are shown in Figure 9. The moments and the relationship between ξ and ξ_m are the same as those for Gaussian AM.

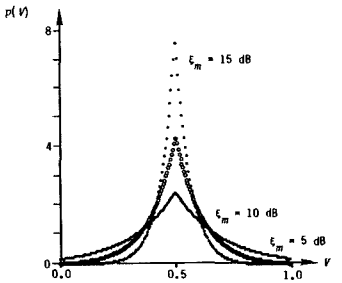

Figure 9. Laplacian-AM p.d.f.s.

PA	V_{eff} / V_{CC}	η_{AVG}			
		CW	TWO-TONE	RAYLEIGH ξ = 10 dB	RAYLEIGH ξ = 20 dB
Class A	1.0	0.500	0.250	0.050	0.005
	0.9	0.450	0.225	0.045	0.004
Class B	1.0	0.785	0.617	0.280	0.089
	0.9	0.707	0.555	0.252	0.080
Class D	1.0	1.000	1.000	1.000	1.000
	0.9	0.900	0.887	0.781	0.530

Table 1. Average efficiencies.

4. AVERAGE-EFFICIENCY CALCULATIONS

The theory and probability-density functions derived in the preceding sections are now used to calculate average-efficiency for several cases of interest. The examples include

- Class-A,
- Class-B, and
- Class-D

power amplifiers, with

- Two-tone test signal,
- Rayleigh-envelope with ξ = 10 dB, and
- Rayleigh-envelope with ξ = 20 dB.

Similar approaches can be used to calculate the average efficiency with other PAs and/or other signals.

The method used here is to relate the average input and output power to the peak-envelope output power. The average output power is independent of the PA and is obtained from (17). The results are summarized in Table 1.

Class A

In class-A PAs, the transistors are biased so that the collector current(s) are positive at all times. The quiescent current (hence dc input current) must therefore be at least as equal to the maximum output current at PEP. In addition, the true supply voltage V_{CC} is reduced to an effective supply voltage V_{eff} by the saturation voltage V_{sat} of the transistor(s). For a

push-pull PA,

$$V_{eff} = V_{CC} - V_{sat} \quad . \tag{41}$$

For a complementary PA, V_{sat} is multiplied by 2. The dc input power and instantaneous efficiency are therefore [1, Chapter 12]

$$P_i = V_{CC}\, I_{omPEP} = \frac{V_{CC}}{V_{eff}} \cdot 2P_{oPEP} \tag{42}$$

and

$$\eta = \frac{V_{eff}}{V_{CC}} \frac{v^2_{om}}{V_{omPEP}} \quad . \tag{43}$$

The parabolic efficiency curve is shown in Figure 1. The effects of FET on resistance can similarly be reduced to a ratio of V_{eff}/V_{DD}.

The dc input current is constant, hence $P_{iAVG} = P_i$. The average efficiency is therefore

$$\eta_{AVG} = \frac{1}{2\xi} \cdot \frac{V_{eff}}{V_{CC}} \quad . \tag{44}$$

Insertion of $\xi = 2$ for the two-tone envelope gives a maximum efficiency of 25 percent, which is reduced by the ratio V_{eff}/V_{CC}. Similarly, signals with Rayleigh envelopes and 10- and 20-dB peak-to-average ratios are amplified by class-A PAs with maximum average efficiencies of 5.0 and 0.5 percent, respectively.

Class B

In class-B PAs, the transistors are biased so that each conducts current for approximately half of the time. The dc input current is $2/\pi$ times the maximum instantaneous output current [1]; the instantaneous efficiency is therefore proportional to output voltage, as shown in Figure 1. As in a class-A PA, saturation voltage produces an effective supply voltage that is lower than the true supply voltage. The instantaneous dc input power is therefore

$$P_i = \frac{4}{\pi} \frac{V_{CC}}{V_{eff}} \frac{V_{om}}{V_{omPEP}} P_{oPEP} \quad . \tag{45}$$

The ratio V_{om}/V_{omPEP} is the normalized output voltage V defined in (11) and used throughout this paper. Consequently,

$$P_{iAVG} = \frac{4}{\pi} \frac{V_{CC}}{V_{eff}} \mu_1 P_{oPEP} \tag{46}$$

and

$$\eta_{AVG} = \frac{4}{\pi \mu_1 \xi} \cdot \frac{V_{eff}}{V_{CC}} \quad . \tag{47}$$

Substitution of μ_1 and ξ for the two-tone signal yields

$$\eta_{AVG,Two\text{-}Tone} = \frac{\pi^2}{16}\frac{V_{eff}}{V_{CC}} \approx 0.617\,\frac{V_{eff}}{V_{CC}} \quad . \tag{48}$$

A substitution from (30) for the Rayleigh envelope similarly yields

$$\eta_{AVG,Rayleigh} = \left(\frac{\pi}{4\xi}\right)^{1/2} \cdot \frac{V_{eff}}{V_{CC}} \quad . \tag{49}$$

For peak-to-average ratios of 10 and 20 dB, the average efficiencies of an ideal class-B PA ($V_{sat} = 0$) are only 28 and 8.9 percent, respectively. While these represent considerable improvements over those of the class-A PA, they are nonetheless considerably smaller than the 78.5-percent efficiency at PEP.

Class D

Class-D PAs employ a pair of transistors that are driven to switch at the carrier frequency [1], followed by a series-tuned tank circuit to produce a sinusoidal output. The efficiency of an ideal class-D PA is 100 percent; however, saturation voltage, saturation resistance, and charging of the collector or drain capacitance reduce the efficiency.

The power expended in charging linear shunt capacitance is proportional to the output power and therefore reduces both PEP and average efficiencies by the same factor. The power required to charge voltage-dependent capacitance results in a power-input function [13] that must be averaged numerically.

The supply voltage of a class-D PA must be varied to produce amplitude-modulated RF signals. The effects of the BJT saturation-voltage drop are overcome by increasing the modulator output at all levels by a fixed voltage. The instantaneous input power of an amplitude-modulated class-D PA is therefore

$$P_i = P_o + \frac{2V_{sat}\,V_{om}}{\pi R} \quad , \tag{50}$$

hence its instantaneous efficiency is

$$\eta = \frac{V_{om}}{V_{om} + (4/\pi)V_{sat}} \quad . \tag{51}$$

It is convenient to rewrite the instantaneous input power as

$$P_i = P_o + \varepsilon\, V\, P_{oPEP} \quad , \tag{52}$$

where

$$\varepsilon = \begin{cases} V_{sat} \,/\, V_{eff PEP}, & \text{push-pull PA} \\ 2V_{sat} \,/\, V_{eff PEP}, & \text{complementary PA} \end{cases} \tag{53}$$

represents the saturation-power-loss factor. The average input power is then

$$P_{iAVG} = P_{oAVG} + \varepsilon\,\nu_1\,P_{oPEP} \quad , \tag{54}$$

and the average efficiency is

$$\eta_{AVG} = \frac{1}{1 + s\,\mu_1\,\xi} \quad . \tag{55}$$

Substitution of μ_1 and ξ for the two-tone envelope yields

$$\eta_{AVG,Two\text{-}tone} = \frac{1}{1 + (4/\pi)s} \quad , \tag{56}$$

hence $\eta_{AVG} = 0.887$ for $s = 0.1$. Substitution of μ_1 from (30) yields

$$\eta_{AVG,Rayleigh} = \frac{1}{1 + s(\pi\,\xi/4)^{1/2}} \tag{57}$$

for Rayleigh-envelope signals, hence average efficiencies of 0.781 and 0.530 for $s = 0.1$ and $\xi = 10$ and 20 dB, respectively. These efficiencies represent considerable improvements over those of class-B PAs.

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A 405 MHz Phased Array Antenna for Atmospheric Wind Measurement

by

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The Wave Propagation Laboratory has completed the design and construction of a phased array antenna for use at 405 MHz for atmospheric wind profiling. The steering geometry of the sequentially switched beams is shown in Fig. 1. Transmitted signals are backscattered by temperature or moisture related gradients in the radio refractive index of scales equal to one-half the transmitted wavelength. These signals are Doppler processed to extract radial air mass velocities. The measurement geometry of Fig. 1 allow horizontal velocities at heights up to 15 kilometers to be calculated. These radars are known as Wind Profiling Radars.

The 126 5-element Yagi-Uda antennas are arranged on a square grid whose axes are 45° with respect to the cardinal steering directions. For a given steering angle this arrangement allows element spacing $\sqrt{2}$ larger than that required for a broadside steered array. This feature helps minimize element interaction and reduces the number of elements required to populate a given aperture. This geometry is shown in Fig. 2.

By constraining the phase difference between rows of identically phased elements to an even, integral sub-multiple of 360°, symmetries appear in the phasing maps which reduce the switching hardware. In this design, the element spacing $\sqrt{2}$ X in Fig. 2, is .91λ and Δφ is 60° resulting in an oblique beam direction of 15° from vertical. Only 15 RF coaxial transfer switches are used to synthesize the required 18 phase combinations for North, East, South, and West steering. These 18 signals are labeled A through R in Fig. 3.

The vertical beam is generated by switching around the four beam circuitry of Fig. 3 resulting in identical phasing on all of the elements. Requiring 36 RF coaxial SPDT switches, the vertical beam is more expensive than the four cardinal beams.

After the 18 signals are synthesized they are split and distributed about the array while maintaining proper phasing because of the symmetries. Uneven power splitter/combiners are used for amplitude tapering. A schematic of the whole antenna is shown in Fig. 4, and a map of the quasi-circular array of Fig. 5 shows the placement of 7 each of the 18 phases.

Computer simulations were employed in the design process. For any position in spherical coordinate space the radiation pattern of an array of isotropic radiators may be calculated from the Equation: [Tang & Burns, 1984]

$$E(\cos\alpha_x, \cos\alpha_y) = \sum_{m=0}^{M-1} \sum_{n=0}^{N-1} A_{mn} e^{j2\pi\left(\frac{\phi mn}{360} + md_x \cos\alpha_x + nd_y \cos\alpha_y\right)}$$

This "array factor" pattern is multiplied by the pattern of the individual Yagi elements to obtain the antenna pattern of the phased array. This pattern was projected into X-Y planar coordinates and processed for display on a color graphics workstation. These simulations allowed optimization of element spacing, phasing, and amplitude tapering. These calculations were repeated after the array was constructed using amplitudes and phases measured on each of the 126 elements. The measured patterns are shown in Fig. 6.

Table 1 summarizes the antenna characteristics.

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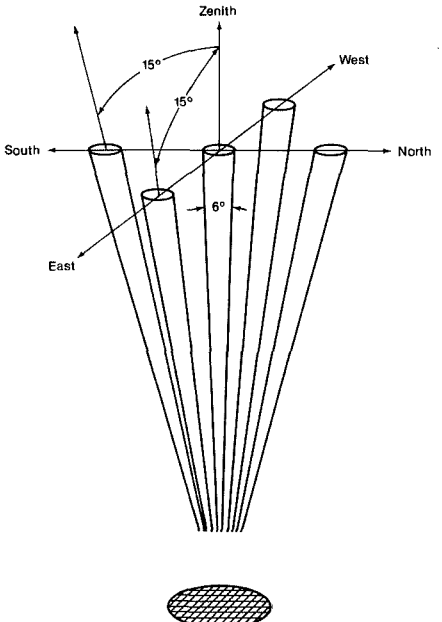
405 MHz Phased Array Antenna

Number of steering directions:	5
Oblique beam directions:	4
Azimuth:	0°, 90°, 180°, 270°
Elevation:	75°
Gain:	30 dBi
One-way 3 dB beamwidth:	6°
Effective aperture:	44 m^2
Peak power:	60,000 w
Average power:	6,000 w
Technology:	126 5-element Yagi-Uda radiators 31 R.F. coaxial switches with indicators 1 1:18 high power reactive splitter/combiner 18 1:7 uneven reactive splitter/combiners low loss foam distribution cables

Table 1



405 MHz PHASED ARRAY

FIG 1

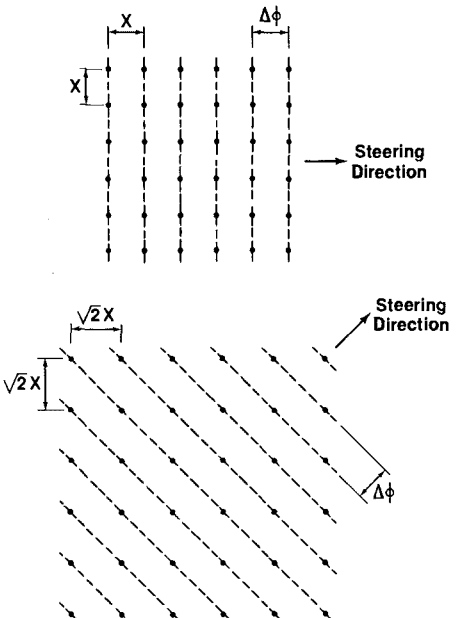
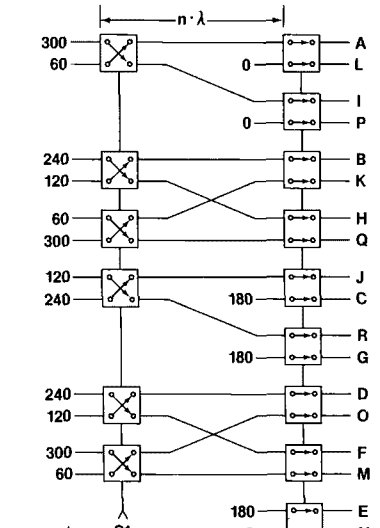
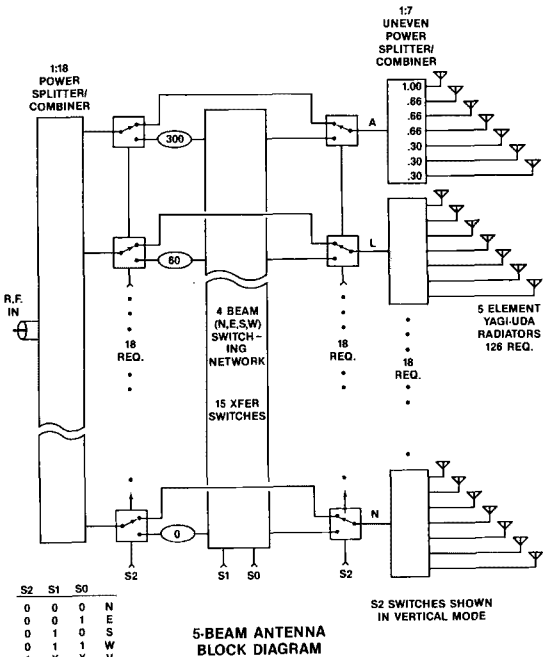


FIG 2



4 BEAM SWITCHING
(SOUTH PHASING POSITIONS)

FIG 3



5-BEAM ANTENNA
BLOCK DIAGRAM

FIG 4

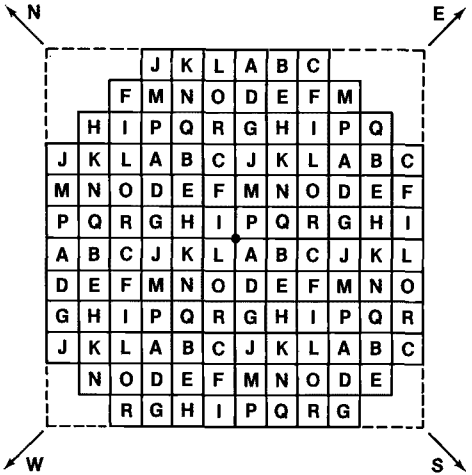
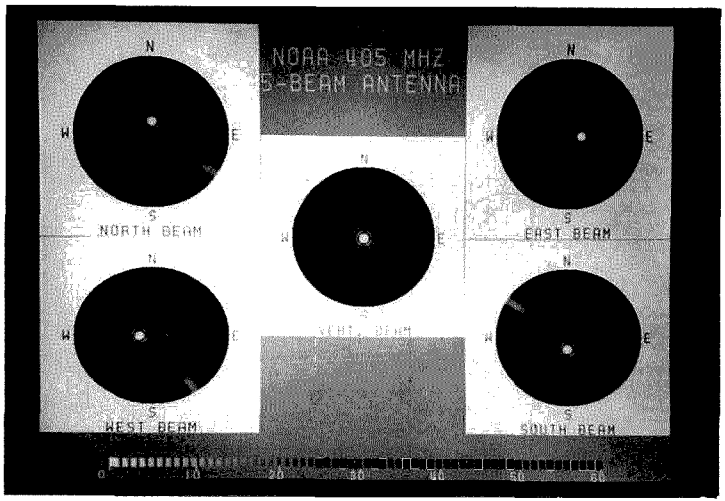

N
E
W
S
J K L A B C
F M N O D E F M
H I P Q R G H I P Q
J K L A B C J K L A B C
M N O D E F M N O D E F
P Q R G H I P Q R G H I
A B C J K L A B C J K L
D E F M N O D E F M N O
G H I P Q R G H I P Q R
J K L A B C J K L A B C
N O D E F M N O D E
R G H I P Q R G

FIG 5


NOAA 405 MHZ
5-BEAM ANTENNA
NORTH BEAM
EAST BEAM
WEST BEAM
SOUTH BEAM
0
10
20
30
40
50
60

Practical Considerations for Modulating or Pulling The Frequency of a Quartz Crystal Oscillator

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ABSTRACT

The quartz crystal for frequency control is a high Q device. This is another way of saying it doesn't like to have its natural frequency changed by external influences. Yet this is exactly what is attempted in voltage controlled crystal oscillators (VCXO's) or frequency modulated crystal oscillators.

There are parameters in both the oscillator circuit and the cyrstal that must be considered when designing a pullable oscillator. This paper will point out these parameters and try to tell the circuit designer how best to use them.

INTRODUCTION

Two factors must be considered in designing a pullable crystal oscillator. The first is the frequency deviation required and the second the linearity of the deviation. The frequency deviation is generally expressed as parts per million of the operating frequency or total Hertz from nominal frequency. The linearity can be described as the deviation from a straight line of the frequency curve versus the parameter that is controlling it. A secondary effect of the linearity is the amount the frequency is changed in either direction from some center frequency. Examples of this are shown in Figure 1A and 1B.

The oscillator circuit as well as the crystal is important in the control of these two factors. So let's first look at the oscillator circuit design.

THE OSCILLATOR CIRCUIT

I've selected the Pierce Oscillator Circuit because it is the easiest to explain and the most tolerant of errors. The basic circuit is as shown in Figure 2.

In this circuit the collector to emitter (Cce) and base to emitter (Cbe) capacitances are necessary to sustain oscillation. However, their capacitances are very temperature dependent, are not controlled by the manufacturer, and are resistive. Therefore, the performance of the circuit in Figure 2 is marginal. We can improve the performance greatly by placing fixed capacitors in parallel with these junction capacitances. The new Pierce Oscillator will now be as shown in Figure 3.

Resistors R1, R2 and Re provide for the DC bias of the transistor. Re raises the emitter off of ground potential which improves the linearity. Ce bypasses the emitter which must be at RF ground.

We can now replace the transistor with its small signal equivalent circuit. The Pierce oscillator will now appear as in Figure 4.

To simplify the circuit a few assumption can be made. First is that R1 // R2 >> hie and 1/hoe // R_L >> XC2. The simplified circuit now appears as in Figure 5.

For the circuit to oscillate, Barkhausen's criteria for oscillation must

be met. Barkhausen states that the product of the gains around the loop must be greater than or equal to one. He also states that the phase shift around the loop, at the frequency of oscillation be n(360°) whenn is any integer.

To analyze this further, let's remove the crystal and look into the two terminals that it is connected to. We see this as a two terminal circuit shown in Figure 6.

The impedance seen, looking into the crystal terminals A and B, is a negative resistance (-e) and an equivalent capacitance (C_t) which is the series combination of C_1 and C_2. We can draw this new circuit as shown in Figrue 7.

We now put the crystal back and we have the circuit shown in Figure 8.

A negative resistance corresponds to a gain. Assuming |e| > crystal resistance, then the first constant of Barkhausen's Criteria is met. In order to have the phase shift around the loop be n(360°) the crystal must be inductive to cancel the effect of C_t.

Oscillation starts by the noise generated in the transistor. This noise is fed back to the input of the transistor, in phase, and is further amplified. The crystal, which is in the feedback path, acts as a very narrow band pass filter. The filter allows only the noise to be fed back that is in the pass band of the crystal and controls the frequency of oscillation. This is the natural crystal frequency using C_t as a load.

THE CRYSTAL CIRCUIT

The equivalent circuit of the crystal in the feedback loop is shown in Figure 9, with the formulas for series resonance and parallel resonance added.

The plot of reactance vs. frequency for the fundamental mode is shown in Figure 10. Since the crystal operates inductively in the oscillator circuit, it's reactance would be somewhere between fr and fa.

Pullability and linearity are increased if we operate the crystal at close to series resonance. A good way to do this is to tune out Co with an inductor an add another inductor in series. The revised crystal equivalent circuit would then appear as in Figure 11. If we now plot the reactance vs. frequency curve it would look like Figure 12. Fa has been pulled further away from Fr which allows for more pullability along the inductive region of the curve.

Most crystals are pulled by a capacitor in series with the crystal. This is usually a varactor that can be varied by an external voltage as shown in Figure 13. As the capacitor gets smaller, the frequency of the crystal is shifted upward towards Fa.

The frequency from resonance may be calculated from the equation:

$$D = \frac{C_m \times 10^6}{2(C_o + C_L)} \quad \text{parts per million}$$

The pulling sensitivity can be calculated from the equation:

$$S = \frac{-C_m \times 10^{-6}}{2(C_o + C_L)^2} \quad \text{ppm/pf}$$

Another useful equation is:

$$fa - fs \cong \frac{fr}{2 C_o C_m \frac{C_o}{C_m}} = fs$$

Note the use of the $\frac{C_o}{C_m}$ ratio. This is a popular expression used by the crystal industry. You want this ratio to be as low as possible to get

the greatest pullability. Typical values of this ratio for quartz crystals are 250 for fundamental mode crystals, 2500 for third overtones and 6500 for fifth overtones.

SUMMARY

We have seen how the crystal and oscillator interface and how one affects the other. The circuit should have ample gain to make certain that it oscillates when the crystal is operated in its reactive or inductive mode. The more the crystal is pulled away from series resonance, the higher is the reactance of the crystal.

For best linearity, and greatest pullability, the circuit should tune out the Co or shunt capacity of the crystal. This can be done with an inductor that resonates with Co at the series resonant frequency of the crystal.

The Co/Cm ration should be as low as possible. For greatest pullability, fundamental mode crystals should be specified. Generally, frequencies in the 8 to 25 Mhz range are preferred.

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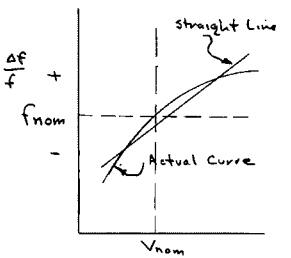
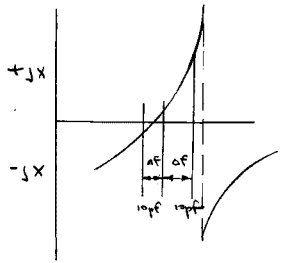


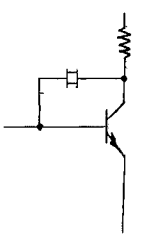
Voltage or Control Parameter

FIG. 1A



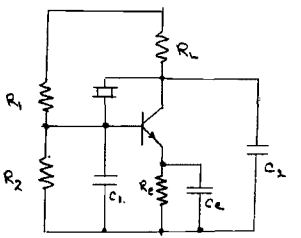
Difference in Pulling Range

FIG. 1B



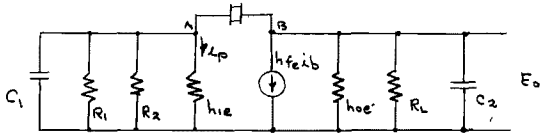
Basic Pierce Oscillator

FIG. 2



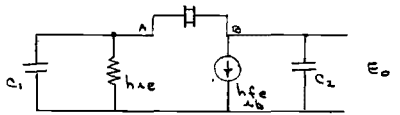
Complete Pierce Oscillator

FIG. 3



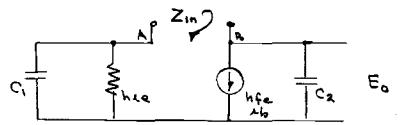
Small Signal Equivalent Circuit

FIG. 4



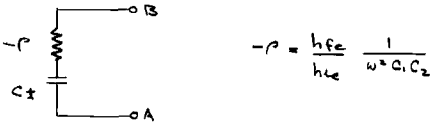
simplified Equivalent Circuit

FIG. 5



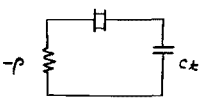
Measuring Zin

FIG. 6



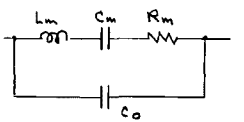
Circuit Further Simplified

FIG. 7



Pierce Oscillator Reduced to Basics

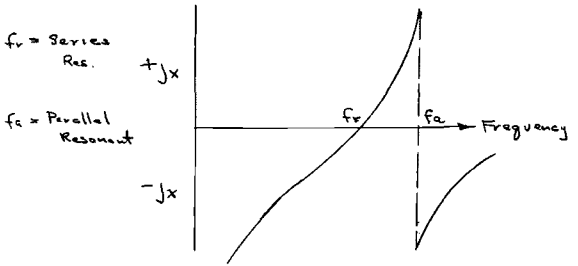
FIG. 8



$f_r = \frac{1}{2\pi \sqrt{L_m C_m}}$ $f_a = \frac{1}{2\pi \sqrt{L_m \frac{C_m C_o}{C_m + C_o}}}$

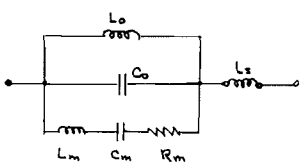
Crystal Equivalent Circuit

FIG. 9



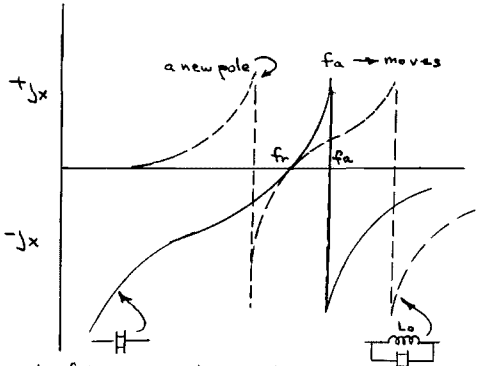
Crystal Reactance Graph vs Frequency

FIG. 10



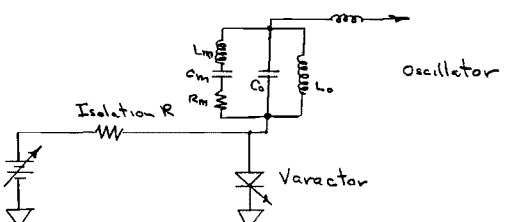
Crystal Equivalent Circuit with added inductances Lo and Ls

FIG. 11



Effect of Lo on Crystal Reactance Graph

FIG. 12



Voltage Controlled Oscillator

FIG. 13

S-BAND BUTLER MATRIX FEED NETWORK

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A B S T R A C T

This paper presents the development of a compact microstrip Butler Feed Network at S-band for an eight element linear array. The feed network is developed on a high dielectric constant soft substrate incorporating the entire feed network on a 10" x 10" sheet. The network features the incorporation of broad band hybrids and phase shifters.

I N T R O D U C T I O N:

Butler Matrix (1, 2, 3, 4) is a passive and theoretically lossless feeding network. This network feeds an array antenna with uniform distribution and constant phase difference between elements. This matrix consists of N inputs and an equal number of output ports. A signal introduced at one input produces equal amplitude excitation at all outputs but with a constant phase different between them, resulting in radiation at a certain angle in space. If the signal is introduced at an other input we will get the radiation at a different angle from the first one.

The network consists of 3 dB hybrids with phase delays in the interconnecting lines. The network has $N = 2^n$ inputs and an equal number of output ports, where n is an integer.

A sketch of an 8 element Butler Matrix is shown in Fig.1. Initially a single piece of broad band coupler and a single piece of broad band phase shifters of values 22.5° 45° and 67.5° were fabricated, tested and optimized before integerating the whole layout. This S-band Butler Feed Network was designed at centre frequency 2.15 GHz with 300 MHz bandwidth on R.T. Duriod 6010.5 0.05 (Er = + 10.5 $\pm$ .25). The measured results obtained were close to theoretical values. This network was also fed to an eight element microstrip linear array to compare the theoretical and practical performance of the beam direction.

Development of Butler Feed Network

The eight element Butler Feed Network without any crossovers is shown in Fig.2. Eight terminals are in middle and the other eight terminals are located on the four sides as shown in Fig.2. The substrate can be grooved in the middle for connections from the sides. We can put the connectors at the back also to avoid grooves in the middle. We can see that the outputs of antenna ports are in horizontal line end the inputs or beam ports are in the vertical line. The 3 dB 90° hybrid was made broadband using G.P. Riblet s(5) technique. The output characteristics, isolation and return loss of this coupler are shown in Fig.3 and Fig.4 respectively.

The phase response of this coupler is shown in Fig.5. A broad band phase shifter was designed on the basis of techniques given by Darko Kajfez(6). One-piece phase shifters of value 22.5°, 45° and 67.5° were fabricated and tested. Their response are shown in Figures (6), (7), and (8). We can see that in the case of the coupler the imbalance is within 0.3 dB throughout the frequency band. The phase is also within 92°, with slightly more variation in the lower side of the frequency. The isolation and the return loss are greater than 25 dB throughout the band. The variation of the phase values in 67.5°, 45° and 22.5° phase shifters in the 300 MHz band are ± 0.5° ± 1.5° ± 3°. The actual layout of the coupler and phase shifter is shown in Fig.9(a) and 9(b). Using the coupler and phase shifters a compact integrated layout was made to fit within 10" x 10" sheet of R.T. Duroid 6010.5 dielectric. The layout is shown in Fig.(10).

Experimental Results on Butler Feed Network

The S-band Butler Feed network connected to the eight element microstrip linear array is shown in the photograph. The photograph also shows the far field pattern of this antenna fed by the Butler Matrix. Connectors to the eight inputs and eight outputs are made from the bottom.

The insertion loss of the matrix is of the order of 2.0 dB. The matrix provides a uniform illumination of the array. However, variations in the coupling ratios of the 90° hybrid couplers and difference in the insertion loss between the reference line and coupled lines of the phase shifter cause amplitude errors in the illuminations. The worst amplitude error is 1.8 dB. Phase errors in the array illuminations average ± 6° for all beams. The maximum phase variation is 12°. The return loss of input port 3L is given in Fig.11. In the 300 MHz band the average return loss is 22dB. The average isolation is 25 dB with the lowest value of 18 dB. The antenna terminals of the matrix are isolated from each other in the same manner. The average isolation is 23 dB.

POSITION OF BEAM PEAKS

We know that the normalized magnitude of the field intensity in the far field of a linear array of a isotropic sources is given by

$$|E| = \frac{\mathrm{Sin}(n\psi/2)}{n \times \mathrm{Sin}(\psi/2)}$$

where $\psi = \frac{2\pi d}{\lambda} \mathrm{Sin}(\alpha) - \delta$

d = element spacing = 0.52λ in our case

λ = Wave length

α = angle from the array normal

and δ = element to element phase shift $= \frac{(2p-1)}{n} \frac{\pi}{2}$

p = beam numbers = $\pm$ 1, $\pm$ 2, $\pm$3, and $\pm$ 4 (in our case)
i.e. the position of the beam peaks are given by

$$\sin^{-1}\left(\frac{\lambda}{n\,d} \left(nq + p - 1/2 \right) \right)$$

The theoretical beam angles are 7°, 21°, 37°, and 57°on each side from the broad side direction.

The position of the main beam is shown in the Fig.12 which is very close to the predicted value. We also see that beam cross-over level is about -3dB which is also close to theoretical value -3.86 dB. The small variation may be due to deviation from the uniform illumination.

The first side level is -12.5 dB compared to -13.2 dB. The difference is due to error in phase values from the theoretical phases in the outputs.

CONCLUSIONS

This feed network can work well up to 300 MHz about the 2.15 GHz centre frequency. The response of the feed networks deviate a bit at the band edges due to increased amplitude imbalance and deviation of phase from 90° between the outputs of the coupler. The phase shifter also introduces phase error, though small at band edges. Slight phase error was also introduced while mounting the connectors. Taking proper care in development and mounting, the everage insertion loss and the phase variation can still be reduced from 2.2 dB and $\pm$ 6°. The band width of the matrix can be still further increased to 500 MHz by increasing the bandwidth of the coupler. The designed phase shifters can work well upto 500 MHz about 2.15 GHz.

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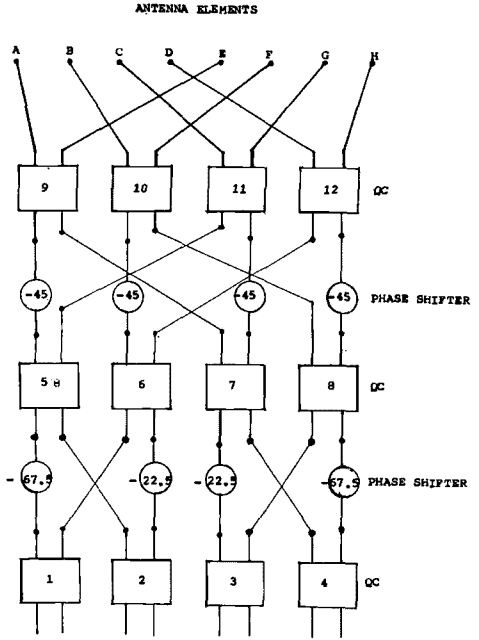


Fig.1 Eight element Butler beam forming matrix

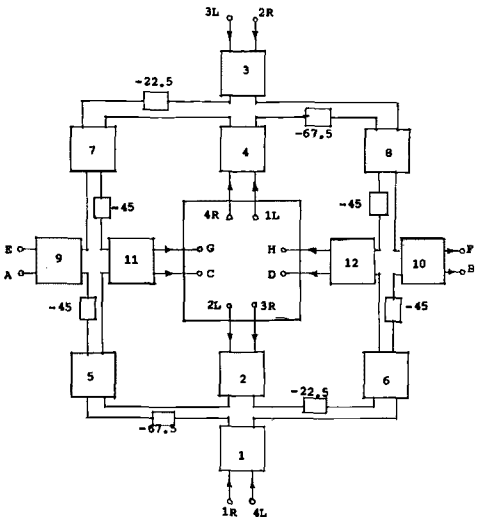


Fig.2 Butler Feed Network without Cross-overs

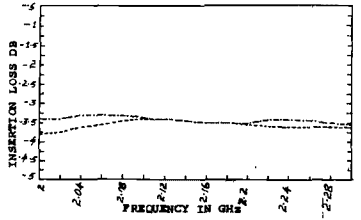


FIG.3 RESPONSE OF COUPLED AND DIRECT PORTS OF BROADBAND COUPLER

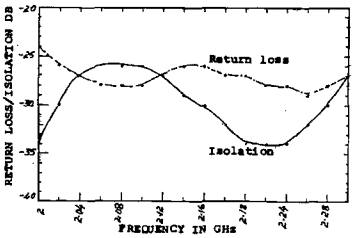


FIG.4 RESPONSE OF ISOLATION AND RETURN LOSS OF BROADBAND COUPLER

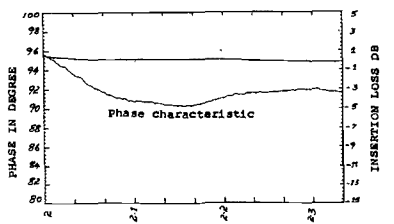
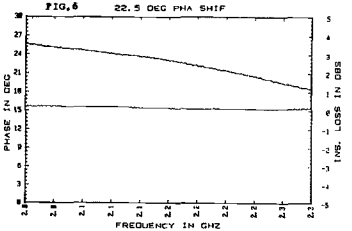
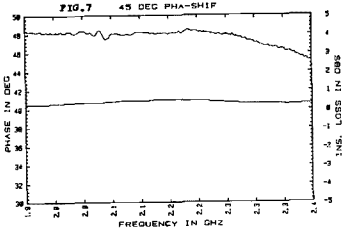
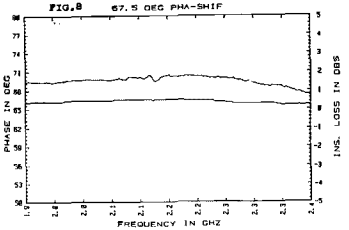


FIG.5 RESPONSE OF PHASE AND I/L OF 3 DB COUPLER







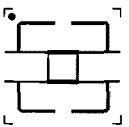


FIG.9(a) 3 dB BROAD BAND COUPLER

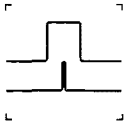


FIG.9(b) 67.5° PHASE SHIFTE

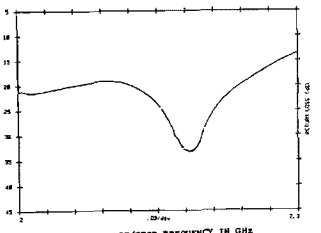


FIG.11 RESPONSE OF R/L AT 3L I/P PORT

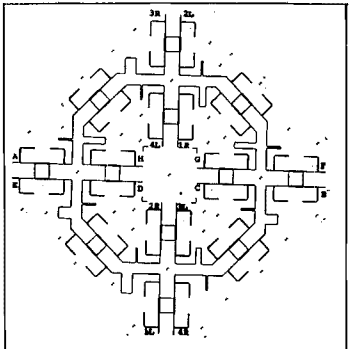


Fig.10 Actual integrated layout of Butler Feed Network for 8 element linear array.

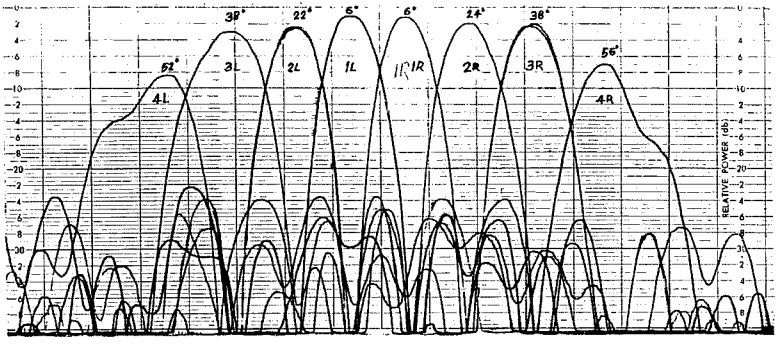
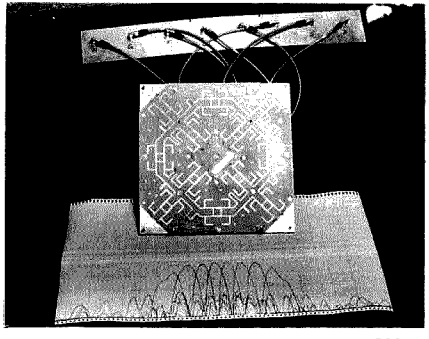
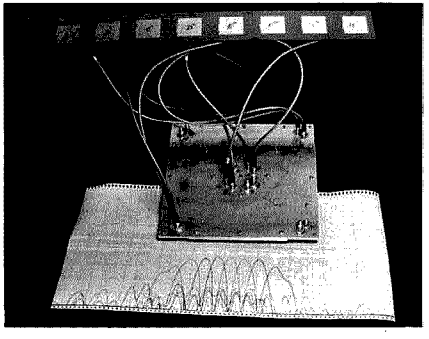


FIG.12 MAJOR AND MINOR LOBES OF ALL EIGHT BEAMS





P.C.MOUNTABLE MINIATURE HELICAL FILTER

by

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A B S T R A C T

This paper presents the development of a miniature P C board mountable helical filter in the VHF/UHF range. The specific development was for application in a space-borne S-Band transponder. The unit size is 45x14x14 mm^3 having a 3 pole Butterworth response, giving an insertion loss of about 1.5 dB with 0.5 dB flatness of about 10 MHz and 50 dB rejection bandwidth of 150 MHz at fo = 375 MHz. This unit is tunable from 250 MHz to 400 MHz and weighs approximately 25 gms.

INTRODUCTION: In the VHF/UHF range helical resonators can be extensively used where high Q and practical size is realisable compared to other conventional types. The helix is enclosed in a highly conductive shield of square cross section. One end of the helix is grounded and the other is left open.

DESIGN CRITERIA: The main aim of this design is to realise a unit miniature in size and yet reliable.

Size reduction has been achieved primarily by the following methods:

a) By optimising the volume of the rectangular cavity and coil size.

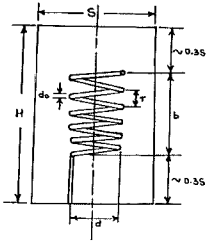
b) Eliminating input/output RF connectors by using P C solderable R F feed-through pins.

c) By using an alignment procedure which can obviate the need of tuning screws.

DESIGN REQUIREMENTS: The following specifications need to be realised.

fo	=	375 MHz
BW_{1dB}	=	17 MHz
BW 50dB	=	150 MHz

Design:- Helical Resonator with square cross section:



H = Height of the cavity in inches

S = Length of one side of the square

d = The mean diameter of coil in inches

b = Height of coil in inches

do= diameter of wire in inches

T = Pitch of the winding in inches.

The following set of equations are given with these notations for a square cross section (1)

Table - 1

1) Qun = $60s\sqrt{fo}$

2) N = $\frac{1600}{S.fo}$ the number of turns

3) n = $\frac{1}{t} = \frac{1600}{s^2 fo}$ the number of turns per inch

4) d = 0.66S for $\frac{d}{1.2S} = 0.55$

5) b = S for $\frac{b}{d} = 1.5$

6) H = 1.6S

It is found that a 3-pole Butterworth filter will satisfy the requirements.

Next Qmin = qmin $\frac{fo}{BW\ 3dB}$ = 37.5

In order to have high Q, the Qun > 10 Qmin

∴ Qun should be at least 375

By using the set of equations in Table 1 and taking into consideration the fabrication difficulties involved, and also keeping in view miniaturisation without deviating much from the electrical specification requirements, the following dimensions are arrived at for practical purposes.

H = 11.7 mm / S = 14 mm / d = 8.5 mm / b = 6 mm/

N = 6.5 turns approx. / n = 32 TPI / T = 0.8mm/

do = 0.3mm approx.

The insertion loss is calculated by I.L. = 20 log $\frac{U}{U-1}$

Where U = $\frac{Qunloaded}{Qminimum}$

In this case, Qun = 375 at least.

Qmin = $\frac{375}{10}$ ∴ I.L. = 20 log $\frac{10}{10-1}$ = 1 dB approx.

The input and output of the resonator are through loops of less than a turn of 22 SWG wire and are placed perpendicular to the helix on the last turn such that loose coupling is maintained.

CONSTRUCTION:- The formers are made of Teflon in which square threads are cut to accomodate the helix coil of 30 SWG enameled copper wire. One end of the coil is grounded and the other is left open. The loops are made from 22 SWG wire. The helix and loops are bonded with

Epotek H-54 low loss dielectric compound. The entire cavity is soldered along the sides to the base plate after tuning is completed. Then, the entire unit is conformally coated to prevent any seepage of alcohol during further P.C. card assembly operations, cleaning, etc. The mechanical configuration is shown in Fig.1.

ALIGNMENT PROCEDURE:

The filter is aligned using return loss phase characteristics.

Initially all resonators are short circuited, including the output port. Initial phase reference is noted. Each resonator is tuned sequentially by closely changing the number of turns to achieve resonance of each resonator.

RESULTS:- The filter response showing the transmission and return loss characteristics, is shown in Fig.2 & Fig.3. Measured insertion loss is about 1.5 dB, weight 22 gms, size $45 \times 14 \times 14$ mm^3.

CONCLUSIONS:

1) The same configuration holds good for different frequencies in the range 250 MHz to 400 MHz, and with a slight increase in cavity and resonator height it can be made even up to 150 MHz.

2) This filter has passed rigorous tests according to MIL-STD-202F.

3) This has been used in an S-Band TTC Transponder aboard Indian remote sensing satellites, etc.

ACKNOWLEDGEMENT:

We sincerely acknowledge the encouragement provided by COL. N. PANT, DIRECTOR, ISRO SATELLITE CENTRE, BANGALORE, for this work. Also sincere thanks are due to Mr. U. PRABHAKARAN and to Mr. R. RAMASUBRAMANYAM for useful comments.

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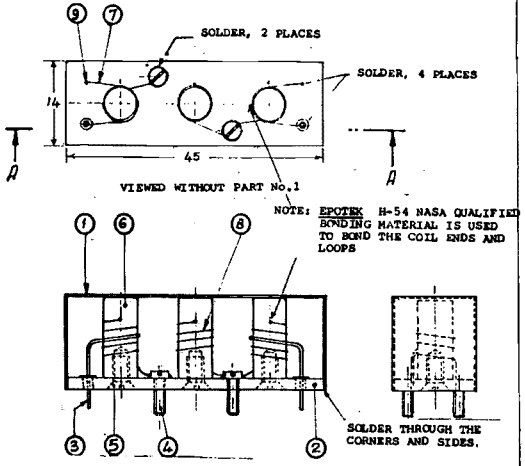


SECTION AT 'A-A'

Part	Qty	Description	Matl.	Remarks
1	1	CAVITY BODY	COPPER	SILVER PLATED
2	1	BOTTOM PLATE	COPPER	SILVER PLATED
3	2	RF FEED THROUGH (GLASS)		
4	2	M2 x 8 CHEESE HEAD SCREW	BRASS	SILVER PLATED
5	3	M3 x 6 C/SK SCREWS	BRASS	SILVER PLATED
6	3	TEFLON FORMER	TEFLON	
7	-	ENAMELLED COPPER WIRE	COPPER	22 SWG
8	-	ENAMELLED COPPER WIRE	COPPER	30 SWG
9	2	GROUNDING PINS		SILVER PLATED

F I G . 1 MECHANICAL DETAILS

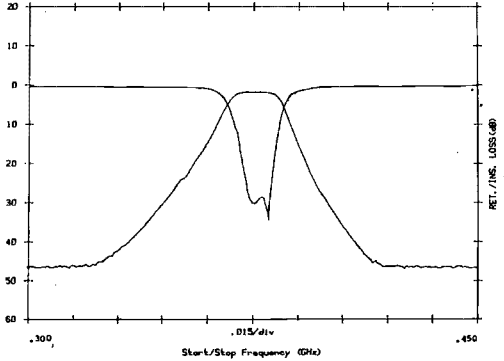
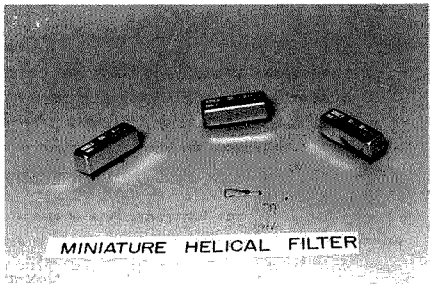


FIG.2 TRANSMISSION/REFLECTION CHARACTERISTICS AT 375 MHz



S-BAND HIGH PERFORMANCE COMBLINE FILTER

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A B S T R A C T

This paper presents the development of an improved high performance combline filter at S-band for input/out applications of a transponder. The unit features reduced size and weight optimised with a minimum number of elements resulting in the following characteristics:

Type : Eight pole Chebyschev 0.1 dB ripple.
Rejection B.W. : $f_o \pm$ 180 MHz - 110 dB
I.L. : 1.0 dB
Ripple B.W. : 100 MHz
Sizes : 183 x 37 x 60mm
Weight : 165 GMS.

The unit is tunable from 2 to 2.4 GHz. The unit is qualified for space borne applications for 1 Watt RF power through low pressure to vaccum.

INTRODUCTION:

A high performance combline filter has been developed at S-band for applications in spacecraft telemetry. The unit features light weight, high rejection on the order of 100 dB and 40 dB down spurious response up to 18 GHz. The unit was tested for 1 Watt RF power from low pressure to vacuum. It was found to be free from RF discharges like corona and multipacting. The unit can be tuned easily to any frequency in the band 2 to 2.4 GHz used for spacecraft telemetry. The filter was constructed from two milled pieces of aluminium joined with screws. This construction makes the unit rugged enough to withstand the severe vibrational requirements of a launch pad. The thermal drift of this unit from 0 to 50°C is less than 5 MHz. A special surface polishing technique was developed to give a bright mirror-like surface finish to the aluminium blocks. This improved the RF conductivity of the surface and brought down the insertion loss to less than 1 dB.

D E S I G N:

The electrical circuit of the combline filter is shown in Fig.1. The circuit consists of coupled transmission lines of electrical length θ shorted at one end and loaded by a lumped capacitor at the other end. These coupled transmission lines are characterised by the self impedance of each resonator, Ci, and mutual capacitance of each resonator with its nearest

neighbours, Cij. The values of Cij were calculated from the prototype given by Mathaie et.al (1). Finally, the physical parameters of the coupled lines were calculated using graphs provided by (2).

The prototype filter along with its element values are given in Fig.2. The value of self impedance and mutual impedance of each resonator is calculated using Mathaie's formule (1). The terminating impedance is a=50,ohms impedance of each resonator is taken as 75 ohms and electrical length θ = pie/4. This gave the value of self and mutual capacitance as:

Self Capacitances	Mutual Capacitance
C0 = C9 = 6.175	C1 = C89 = 1.358
C1 = C8 = 3.764	C12 =C78 = 0.223
C2 = C7 = 4.710	C23 =C67 = 0.167
C3 = C6 = 4.775	C34 =C56 = 0.158
C4 = C5 = 4.786	C45 = 0.156

Finally, reactangular bars were used to construct the coupled line structure. Ground plane spacing was taken as 15mm. and t/b value was taken as 0.3. The cross section of the structure is given in Fig.3. The value of w/b and s/b were calculated using the data given (2). The lumped capacitance, Cs, was realised using a parallel plate capacitor with air as the dielectric. The physical dimensions of the capacitor were calculated using the formula:

$$C_s = \epsilon A/d$$

where A = Area of the plate

d = Separation between them

MECHANICAL FABRICATION AND SURFACE POLISHING

The filter was fabricated in two pieces. One piece consists of transmission lines coupled with one plate of the capacitance. The other piece is a cover which forms the two ground planes for the coupled lines and a ground plane for the lumped capacitance. Both pieces were milled from blocks of aluminium. They were joined to each other using M-3 screws. The launching pieces which couple the electrical energy into the combline structure were fabricated separately and fixed to the cover plate using M-2 steel screws. The structures were chemically polished. The attached photographs show the internal construction and assembly of the filter.

FILTER ALIGNMENT AND TESTING:

The centre frequency of the filter can be tuned to the desired value by adjusting the resonant frequency of the resonators. Since for a small range of tuning frequency the coupling is indepedent of frequency, the pass band will not get distorted by tuning. Each resonator centre frequency is tuned to the desired value by varying the capacitance, Cs. This is achieved by a tuning screw fixed on the cover plate, one for

for each resonator. The resonators were brought to the desired frequency by monitoring the phase of the input impedance of the filter on a network analyzer. However, minor adjustments on the launcher position give good return loss as the filter is tuned to different frequencies. The responses are shown in Fig.4. Also, the unit was tested up to 2 Watts in vacuum for power handling capability. No increase in insertion loss was observed throughout the vacuum range from atmosphere to hard vacuum.

RESULTS:

The insertion loss of the filters was measured on the network analyzer and found to be 0.9 dB. The rejection at ± 180 MHz away from the centre frequency was measured using a high power source and spectrum analyzer. The measured isolation was 110 dB. The return loss at the desired band was 20 dB. The overall size is 168 x 32 x 30 mm and the measured weight is 165 gms. The photo of the filter along with a similar filter provided by M/s.Delta Microwave for a similar application is given. It can be seen that a substantial reduction in overall size and weight has been achieved. The unit is found to be free from RF discharges like corona and multipacting in the vacuum range starting from atmospheric to hard vacuum for all the required operational power levels.

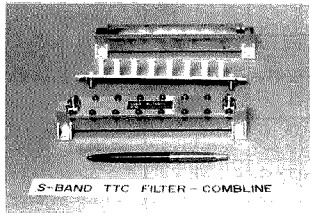
ACKNOWLEDGEMENT

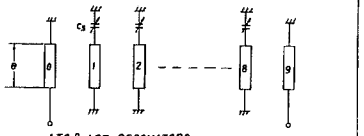
We sincerely acknowledge the encouragement provided by Col, N.Pant, Director, I.S.R.O. Satellite Centre, Bangalore, for this work. Also, sincere thanks are due to Shri.Seetharaman and Ramasubramaniam for useful comments. We are also thankful to Shri.C.Suresh of P.C.B. Lab for his help in chemical polishing of the filter.

REFERENCES:

1. Microwave filters impedance matching networks and coupling structures by G.L.Mathaei, Leo Yong and E.M.T. Jones.

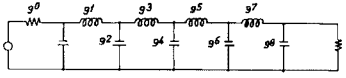
2. Coupled rectangular bars between parallel plates by W.J.Getsinger, I.R.E. Trans on M T T Jan-1962 p -65-72.





1 TO 8 ARE RESONATORS
0 AND 9 ARE LAUNCHERS

FIG.1



g0 = 1.0000
g1 = 1.1897, g2 = 1.4346, g3 = 2.1199, g4 = 1.6010, g5 = 2.1699
g6 = 1.5640, g7 = 1.9444, g8 = 0.8778, g9 = 1.3554.

FIG.2

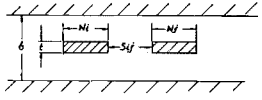


FIG.3

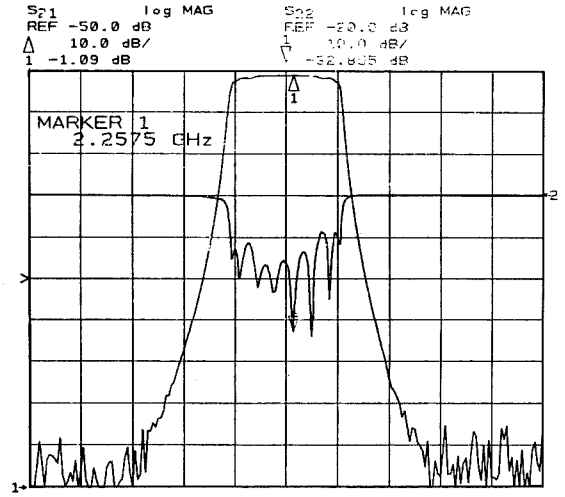


FIG.4 TRANSMISSION/REFLECTION CHARACTERISTIC OF THE FILTER.

Noise Measurement Instrumentation

by
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INTRODUCTION

The National Science Foundation funds Cornell University to support the National Astronomy and Ionosphere Center (N.A.I.C.). The major facility of the center is the world's largest single dish, radio telescope located near Arecibo, Puerto Rico (Figure 1). Receiver and antenna systems for that installation are developed at a research and development lab located at Research Park, Ithaca, New York.

Most of the front ends for the receiver systems used at the observatory are cryogenically cooled GaAsFET amplifiers. Some masers are in use at "S" band. The expection is that the next generation receivers will be cryogenically cooled amplifiers using modulation doped GaAsFETs (MODFETS). These are referred to also as high electon mobility transistors (HEMTS). They are in the development stage. Commercial units have been promised for early or mid 1986.[1] The forecast is that receiver system noise temperature will approach or equal the performance of masers at very much reduced cost and complexity. A receiver equivalent flange temperature of 4°K at "S" band is a design goal.

Even with present GaAsFET front ends receiver performances achieve 10°K at "L" band, 15°K at "S" band, and 22°K at "C" band when cooled to ~ 16°K with a closed cycle helium refrigerator.

Efforts have been made to test such low noise devices using commercially available noise measurement test equipment. A typical system is the H.P. 8970A.[2] The manufacturer quotes a noise figure instrumentation uncertainty of ± 0.1 dB. This is a noise temperature uncertainty of 14°K. Obviously, better resolution is required to measure receivers whose noise contribution may be very much less than the instrumentation uncertainty. It was decided to develop our own computer-aided automatic noise measurement test facility. *It is described herewith.*

FUNCTION

An instrumentation system for the development of low noise receivers should provide for the measurement and plotting of receiver noise temperature vs. frequency. It is useful to measure and plot receiver gain vs. frequency, also. In order to optimize receiver performance these measurements need to be made for various bias and tuning conditions. Speed and accuracy are important factors.

BASIC SYSTEM

A major part of such a system is a receiver back end (B.E.). A block diagram of a typical B.E. is shown in Figure 2. A hot and cold load standard are also required. Typically, a cold load (T_C) consists of a 50 ohm termination bathed in LN_2 which is contained in a vacuum dewar. A standard hot load (T_H) usually is a 50 ohm termination located in an oven at 100°c. Hence T_C = 77.3°K and T_H = 373.2°K. Manufacturers provide a plot of the deviation from 77.3°K and 373.2°K (T_C and T_H) vs. frequency for their particular hot/cold standard. This information defines the effect of transmission line losses in order to determine the real T_C and T_H.[3]

I. A procedure for measuring noise temperature for a given frequency is as follows (use block diagram of Figure 2 for the receiver back end):

1. Connect the Device Under Test (DUT) to the input of a Receiver B.E.
2. Set L.O. to frequency of interest.
3. Connect the input of the DUT to T_C and read V_{out1} (First set variable IF attenuator so that V_{out1} is within reasonable dynamic range of receiver back end).
4. Connect the input of the DUT to T_H and read V_{out2}.
5. Calculate y factor = $\frac{V_{out2}}{V_{out1}}$
6. Calculate system temperature: $T_{SYS} = \frac{T_H - yT_C}{y - 1}$
7. Calculate $T_{DUT} = \frac{T_{SYS} - T_{BE}}{G_{DUT}}$

a.) T_{BE} for each frequency of interest must first be obtained by the same steps outlined in 2 through 6 above except that (in Steps 3 & 4) connections to T_C and T_H are made directly to the post RF amplifier instead of to the DUT. In Step 6 substitute T_{BE} for T_{SYS}.

b.) The gain of the DUT (G_{DUT}) is obtained as follows:

(1) Connect the Receiver B.E. to a reference load.

(2) Read Vout.

(3) Insert the DUT between the receiver B.E. and the reference load.

(4) Add attenuation until Vout = the same as previous reading for Vout.

(5) The added attenuation = G_{DUT}.

These steps, (1) through (5), must be made for each frequency of interest.

II. Some problems associated with the procedures defined above are:

1. The connecting and disconnecting of the Device Under Test is an exacting business. Errors result from imperfect connections.
2. The time to conduct all of the steps for all of the frequencies of interest is prohibitive.
3. Receiver drift over such a long period can cause errors in the reaults.
4. Standard hot/cold load values (T_C = 77.3°K and T_H = 373.2°K) are too high for obtaining accurate noise measurements of a very low noise receiver whose noise contribution may be $\leq$ 20° K.

One technique to minimize the time for measuring and plotting receiver noise vs. frequency and receiver gain vs. frequency is to use a spectrum analyzer as a substitute for a receiver back end. The spectrum analyzer can drive an X-Y plotter to produce reasonable results. This arrangement does not address problems outlined in II-1 and II-4 above. Also more sophisticated techniques are needed to provide for modifying bias and tuning parameters between tests.

THE COMPUTER-AIDED AUTOMATED SYSTEM

To answer most of the needs for fast and accurate noise and gain measurements, a computer-aided instrumentation system was developed. An Apple II E computer® and an ISAAC 91-A® interface system were procured.[4] Rather than develop our own analog to digital input-output system, we chose to select a commercially available interface. The important thing was to get on line in the shortest possible time and to have a system that requires minimal effort for modification. The ISAAC 91-A by the Cyborg Company seems to be a good choice. It is designed especially for the Apple II E. Another ISAAC unit is compatible with the IBM PC. Its "Labsoft"® software package simplifies communications with the computer. Specifications are given in the appendix. A block diagram of the control and data acquisition system is shown in Figure 3. Figures 4 and 5 are flow charts of the "T_{SYS}" program and the "noise temp" program respectively.

A test dewar/refrigerator was assembled to provide rapid cool down and warm up times and for rapid installation of various amplifiers at the 16°K station of the dewar (see Figures 6 and 7). A receiver back end was developed which includes a switchable range low pass filter, amplifiers, adjustable attenuators and a voltage to frequency converter (V/F) output (see Figures 8 through 11). The V/F output is fed to a counter input channel of the ISAAC interface. The advantage of this technique is that it allows for rapid dumping of sampled signal levels between frequency settings. Also the V/F technique effectively averages voltage fluctuations over a specified length of sample time.

The hot load reference is provided by driving an H.P. 346B[5] noise diode through a directional coupler (-20 dB). When the diode is on, this results in a nominal noise temp. of ~ 100°K. The cold load consists of a 50 ohm termination located at the 16°K station of a test dewar, hence the cold temperature is ~ 16°K. However, transmission line losses, directional coupler insertion loss and ~ 3°K from hot load port of the coupler (when noise diode is off) result in a total T_C of ~ 30°K. Likewise actual T_H = ~ 100°

K (when diode is on) plus (T_C - ~ 3°K) ~ 127°K. These values must be calculated or measured in advance for each frequency of interest and placed in memory by the computer program.

After initialization is made the computer steps are:

1. Read the ambient temperature = (T_A)
   Read 16°K station temp. in dewar = (T_D)

   These readings are taken from voltage vs. temp. of a nonlinear diode (computer uses look up table from manufacturer's data).[6]

2. Read $T_{transmission\ line\ losses}$ + $T_{noise\ diode}$ (off) from a look up table. Add to T_D. This equals T_C for each freq. of interest.

3. Read (from look up table) $T_{noise\ diode}$ (on) and add T_C from above reading. Subtract $T_{noise\ diode}$ (off). This = T_H for each freq. of interest.

4. Read output of V/F = V_1 (first adjust "IF" attenuator for a reasonable dynamic range region of receiver R.E.).

5. Turn on noise diode (TTL noise diode drive = 1).

6. Read output of V/F = V_2.

7. Calculate y factor = $\frac{V_2}{V_1}$

8. Calculate T_{rec} = $\frac{T_H - yT_C}{y - 1}$ for this particular freq.

9. Increment YIG oscillator (= L.O.) from predetermined steps.

10. Repeat Steps 2 through 9 for 50 frequencies in 20 MHz increments.

11. Calculate T_{DUT} for each freq. = $\frac{T_{rec} - T_{RE}}{G_{DUT}}$

V. T_{RE} and G_{DUT} must be obtained in advance for these steps and included as information during the initialization process.

   1. T_{RE} is obtained in the same way as in Steps IV - 2 through 10 except that the DUT is bypassed and the results in Step IV - 8 = T_{RE} instead of T_{rec}.

   2. The gain of DUT (G_{DUT}) is obtained as follows:

      a.) Connect receiver R.E. to a reference load and record in memory V_{out1} vs. frequency.

      b.) Connect DUT between R.E. and same reference load.

      c.) Add fixed attenuator to bring V^2 det. output to within a reasonable region of the dynamic range of the R.E.

      d.) Record V_{out2} vs. frequency.

      e.) Calculate G_{DUT} = added attenuation + 10 log $\frac{V_2}{V_1}$ for each freq. of interest.

VI. For DUT optimization:

   1. a.) Program computer to change I_D.

      b.) Run test data IV - 2 through 10.

      c.) Compare with previous run.

      d.) Repeat for optiaum performance.

   2. a.) Program computer to change V_D.

      b.) Repeat Steps VI - 1-b through 1-d.

   3. During Runs 1 and 2 compare G_{DUT} vs. freq. as well as noise temps. vs. freq.

   4. Compromise minimum noise temp. and optiaum flatness and gain of DUT.

   5. If provisions are made for external tuning of DUT,

repeat Steps 1 through 4 above for each change in tuning until optimum performance is achieved.

VII. A sample plot of an optimized receiver is shown in Figure 12. Gain vs. frequency and noise temp. vs. frequency are plotted. This receiver was tested while operating at room temperature.[7]

Other less sophisticated programs are included. A system temperature measuring technique is for a more rapid measurement. As long as T_{RX} is known and the gain of the device under test is obtained (from e.g., a swept amplitude network analyser), the T_{DUT} can be calculated readily. In many cases the T_{RX} contribution may be negligible and hence the T_{DUT} approaches the value of T_{SYS}. The hot and cold levels used during the T_{SYS} testing can be those used in the more sophisticated testing or can be a standard 77.3°K cold load and a standard room temperature load with a thermometer.

CONCLUSION

The system allows for relatively rapid testing and plotting of various noise temperatures vs. frequency. It saves countless hours in the optimization of an amplifier.

Figure 13 shows a plot of a typical cryogenically cooled GaAsFET amplifier system temperature vs. frequency. This test can be made in less than five minutes using the computer-aided automatic noise temperature instrumentation system.[8] The conventional method would require a substantial increase in testing and computing time.

The ISAAC 91-A interface system minimizes the time for developing the test facility.

ACKNOWLEDGEMENTS

Acknowledgement is given to Dr. Sander Weinreb of the National Radio Astronomy Observatory. Many of the ideas for this system were borrowed from a similar system used by the NRAO at Charlottesville, VA.[9] A discussion with Dr. Weinreb and his associates led to the development of this test facility. His group provided the low loss input transmission lines.

Mr. Andrew Ingram, graduate student in Electrical Engineering at Cornell University, developed the software to be compatible with the ISAAC interface and the Apple IIE computer. Pierson C. Mosher developed the cryogenic system. Kurt Kabelac and David VanWinkle assisted in wiring and machining. Lynn Baker provided consultation.

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ISAAC is a registered trademark of Cyborg Corporation.
Labsoft is a registered trademark of Cyborg Corporation.

SYMBOL GLOSSARY

Symbol	Explanation
DUT	Device Under Test
G_{DUT}	Gain of Device Under Test
IF	Intermediate Frequency
LN_2	Liquid Nitrogen
L.O.	Local Oscillator
Rec. BE	Receiver Back End
T_A	Ambient Temperature
T_C	Cold Load Temperature
T_D	Dewar Temperature at 16°K Station
T_{DUT}	Noise Contribution of DUT
T_H	Hot Load Temperature
T_{REC}	Noise Contribution of Total System
V/F	Voltage to Frequency Converter
V_{out1}	Square Law Detected Output when Rec. is connected to T_C
V_{out2}	Square Law Detected Output when Rec. is connected to T_H
Y Factor	Ratio of $\frac{V_{out2}}{V_{out1}}$

REFERENCES

1 - Toshiba S 8900 Preliminary Data Sheet

2 - H.P. 8970A Noise Figure Meter Technical Data

3 - Maurey Microwave MT 7118-47 Cryogenic Termination Data Manual

4 - ISAAC 91-A by Cyborg Co., Newton, MA 02158

5 - H.P. 346B Noise Source Operating & Service Manual

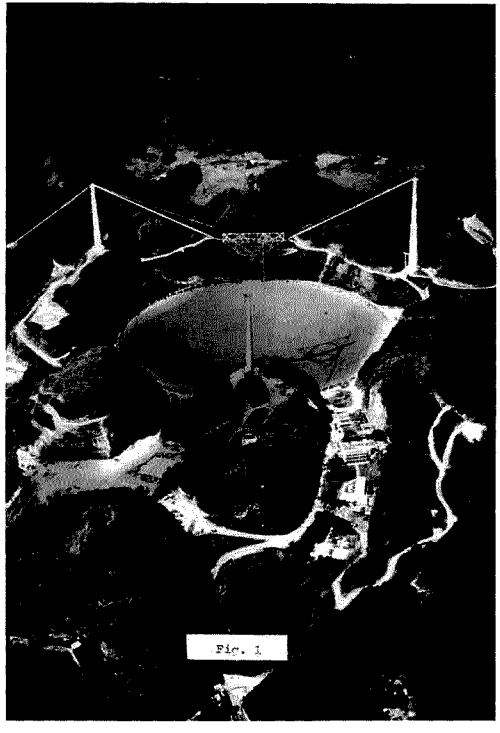
6 - Lakeshore Cryotronics Inc. DT-500-DRC D Voltage-Temperature Characteristics

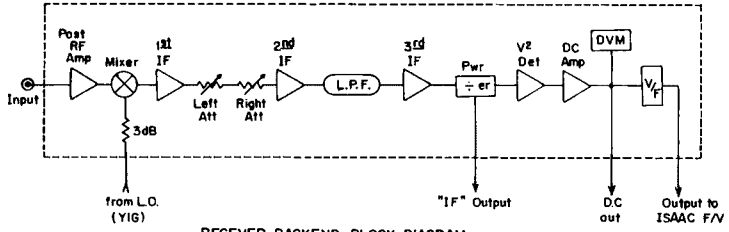
7 - NAIC Report: Dual Channel 6cm Cooled GaAsFET Receiver, March 1984, George Peter, et al.

8 - NAIC Report: Computer-aided Noise Measurement Instrumentation Manual 4-84. George Peter, et al.

9 - NRAO Electronics Division. Internal Report #212 - The Adios Analog - Digital Input Output System for Apple Computer - G. Weinreb & S. Weinreb.

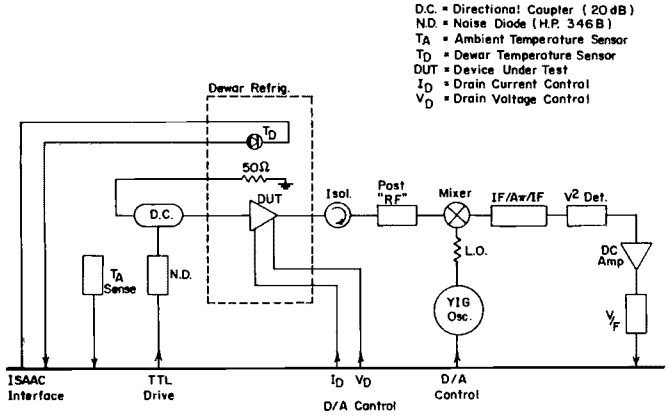
FIGURE	DESCRIPTION
1	Picture of Radio Telescope
2	Block Diagram Back End
3	Block Diagram Control & Data Acquisition System
4	Flow Chart Tsys Program
5	Flow Chart Noise Temp. Program
6	Test Dewar - Top View
7	Test Dewar - With Refrigerator Assembly
8	Receiver Rack
9	Receiver, Peripheral Rack, and Test Dewar
10	Receiver with Computer and Interface
11	Directional Coupler, J Line, and Noise Diode
12	Sample Plot Gain & Noise Temp. vs. Freq.
13	Plot of Cooled Receiver Noise Temp. vs. Freq.





RECEVER BACKEND BLOCK DIAGRAM.

Fig. 2



CONTROL AND DATA ACQUISITION BLOCK DIAGRAM.

Fig. 3

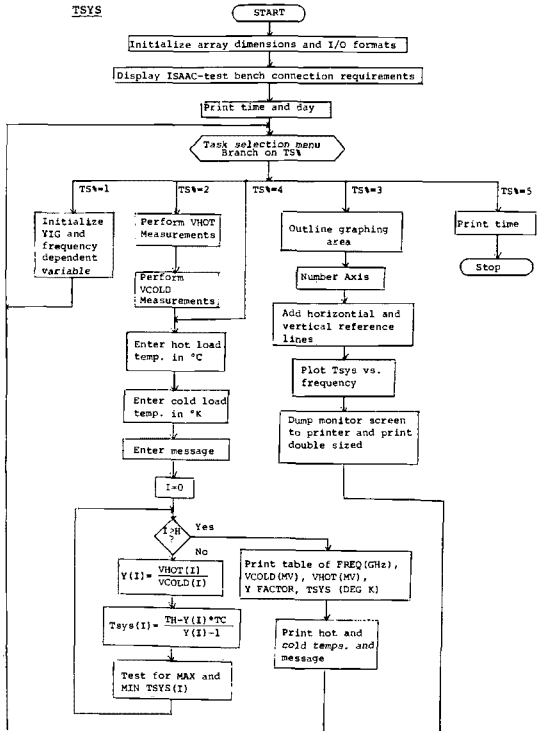

TSYS
START
Initialize array dimensions and I/O formats
Display ISAAC-test bench connection requirements
Print time and day
Task selection menu
Branch on TS%
TS%=1
TS%=2
TS%=4
TS%=3
TS%=5
Initialize YIG and frequency dependent variable
Perform VHOT Measurements
Perform VCOLD Measurements
Outline graphing area
Number Axis
Add horizontal and vertical reference lines
Print time
Stop
Enter hot load temp. in °C
Enter cold load temp. in °K
Enter message
Plot Tsys vs. frequency
Dump monitor screen to printer and print double sized
I=0
I=H ?
Yes
No
Y(I)= VHOT(I) / VCOLD(I)
Print table of FREQ(GHz), VCOLD(MV), VHOT(MV), Y FACTOR, TSYS (DEG K)
Tsys(I)= TH-Y(I)*TC / Y(I)-1
Print hot and cold temps. and message
Test for MAX and MIN TSYS(I)

Fig. 4

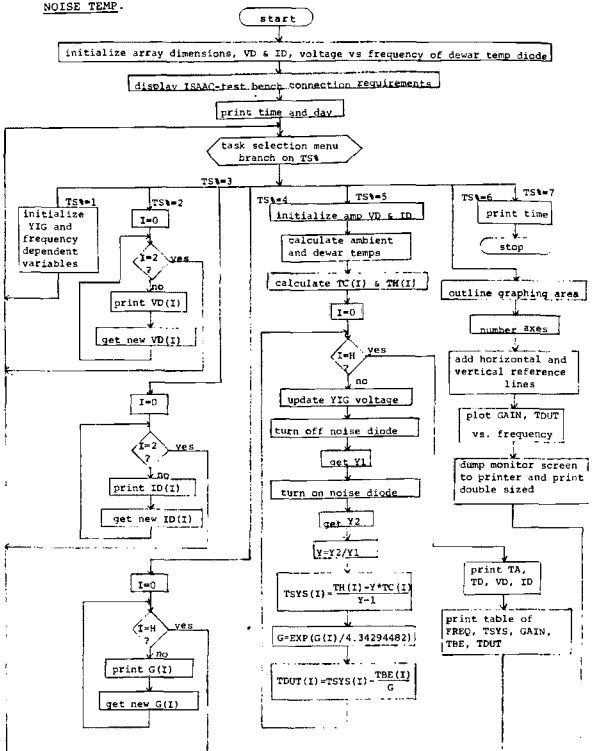

NOISE TEMP.
start
initialize array dimensions, VD & ID, voltage vs frequency of dewar temp diode
display ISAAC-test bench connection requirements
print time and day
task selection menu
branch on TS%
TS%=1
TS%=2
TS%=3
TS%=4
TS%=5
TS%=6
TS%=7
initialize YIG and frequency dependent variables
I=0
I=2 ?
yes
no
print VD(I)
get new VD(I)
I=0
I=2 ?
yes
no
print ID(I)
get new ID(I)
I=0
I=H ?
yes
no
print G(I)
get new G(I)
initialize amp VD & ID
calculate ambient and dewar temps
calculate TC(I) & TH(I)
I=0
I=H ?
yes
no
update YIG voltage
turn off noise diode
get Y1
turn on noise diode
get Y2
Y=Y2/Y1
TSYS(I)= TH(I)-Y*TC(I) / Y-1
G=EXP(G(I)/4.34294482)
TDUT(I)=TSYS(I)- TBE(I) / G
print time
stop
outline graphing area
number axes
add horizontal and vertical reference lines
plot GAIN, TDUT vs. frequency
dump monitor screen to printer and print double sized
print TA, TD, VD, ID
print table of FREQ, TSYS, GAIN, TBE, TDUT

Fig. 5

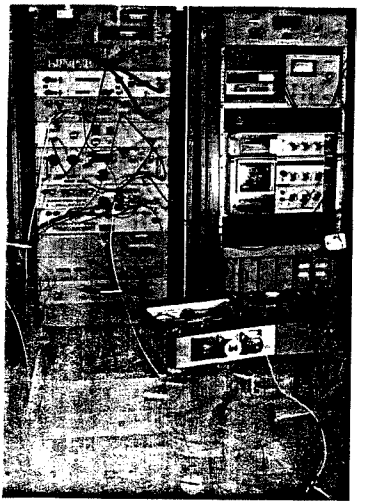


Fig. 8

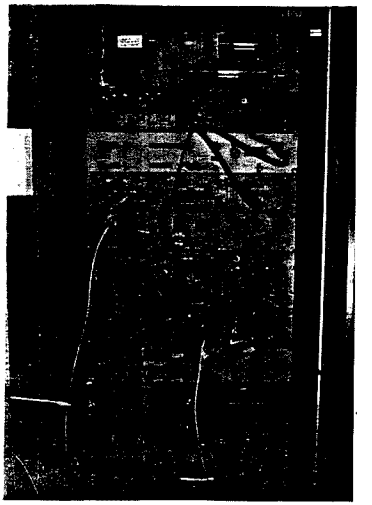


Fig. 9

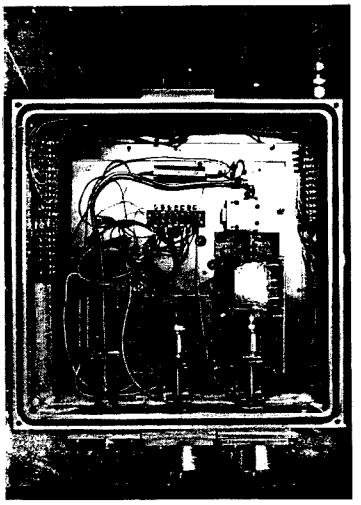


Fig. 6

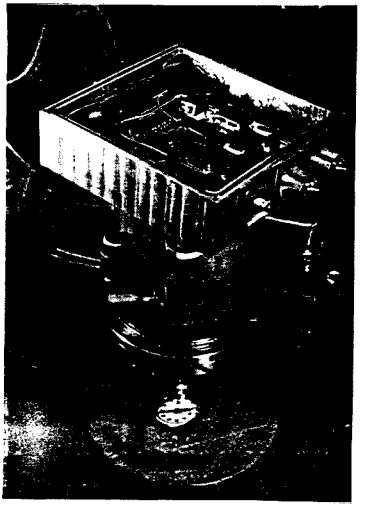


Fig. 7

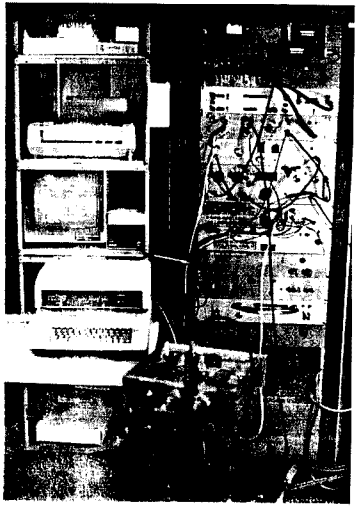


Fig. 10

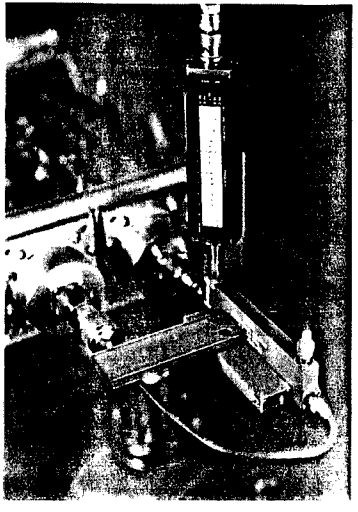


Fig. 11

POST AMP #1-1 5/18/84

TD = 13 DEG K TA = 288.091199 DEG K
VD1 = 4 VOLTS VD2 = 0 VOLTS VD3 = 0 VOLTS
ID1 = 20 MA ID2 = 0 MA ID3 = 0 MA

FREQ(GHZ)	TSYS(DEG K)	GAIN(DB)	TBE(DEG K)	TOUT(DEG K)
4.2	108.312151	12.6	160	99.5194972
4.25	100.915277	12.75	161	92.348037
4.3	99.5761709	12.9	167	91.0113857
4.35	97.5047259	13.15	173	89.123544
4.40000001	88.9786261	13.35	174	80.9331963
4.45000001	79.7263862	13.6	178	71.9564044
4.50000001	73.1402189	13.85	183	65.5988343
4.55000001	71.7695746	14.1	185	64.5722394
4.60000001	72.1413153	14.35	187	65.2731342
4.65000001	69.3786729	14.55	191	62.6793121
4.70000001	68.0493226	14.65	195	61.3453598
4.75000001	68.148501	14.75	197	61.5446819
4.80000001	69.511806	14.8	202	62.8229573
4.85000001	69.4286967	14.75	208	62.4614155
4.90000001	72.1273758	14.65	214	64.7921451
4.95000001	74.0534894	14.5	219	66.2830752
5.00000001	81.0295756	14.4	229	72.7175681
5.05000001	83.6417352	14.2	238	74.5932275
5.10000001	89.2936613	14	247	79.4604141
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5.20000002	110.239198	13.2	274	97.1247238

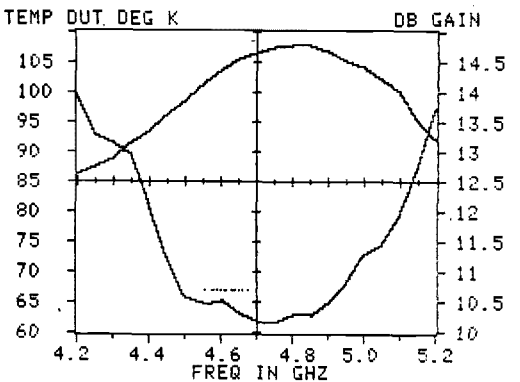

Fig. 12

FREQ(GHZ)	VHOT(MV)	VCOLD(MV)	Y FACTOR	TSYS(DEG K
2.2	313.26	100.1	3.12947053	19.6392006
2.21	301.97	96.18	3.13963402	19.1592536
2.22	302.59	95.97	3.15296447	18.5366238
2.23	316.38	100.08	3.16127098	18.1525326
2.24	342.4	108.33	3.16071264	18.1782578
2.25	371.2	117.69	3.15404877	18.4863177
2.26	416.28	132.34	3.14553423	18.8827161
2.27	425.43	135.24	3.1457409	18.873057
2.28	413.09	130.95	3.15456281	18.4624867
2.29	402.78	127.79	3.15188982	18.5865319
2.3	415.78	132.06	3.14841739	18.7481376

HOT TEMP = 296.56 DEG K
COLD TEMP = 81.4 DEG K
CH#1/30MHZ IF FILTER/VD1=1.476V/ID1=4.23MA/VD2=5.054V/ID2=6.80MA/VG1=-297V/VG2=-0.864V

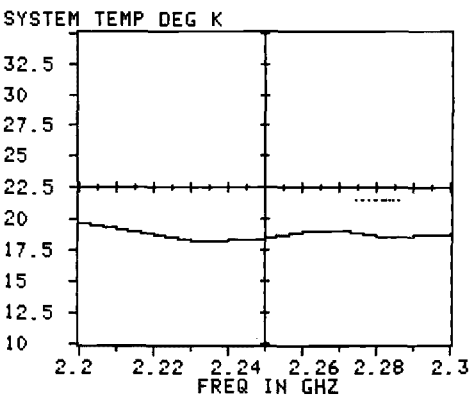

Fig. 13

APPENDIX : HARDWARE SPECIFICATIONS

All specifications typical @ 23°C.

Storage temperature: 0-70°C.
Operating temperature: 10-40°C (30 min. warm up)

A/D Subsystem

Resolution: 12 bit (.025%)
Channel acquisition time: 100 microseconds
A/D convecsion time: 25 microseconds
Accuracy: +/-.05% of full scale
Differential nonlinearity: +/- .025% of full scale
Temperature coefficient: +/- 75ppm/°C
Common mode rejection (differential mode): 70 dB
Input bias current: +/- 100 nanoAmps
Input impedence: < 100 picofarads
> 100 megohms

D/A Subsystem

Resolution: 12 bit (.025%)
Capacitive load: < 1000 picofarads
Accuracy: +/- .05% of full scale
Differential nonlinearity: +/- .025% of full scale
Output current: +/- 5 milliamperes
Overshoot: < 2% of full scale
Temperature coefficient: +/- 50ppm/°C
Settling time: < 5 microseconds (to < 2% of full scale)

Binary Input Subsystem

Input port: 16 bit
Input signal: (high)+ 2 Volts/40 microamperes
(low) + 0.8 Volts/0.9 microamperes
Communications: STROBE, HOLD, and CLEAR TO SEND

Binary Output Subsystem

Output port: 16 bit
Fan out: 4 standard TTL loads (50 LS TTL loads)
Output signal: (high) + 3.1 Volts/2.6 milliamperes
(low) + 0.5 Volts/20 milliamperes

Binary Output Subsystem (cont.)

Communications: STROBE, GATE, CLEAR TO SEND
Communications fan out: 4 standard TTL loads
(20 LS TTL loads)

Schmitt Trigger Subsystem

Response time: 5 microseconds
Hysteresis: 20 millivolts

Counter Device (Channels 0-6)

Input signal: (high) + 2 Volts/20 microamperes
(low) +0.8 Volts/400 microamperes
Maximum count frequency: 10 megahertz (50% duty cycle)
Minimum count frequency: DC

Counter Device (Channel 7)

Maximum input voltage: 50 Volts (DC + peak AC)
Sensitivity: 100 millivolts RMS
Maximum count frequency: 2 megaHertz (50% duty cycle)
Minimum count frequency: 0.5 Hertz (sine wave)

Timer Subsystem

Accuracy: (dependent on Apple CPU clock)
Resolution: 1 millisecond

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TEMPERATURE COMPENSATION CIRCUIT FOR SPACE DATA TRANSMITTERS

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A B S T R A C T

Temperature compensation for data transmitters used in spacecraft is a long felt requirement to maintain a constant equivalent isotropic radiated power. Presented in this paper is a simple and efficient technique which incorporates an automatic gain adjusting circuit associated with temperature sensitive components. The advantages over other types of schemes are explained. The application of this scheme is explained with the help of an X-band data transmitter qualified for on-board use in the Indian Remote Sensing Satellite.

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I N T R O D U C T I O N:

The design of systems for space applications calls for best efficiency, as DC power is precious for spacecraft, while avoiding thermal stress on components to ensure reliable operation over the wide temperature ranges.

Efficiency and reliability are two vital parameters for a space system design. No compromize on reliability is possible in space system design as no scope exists after launching a spacecraft into orbit for repair or replacement of a system. Usage of 100% screened and tested components with proper derating will ensure that components are reliable and that circuits are designed to avoid additional stress on the components over the severe environment change, as quite a few parameters will vary with temperature. Temperature effects accumulated over all the stages of the system result in unwanted effects in alarming proportion and may even lead to failure of the system.

In an amplifier chain, for example, the drive requirements of an amplifier stage change with temperature, as base emitter voltage (Vbe) and current gain (B) of a transistor change. At low temperatures the amplifier may not have sufficient drive to give required output and at

high temperature the transistor may be driven into hard saturation resulting in poor efficiency with over dissipation.

In a data transmitter the level at the input of a power amplifier, viz. TWTA, should remain constant over the temperature range to avoid phase shift changes. Power variation in each stage of a transmitter has to be minimized to overcome unwanted effect. This can be achieved by incorporating temperature compensation techniques.

COMPENSATION TECHNIQUES FOR THE DESIGN OF A TRANSMITTER:

The basic transmitter to transmit data from spacecraft uses RF amplifiers, frequency multipliers to generate microwave signals from the basic crystal oscillator used as a high stability frequency source, a modulator to enable the microwave carrier to carry the data, and final power amplifiers such as TWTA to boost the modulated microwave signal to a sufficient level so the antenna can radiate enough power to enable the ground system to capture the signal to get the data. A typical transmitter schematic is shown in the Fig.1.

All stages of the transmitter have to be designed in such a way that the level at the input of TWTA remains fairly constant over the full temperature range and no transistor or diode dissipates more power than the designed value, even at extreme temperatures. This calls for maintaining the variation in each stage within limits.

To some extent, variation in the passive component values and their effect on gain and power output can be estimated from the available data and can be taken care of in the design by providing wider band widths.

To reduce the power and gain variations resulting from various parameter changes due to temperature variation, many methods are available and their merits are discussed in the following paragraphs.

TEMPERATURE COMPENSATION IN FREQUENCY MULTIPLIERS:

The variation of the power output in frequency multipliers using step recovery diodes can be minimized by compensating for the change of lifetime of the SRD. The bias is directly proportional to the diode lifetime. The rate of change of SRD's lifetime is +0.5% to 0.7% per ^{o}C (1). This is closely matched by the rate of resistance change of a silicon resistor (sensitor).

The multiplier can be temperature compensated simply by using a sensistor to develop the bias voltage, instead of a resistor. This type of simple compensation maintains the output variation within 1 dB over a fairly wide temperature range.

For further compensation, the power output of the driver amplifier (at input frequency) should be varied to compensate for the variation in the conversion loss of the multiplier with temperature by adjusting the gain of the preceeding stages, using temperature sensitive components in the bias/supply circuitry of the driver amplifier.

TEMPERATURE COMPENSATION IN AMPLIFIERS:

A simple and coarse method to restrict the output variation in an amplifier to some extent is to add a resistor in series to the supply voltage. This method is inefficient and also inaccurate.

The commonly used technique is to operate the power amplifier stages in Class C and to drive them fully into saturation where decrease in input level will not result in equal reduction in output level. The collector efficiency is reduced as the transistors are operated in the gain compression region. This carries the disadvantages explained earlier and cannot take care of the variation of preceeding stages totally or the variation of succeeding stages.

Another technique is to use temperature sensitive components like thermistors in the bias network of Class A stages. This cannot take care of the variation of other stages.

Since efficiency is the prime consideration for space systems, there is a need to look at other methods, such as the leveling loop approach, which is complex.

The standard leveling loops control the gain of the preceeding Class A stages by sensing output power level. Another way is to use an variable attenuator like a PIN diode attenuator to keep the output level at constant value by varying the attenuation automatically depending on output level.

The basic circuit schematics to provide autoleveling are shown in Fig.2. The necessary circuit elements include a directional coupler, detector, feedback amplifier and a PIN diode attenuator in the second approach. The directional coupler samples the RF output signal which is converted to a

proportionate DC signal which is amplified by the feedback amplifier, the output of which controls the bias current of the transistors to adjust the gain or the bias current through the attenuator diode to adjust the attenuation to keep the output constant. This type of leveling loop technique to keep the output constant by controling the gain or attenuation at low power level, maintains efficiency of the transmitter.

Another simple leveling loop technique (2) which maintains both efficiency and output of cascaded amplifier stages uses the voltage drop across a resistor connected in series with the collector bias network of the output transistor to control the gain of the preceeding Class A amplifier stage.

Power output and efficiency of the amplifier using this simple leveling loop are nearly flat against variations of temperature and input drive level. This approach cannot take care of the variations of succeeding stages.

This disadvantage can be overcome by incorporating a temperature sensitive resistor, viz. thermistor, to drive the reference voltage. The schematic of the amplifier circuit used to maintain the output of the final multiplier (i.e. at the input of the TWTA shown in Fig.1) is shown in Fig.3.

The cascaded amplifier section consists of one Class A amplifier driving the Class C amplifier stage. The voltage generated across resistor R_1 connected in series to the collector supply of Q_2, is compared with the reference level generated by the resistors and thermistor network by a PNP transistor (Q_3). As the collector current of Q_2 changes, the bias voltage supplied to Q_1 by the comparator/feedback amplifier Q_3 changes, resulting in a change in the gain of the Class A amplifier Q_1 and thereby the drive level to Q_2 which brings the collector current of Q_2 back to the initial value. Since output power is nearly proportional to collector current, the output level remains constant.

Any change in the drive obtained from proceeding stages tries to change the current in Q_2 and the loop adjusts the gain of Q_1 to maintain the current in Q_2, thereby keeping the output level constant. The PNP transistor Q_4 connected as a diode in the bias circuit of Q_3 compensates for the changes in the emitter base junction of the transistor Q_3 over the temperature range.

The output power can be adjusted by changing the reference voltage at the base of Q_3. The thermistor network is designed in such a way that the change in the reference voltage due to temperature variation adjusts the output power of the amplifier to compensate the power

change in the succeeding stages. The temperature compensation network can be selected easily if the power variation in succeeding stages is known, else this can be estimated practically.

DESIGN OF THE COMPENSATING NETWORKS IN TRANSMITTERS

In a transmitter like the one shown in Fig.1 it is found that temperature compensation of the SRD frequency multipliers and the two stage amplifier preceeding the final multiplier, by incorporating the autoleveling loop associated with the thermistor network, is adequate to keep the power level at the input of the TWTA constant.

The first frequency multiplier can be of the order of 2 or 3 using a transistor, as the basic crystal oscillator frequency will be below 100 MHz. The following amplifiers also need not have any special compensation network and even need not be operated in hard saturation. The variation will be taken care of by the autoleveled amplifier following the second frequency multiplier.

In the frequency multiplier that uses SRDs, usage of a silicon resistor as the biasing resistor nearly compensates for the changes caused by lifetime variation with temperature. In spite of this compensation, power loss variation will be on the order of 1 dB over a $-20^{\circ}C$ to $+60^{\circ}C$ temperature range. This variation has to be taken care of by the proposed compensated leveling loop. The compensated leveling loop should be designed to take care of the variation in input level in various preceeding stages caused by the wide environment change and the loss variation in the succeeding stages. The current sensing resistor R_1 should be selected to be a low value (less than 10 ohms) as higher values drop supply voltage to the transistor, thereby reducing the available gain and power.

The Class C amplifier should be designed to have a higher compression point, i.e. to give higher power output at room temperature than normally required. In the potential divider network at the base of Q_2 a potentiometer P2 is used in place of the thermistor network (R3, R4 & R5). Resistor R6 is to limit the base current and in turn the collector current of the Class A amplifier (Q_1). This value is to be adjusted to limit the collector current within a safe limit when no input is fed and to be the normal operating current with drive at room temperature. It should be noted here that the collector current of the Class A amplifier will be maximum at no drive condition. To be on the safe side a high value can be

choosen for R6 to start with which can be reduced after adjusting the reference voltage for the required output.

With normal expected drive to Q_1, the reference voltage at the base of Q_2 can be adjusted with the help of potentiometers P_1 and P_2 to get the required output from the Class C amplifier. The AGC action can be checked by varying the input level. To get a wider range for AGC action, if necessary the P_1 and P_2 combination may be readjusted by changing R_1. Check for the change in output level of at least $\pm$ 1 dB variation which will be higher than the expected variation in loss in the succeeding stages, by varying the potentiometer P_2.

If the loss of the multiplier and modulator at different temperatures is known, the output of the amplifier chain required to maintain the output of the modulator can be estimated and the corresponding P_2 values can be measured. If the variation is not known, or for greater accuracy the whole transmitter up to the modulator can be kept in hot and cold simulation chambers by bringing the potentiometer P_2 outside. The value of P_2 needed to keep the output level constant should be measured at different temperatures. A thermistor, resistor combination can be worked out to closely follow the resistance values required at different temperatures.

By using MSC 80064 and MSC 3000 transistors for Class A and Class C amplifiers, an amplifier chain is designed at L-band to drive an X5 frequency multiplier. A compensated leveling loop technique is incorporated in the L-band amplifier chain. The final power output is found to be within $\pm$ 0.2 dB over $-30^{\circ}C$ to $+70^{\circ}C$ against $\pm$ 4 dB input level variation to the amplifier. An isolator has to be used at the input of the Class A amplifier to take care of the return loss changes.

CONCLUSION:

Different types of temperature compensation methods that can be used in designing telemetry/data transmitters for space application, where it is essential to maintain the efficiency of the system by avoiding thermal stress on components over the wide environments, are pointed out. A simple but more effective compensated auto leveling loop that controls the gain of a Class A amplifier stage, depending on the current of the final Class C amplifier, is presented. The output level is maintained constant against variations in the drive level upto $\pm$ 4 dB. The reference voltage generated by the potential divider

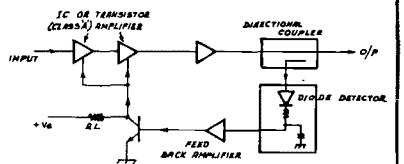

FIG. 2 a. SCHEMATIC OF AGC CIRCUIT.

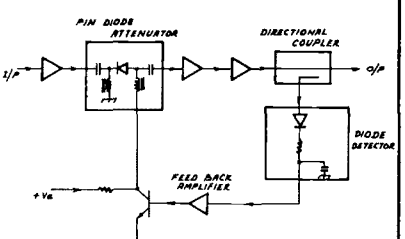

FIG. 2 b. SCHEMATIC OF AUTOLEVELLED CIRCUIT.

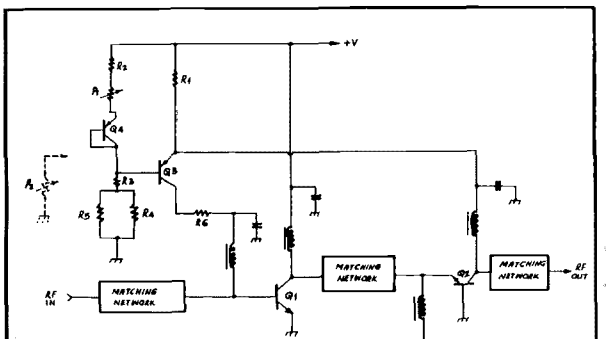

FIG. 3. SCHEMATIC OF AN AMPLIFIER USING COMPENSATED AUTOLEVELLING LOOP CIRCUIT.

consisting of a thermistor network is automatically varied to adjust the output level to compensate the power variation in succeeding stages. An X-band data transmitter designed with this type of temperature compensated leveling loop gave good results and was found to be very useful for space applications. It is found that a compensated leveling loop in the final amplifier chain preceeding the last multiplier is adequate to take care of all the variations caused by temperature change.

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The authors gratefully acknowledge the encouragement from Col. N. Pant, Director, I.S.R.O. Satellite Centre and Dr. S. P. Kosta, Dy. Director (Spacecraft Electronics Group) ISRO Satellite Centre and thank other colleagues for their valuable suggestions.

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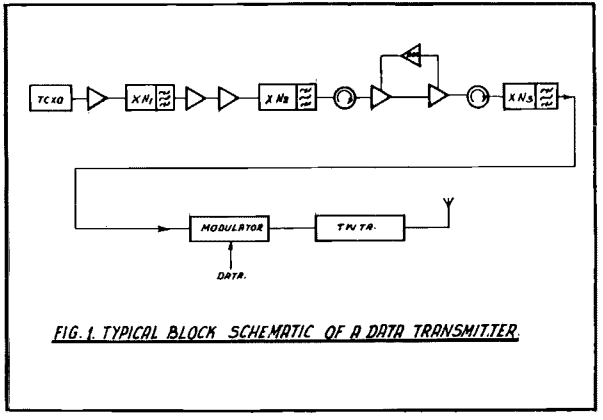

FIG. 1. TYPICAL BLOCK SCHEMATIC OF A DATA TRANSMITTER.

TESTING OF NARROWBAND COMMUNICATIONS RECEIVERS - ACSB AND SSB

by

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This paper discusses the effects of adjacent channel, reciprocal mixing and intermodulation performance on narrowband Amplitude Compandored Sideband (ACSB) or Single Sideband (SSB) receivers. A test procedure will be given to evaluate this performance and the signal generator specifications will be discussed in relation to the above tests.

SPECTRUM EFFICIENCY

The Commercial Spectrum.

Over the last few years, the radio frequencies allocated to mobile radio have become very congested. Action now has to be taken to overcome these problems. In the larger metropolitan areas such as Los Angeles there are virtually no frequencies available. So what can be done? First of all, more frequencies can be released for the mobile radio users and this has been done by opening up the 800/900MHz band, primarily for cellular radio. Other action needs to be taken for such organizations as the police and fire departments, who must have secure radio channels.

The present systems employ FM in 20 KHz channels. This modulation system was implemented because of its superior fidelity, better signal to noise performance, and most important of all "hands-off operation". Unfortunately, a price was paid for this...spectrum inefficiency.

A new narrowband technology, for the commercial user, employing audio compandored single sideband techniques has now been approved. ACSB systems offer communications in a bandwidth significantly less than that used in FM systems. It can be shown that all the information from the human voice can be contained in the frequency range 300 Hz to 3.4 KHz. In fact, in SSB systems, intelligibility is still maintained with a high frequency cut off at 2.4 KHz. Research in the U.S. by Dr. Lusignon[1] and Dr. Fred Cleveland and in the U.K. by Professor W. Gosling and Dr. Joe McGeehan,[2] showed that SSB could meet the needs of the VHF and UHF land mobile users. The FCC is now licensing ACSB radio systems with 5KHz channel spacing in an attempt to reduce the congestion.

Four new ACSB channels can be introduced where one FM channel previously resided. See Figure 1.

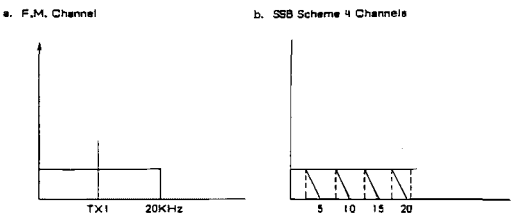


Figure 1

The Military Spectrum.

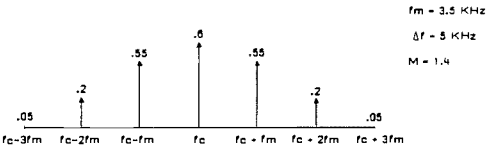
The military have used SSB at HF for many years, as it lends itself to better power efficiency, communications efficiency, security and reliability. Military systems have been developed to give the ultimate performance from both transmitter and receiver. Specifications for military equipment are more stringent than commercial. For instance, adjacent channel transmitters could be using as much as 1 KW of power while most commercial mobile radio transmitters may use only 10 watts. The military receiver, to handle such large signals, needs to have 20 dB better adjacent channel performance than the commercial equipment. See Table 1.

Table 1

Minimum FM STO As Defined by RS204C	TYPICAL FM MOBILE SPEC	MILITARY COMMUNICATIONS RECEIVER 2.7KHz B.W.	ACSB MOBILE SPEC
Usable Sensitivity 0.5µV	.5µV	<0.35µV	0.25µV
Adjacent Channel Selectivity >70 dB	75 dB	>90 dB	80 dB
Intermodulation (In Band) >00 dB	60 dB	>60 dB	N/S

FM v SSB

Figure 2 shows an FM spectrum of a carrier fc with 5 KHz of deviation (Δf) and a maximum modulating frequency of 3.5 KHz. This results in a modulation index of approximately 1.4. The side frequency pairs can be calculated from Bessel functions. By inspection, the majority of the power is contained in the first two side frequencies resulting in a bandwidth of 14 KHz.



Pig 2 FM Spectrum of a carrier fc, deviation Δf and maximum modulating frequency fm.

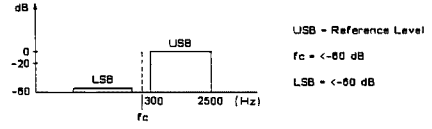
Figure 3a shows an SSB spectrum. The carrier is reduced 60 dB below the speech sideband. (shown as an upper sideband.) The lower sideband is also reduced by at least 60 dB, resulting in the majority of the spectrum power being contained in a 2.2 KHz bandwidth.

Figure 3b shows an ACSB spectrum with a slightly greater bandwidth due to the 3.1 KHz tone above band (TAB). Other ACSB methods have been proposed with tones in band (TIB) From the above examples, the spectrum efficiency of SSB is clear.

After reducing the bandwidth and implementing essentially an AM scheme particular attention must be paid to performance. In fact, the same performance as was achieved in the FM system should be aimed for.

Originally adjacent FM channels were geographically spaced to reduce the chances of adjacent channel inteference. This luxury can no longer be afforded because of spectrum congestion. The same will apply to an SSB or ACSB system, and with channels only 5 KHz apart particular attention must be paid to transmitter and receiver performance.

a. SSB Spectrum



b. ACSB Spectrum

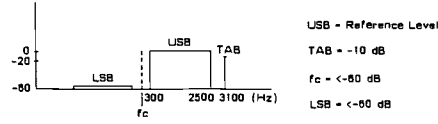


Figure 3

RECEIVER TESTING

Emphasis has already been placed on spectrum conservation by the use of SSB schemes. Correct alignment of the transmitters is, therefore, always paramount. Non-linearity in an SSB transmitter produces the same effect as over-deviation in an FM transmitter.....gross spectrum abuse. Assuming that the transmitters are correctly aligned, receiver performance must be assessed with the equivalent of a good clean radio transmitter. Consideration must, therefore, be given to the signal generator. A phase noise spec 20 KHz from carrier, good enough for present FM channel spacing, is no longer acceptable. Equal performance 5 KHz from carrier must now be sought. As will be shown later, far more stringent tests such as reciprocal mixing on narrowband CW military receivers necessitates low phase noise even closer than 5 KHz. Generator specifications relevant to the test in question will be highlighted.

ON CHANNEL TESTS

The most important of these tests, that of sensitivity will be discussed briefly. The sensitivity of the receiver must be established before proceeding to discover how strong off channel signals affect this performance.

Referring to Table 1 the performance for the SSB communications receiver for a 10 dB (S+N)/N ratio is 0.35 microvolt (-117dBm) or better. To test for this performance, a single tone only is needed. (Unlike the AM or FM receiver, the carrier is of no value.)

USABLE SENSITIVITY

TEST SETUP

TEST PROCEDURE

1. Connect audio load and AC voltmeter to receiver under test.
2. Set generator RF to produce a 1 KHz (±100 Hz) beat note. Use manual RF gain, if available.
   (N.B. no modulation is needed on generator.)
3. Set generator output for approximately 1 millivolt and adjust volume for 25% of maximum rated output.
4. Reduce RF level until ratio of audio output, between signal on and off conditions is 10 dB.
5. The signal level to achieve the condition in 4, is the usable sensitivity.

Arguments have been raised over the definition of "usable sensitivity". This test procedure uses the 10 dB S/N standard as it was originally defined by EIA. However, the

paper given by Jim Eaglesen at the 1985 RF Expo defines "usable sensitivity" more accurately.

H.D.S. (Minimum Discernable Signal) is the level where the signal is just detectable. Representing 0 dB SNR, this can only be used for theoretical calculations. SNR (Signal to Noise Ratio) is the level at which a signal just becomes useful. Most manufacturers specify 10 dB SNR.

Other on channel tests are 1) AGC - determines the ability of the receiver to mantain constant audio output level with varying RF innput levels; 2) A.G.C. time constant. Fast attack times need to be used at VHF to optimize the receiver during fast fade conditions as would be experienced under mobile operation; 3) Spurious performance. Not a true on-channel test, but requires only one input signal. This is the ability of the receiver to prevent single unwanted signals from causing an unwanted response at the output of the receiver, normally caused by discrete spurii from the synthesizer mixing with other signals.

SIGNAL GENERATOR PERFORMANCE

For sensitivity testing, the most important aspect of the generator is output level accuracy. As well as the absolute accuracy specification, typically ±1 dB at -120 dBm, attention must be made to VSWR. Most modern wideband receiver front ends have VSWRs approaching 2:1 and with signal generator VSWRs of 1.5:1, errors as great as 4 dB can be experienced at the antenna input of the receiver.

OFF CHANNEL TESTS

ADJACENT CHANNEL PERFORMANCE

This is a measure of the receiver's ability to differentiate between a desired signal (on-channel) and signals on adjacent channels. It is primarily a function of the IF filter response and could also be called a selectivity test. Some test methods do not use an on-channel signal generator and rely on the increase in noise level caused by a high level signal off-channel, this does not test for the true operating conditions. At 5 KHz offsets, as found in SSB receivers, reciprocal mixing tends to mask the selectivity performance.

SIGNAL GENERATOR PERFORMANCE

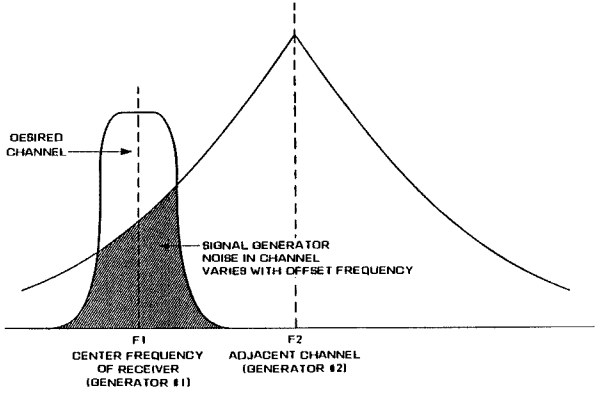
Care must be taken with the adjacent channel test to ensure that the phase noise of the off channel signal generator does not hide the true adjacent channel performance of the receiver. See figure 4. To establish if a signal generator will meet these requirements, the following facts are needed.

1. What is the adjacent channel offset on the receiver to be tested?
2. What is the IF bandwidth of the receiver?
3. What is the specified adjacent channel performance?

Inserting some typical figures for an SSB receiver, the results are as follows:

1. Adjacent channel offset = 5 KHz
2. IF Bandwidth = 2.7 KHz
3. Adjacent channel spec = 80 dB

IMPORTANCE OF SIGNAL GENERATOR PHASE NOISE IN ADJACENT CHANNEL TESTS



TYPICAL REQUIREMENTS:

For 5 KHz channel spacing phase noise should be at least -130 to -140 dBc/Hz for selectivity measurements of 80 dB and suprious signals should be down greater then 80 dB.

Figure 4

The signal generator noise is specified in a 1 Hz bandwidth, but the measurement is made in the receiver's 2.7 KHz IF bandwidth. To find the difference, in dB, use the formula: 10 log IF bandwidth/1 Hz.

For 2.7 KHz, the result is 34 dB.

The required signal generator noise spec can now be calculated at a 5 KHz offset, using the formula: - receiver spec + bandwidth conversion (as above) + 10 dB measurement margin.

From the example; 80 dB + 34 dB + 10 dB

= 124dB below carrier.

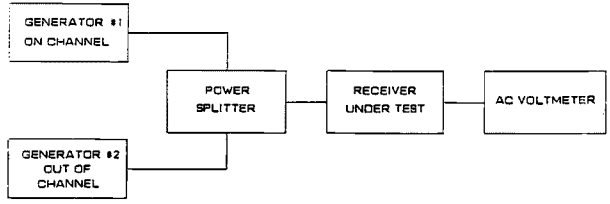
Table 2 gives the required signal generator phase noise performance against narrowband communication bandwidths and their typical 80dB measurement points. To determine how much better than the 80 dB adjacent channel spec a receiver is, even greater performance is needed from the signal generator. For example, 90 dB adjacent channel performance requires a phase noise spec of -134dBc, at a 5 KHz offset.

Table 2

Signal generator PHASE NOISE in dBc needed to measure 80dB adjacent channel performance on receivers with the following common bandwidths.

① 1 Receiver Bandwidth	② Mode	③ Equivalent Noise Bandwidth	④ 80dB Filter Response	⑤ 2 - Signal Generator Performance at the offset in column 4
400 Hz	C.W.	26 dB	1500Hz	-116 dBc
1200	RTTY	31 dB	4000Hz	-121 dBc
2700	SSB	34 dB	5000Hz	-124 dBc
6800	AM	38 dB	15000Hz	-128 dBc

ADJACENT CHANNEL TEST

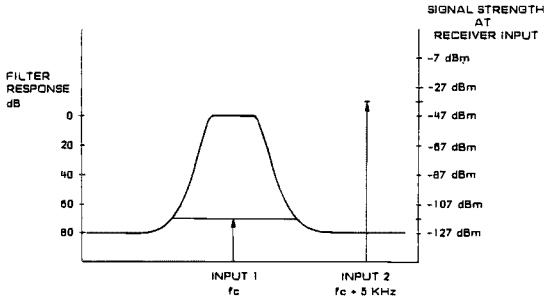


TEST PROCEDURE

1. Turn generator number 2 off, set generator number 1 to the receiver frequency +1 KHz. Obtain the condition for usable sensitivity, i.e. 10 dB S/N.
2. Increase the level of the wanted input signal by 3 dB.
3. Turn generator number 2 on and tune it 5 KHz away from generator 1.
4. Increase level of generator number 2 until the S/N ratio falls back to 10 dB.
5. The ratio of the unwanted signal measured in Step 4 to the reference sensitivity is the adjacent channel performance.

ADJACENT CHANNEL TEST

FIGURE 5



The input to an IF filter consists of two signals, the wanted signal equivalent to -117 dBm at the antenna input and a strong -27 dBm signal 5 KHz higher. The filter offers 80 dB attenuation at a 5 KHz offset, reducing input 2 to a level of -117 dBm at the output of the filter. The adjacent channel signal will now be at the same level as the wanted signal and will continue through the rest of the receiver, interfering with the wanted signal.

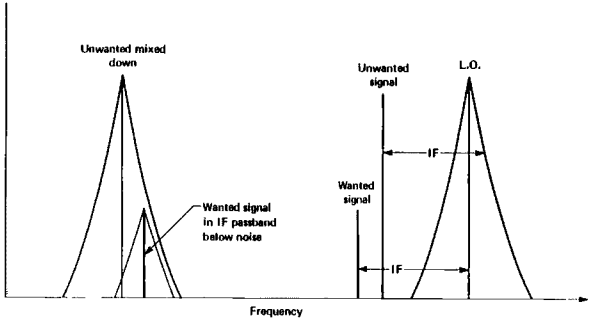
RECIPROCAL MIXING PERFORMANCE

Reciprocal mixing is caused by phase noise imperfections on the receiver's local oscillator. Normally the strong local oscillator signal is mixed with a weak wanted signal to produce the IF signal. However, the mixer will perform the same for any other pair of signals separated by the IF. Reciprocal mixing is so named because the role of local oscillator and signal are reversed; a strong unwanted signal off-frequency mixes with the weaker phase noise of the local oscillator. As an example, when a strong signal 5 KHz from the receive frequency mixes with the phase noise 5 KHz from the center of the local oscillator, the result is an IF output with noise proportional to the local oscillator phase noise. See Figure 6. Until the emergence of synthesized local oscillators, with their less than perfect noise sidebands, reciprocal mixing went unrecognized. Crystal oscillators, used at VHF and UHF for frequency stability, had far better noise performance, and reciprocal mixing was well below the adjacent channel performance.

Reciprocal mixing and adjacent channel performance are very closely related. The ultimate performance of the IF filter can never be realized if the receiver local oscillator is noisy.

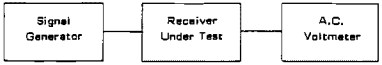
SIGNAL GENERATOR PERFORMANCE

The close to carrier noise performance of the generator must be at least as good as that for adjacent channel tests. If a measure of the reciever local oscillator phase noise is required, refer to Table 2.



RECIPROCAL MIXING
Figure 8

RECIPROCAL MIXING TEST



TEST PROCEDURE

1. Tune the signal generator to the offset of interest.
2. Monitor the AF output level noise with no input to the receiver.
3. Increase the signal generator until a 3dB increase in noise at the AC voltmeter is observed.
4. Note the level obtained in 3 and add this to the noise floor of the receiver. Note: the noise floor is 10dB lower than the usable sensitivity figure. Refer to Fig. 6 and table 3.

This test should be repeated at different offsets to establish the phase noise of the oscillator and therefore, the ultimate adjacent channel performance.

Table 3

① Frequency Offset	② Input Level	③ Level with Respect to -127 dBm Noise Floor in 2.7 KHz BW	④ Receiver Oscillator Phase Noise in a 1 Hz BW
5 KHz	-55 dBm	72 dB	-106 dBc
10 KHz	-47 dBm	80 dB	-114 dBc
20 KHz	-38 dBm	89 dB	-123 dBc
100 KHz	-19 dBm	108 dB	-142 dBc

INTERMODULATION PERFORMANCE

In the strong signal environment of large metropolitan cities or where many transmitters are operational at the same time and geographically close, it is not just adjacent channel performance that is critical. Two strong signals spaced at some distance from the adjacent channel, yet within the bandwidth of the roofing filter, can mix in the front end of the receiver and produce intermodulation products that fall in the IF passband. This test is a measure of the capability of a receiver to inhibit the generation of such in band signals.

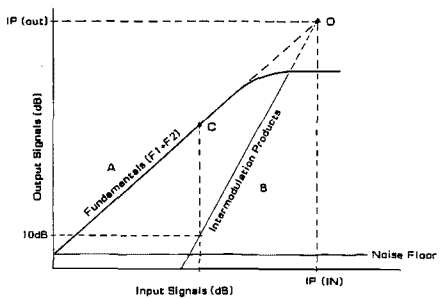
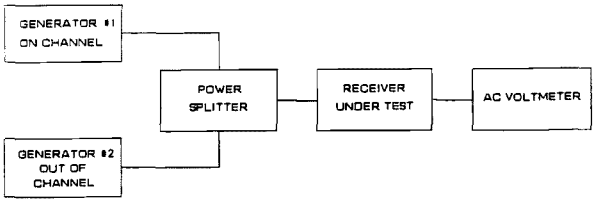


Figure 8

INTERMODULATION TEST



TEST PROCEDURE (3RD ORDER)

1. Set generator number 1 to fc + 20KHz.
2. Set generator number 2 to fc + 39KHz.
3. Increase the outputs of the two generators, keeping the amplitudes the same, until the receiver produces a 10 dB S/N.
4. The difference in level between the usable sensitivity (10 dB S/N) and the outputs of the generators to obtain the condition 3 is the intermodulation performance of the receiver.

The above relationship is more often specified as a 3rd order intercept point (I P). This can best be explained by reference to the figure.

Curve A (Figure 8) represents the signal level of one of the two fundamental signals. These signals are increased above the noise floor until a point is reached (C) where the 3rd order intermodulation product (IMP) starts to emerge from

the receiver noise. When the IMP is 10 dB above the noise floor, it is at the same level as the usable sensitivity. The difference in this level and the fundamental is the value found in 4 of the test procedure. As the fundamental amplitude is increased, so does the IMP, at a rate three times faster. At the theoretical point D on the graph, the IMP and the fundamental meet. (This is theoretical as the input amplifier of the receiver will go into gain compression well before this point). Point D is the 3rd order intercept point. (IP) It can be referred to input or output. The input intercept differs from the output intercept by the small signal power gain of the stage in question. For a more comprehensive study of intermodulation refer to 3,4.

CONCLUSION

Techniques for testing receivers have not changed significantly over the last 10 years. The introduction of synthesized signal generators in the 1970's by companies such as Racal and Hewlett Packard were a major step forward. Until then, at VHF and UHF, signal generators had to be left on permanently, to ensure they were stable enough to test the crystal controlled receivers. The synthesized signal generator manufacturers were already specifying noise performance capable of handling today's 20 KHz spacings. History is now repeating itself. Todays communication systems are poised on the edge of a technology breakthrough, but the signal generators available are only able to handle the 20 KHz technology. SSB systems have been around for many years and now are becoming very popular in the commercial field. As in the 50's and 60's the test equipment presently available for such systems testing is not ideal. Racal-Dana and Hewlett Packard again lead the way with their models 9087 and 8662A. The military have actually progressed to even higher technology systems that implement frequency agile and spread spectrum techniques.

Anyone considering measuring todays communications systems must not forget the future; nor should the instrument manufacturers. Signal generators are now needed with good noise performance for narrowband systems, fast switching speed for frequency agile systems and digital modulation capability for spread spectrum.

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SIMPLE APPROACHES TO LIMITING RADIATION FROM FOIL-SHIELDED COMPUTER CABLES

by

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John Juba Jr.

Electromagnetic (EM) susceptibility has typically been a difficult problem in the development of high-reliability communication, navigation, and electronic warfare equipment. The military susceptibility standard, MIL-STD-461B, outlines most government electromagnetic interference (EMI) requirements. This document is augmented by MIL-STD-462 which describes acceptable testing procedures.

Military EMI requirements can be ten times more stringent than commercial standards. These military requirements result from two prime factors. The first is that, in a typical military communications center, the equipment is installed close together creating a worse-than-normal EM environment. The second is to assure reasonable equipment immunity to a potential hostile environment due to electronic countermeasures.

Besides having to meet the more familiar EMI standards, many of these equipment must also comply with TEMPEST requirements. The TEMPEST requirements are part of a classified U. S. government security program. They deal with controlling the emission and detection of energy from communication and data processing equipment which could reveal classified information being processed by the equipment. All too often, TEMPEST guidelines for equipment installation and interconnection (part of this control of emissions) are considered adverse to typical installation criteria.

MIL-HDBK-419, although not a TEMPEST specification, contains equipment and cable shield grounding recommendations which are highly compatible with the TEMPEST guidelines and represents a more modern approach to facility design. This document clearly states that the only differences in grounding techniques between those employed at facilities processing National Security related information (RED equipments) and any other facility are the grounding configurations used to

terminate cable shields. These configurations are applicable when the equipment involved is referenced to an equipotential ground plane. (MIL-HDBK-419 defines and describes the equipotential ground plane.)

Although the majority of MIL-HDBK-419 deals with design considerations for new facilities, implementation of recommended installation techniques in existing facilities is also described. Concerning the ground systems installed in most existing facilities, this standard states,

"... While these systems generally do not meet today's standards and requirements, they will continue to be in use for many years at existing facilities. Information on and description of these systems is therefore included for maintenance purposes only . . . . Any major building or facility rehabilitation should include upgrade of the grounding system to include use of the equipotential plane . . . . "

Relating cable shield grounding configurations to the use of a facility equipotential ground plane is fundamental to reducing EM radiation from interface cabling. With this concept in mind, a test setup was designed to study what standard approaches to EM radiation reduction could easily be implemented at older communication facilities.

The test configuration was developed with the intent of establishing a controlled, easily varied test setup. The approach chosen was to enclose each a line driver unit, a line receiver unit, and system power supply. These would then be placed in a shielded enclosure along with a cable under study. Manual scanning with a receiver system was chosen over a spectrum analyzer because a greater resolution of the E-field radiation profile was desired. Figure 1 depicts the general orientation of the cables, interface units, and test equipment. The line driver and line receiver units were secured to a copper-clad test bench bonded to the walls of the shielded enclosure and elevated one meter above the floor. This test bench acted as the equipotential plane of the test setup. The parameters to be varied during the course of testing were 1)the presence or absence of a line-terminating resistor, 2)the cable shield terminations, and 3)the use of filterpin connectors versus non-filterpin connectors.

Two computer I/O cables chosen for the study were supplied by a customer as cables typically used in their communications center. The first cable tested (BRAND-REX telephone cable 11PR-24AWG 200 C) contained 13 pairs of stranded wire. These wires were not twisted pairs. The cable had only a single Beldfoil shield with a stranded drain wire surrounding the wire conductors. This cable was terminated with ITT connectors (#MS 3475L16-26S) at both ends. The overall length of the cable was 28.5 feet (8.7 m).

The second cable had 27 twisted wire pairs which were each shielded with Beldfoil and had individual stranded drain wires. In addition, the 27 pairs and their shields were collectively shielded by an overall cable shield of Beldfoil with an associated stranded drain wire. This cable was also provided by the customer and came terminated with Amphenol connectors (#3475L22-55S 8206-2) at both ends. The overall length of the cable was 29.25 feet (8.9 m).

In order to test the effectiveness of different configurations of shield terminations, the I/O cable needed to carry digital data of a standard format. For this purpose, a line driver unit and a line receiver unit were constructed in small RF-tight boxes in such a manner as to assure that emanations detected during E-field tests were produced strictly by the cable and not either unit. The line drivers and line receivers used mmeet the requirements of EIA Standard RS-422. (Balanced transmission of data was chosen because of the greater noise immunity.) The line driver unit and the line receiver unit were fitted with one 26-pin connector and one 55-pin connector on an end wall of the boxes. This permitted connection of either I/O cable to the units. The two connectors were wired in parallel with correspondingly lettered pins connected together. (Unused pins on the 55-pin connectors were left open in the boxes.) With this arrangement, one or several pairs of conductors could be used for the evaluation if need be.

The line receiver unit was also equipped with a BNC connector. This connector allowed the receive data to be monitored. The schematic (Figure 2) shows the chips

used and their interconnection. Power was supplied to the circuit boards in the manner described below.

A regulated supply provided filtered +7.3v, -7.3v, and COMMON to the line driver unit (these voltages slightly exceed the devices' ratings and were considered to yield "worst-case" results). In addition to connection to the card edges, these leads were wired to three pin letters (six pins) of the multi-pin connectors. Power was then supplied to the line receiver unit via the I/O cable and multi-pin connectors.

System Grounding

Grounding of the system was treated as follows. Inside the line driver unit, three pieces of stranded wire connected the filtered COMMON of the power supply to the inside of the box, to circuit ground on the board, and to the conductors designated as COMMON from the multi-pin connectors. Inside the line receiver unit, a piece of stranded wire connected the COMMON cable conductor (at the card-edge connector) to the box. The line driver unit and the line receiver unit were each placed on insulating material on top of the test bench. These units were then grounded to the copper test bench by 0.5-inch ground straps.

The cable shields were to be grounded at the line driver and/or line receiver units' bulkheads. Because of the Beldfoil shield construction of the cable, drain-wire connections to ground were concidered to be the simplest termination mode available. A 3.5 cm. drain wire length was used as a minimum pig-tail termination. The wire termination was then passed through the rear of the backshell to act as the shield ground termination. These shields, their drain wires, and the ground-wire connection were insulated with electrical tape so as to be isolated from the overall cable shield. 3.5 cm. wires were also used at both ends of the overall cable shield and passed through the rear of the backshells for use as this shield's ground termination. The overall cable shield, its drain wire, and the ground-wire connections were insulated with electrical tape so as to be isolated from the backshells' conductive coating.

On the 26-line cable, the 3.5 cm. long ground-wires were passed through the rear of the backshells. The shield, drain wire, and ground-wire connections were then insulated with electrical tape and the backshells were replaced. When a cable was to be tested, it was suspended from the screen room ceiling. The cable was looped around the shielded enclosure as nearly to 1 meter from the screenroom walls, floor, ceiling, and test bench as possible. The cable ends were attached to the line-driver unit and line-receiver unit, which were clamped to the test bench.

The shield ground wires were terminated in spade lugs. This permitted the shield terminations to be reconfigured by fastening the appropriate lug to the connector backshells at a cable restraint screw. For the 26-line and the 55-line cable shields, tests were performed using various shield termination configurations with and without a matching resistor present.

The antenna was positioned approximately 1 meter from the cable and 1 meter from the test bench. Figure 3 illustrates the orientation of the cable, antenna, and interface units within the shielded enclosure. Test data were repeatable, provided that the particular I/O cable under test maintained a constant orientation. If, for example, a series of tests were performed on one of the cables during which several of the parameters under study were changed and then the tests for the first parameter change were repeated, the results of the two tests would be within 3 dB of each other. If one cable was fully tested and then the other cable was fully tested, any attempts to repeat tests of the first cable would give a somewhat different radiation profile because of the different orientation of the cable with respect to the antenna and shielded enclosure. Even though the radiation profile would be different for the reconfigured cable, the relative test results remained the same.

Digital Signal Line Conduction (DSLC) Tests

Two sets of DSLC tests were performed. Both sets were run at a data rate of 9.6 kbit/sec. Test parameters were based upon the operating data rate of 9.6 kbit/sec. For these tests, high-pass filter sections were inserted at 10 kHz, 100 kHz, 1 Mhz, and 10

instance, there was a general increase (6 - 15 dB) in emanation levels for all but the top decade (30 - 300 Mhz) when Z was omitted. The least sensitive configuration when filterpins were not used was with the shield grounded only at the source end (Figure 7). Here, the omission of Z results in additional emanations from 0.010 to 0.050 Mhz and 4 - 8 dB enhancement of frequencies from 3 - 8 Mhz and from 40 - 60 MHz.

When filterpin connectors were used with the 26-line cable, none of the grounding configurations showed variations beyond 2 Mhz attributable to the presence or absence of Z. Grounding the cable shield at both ends seemed to result in the least sensitivity of all configurations (filtered or unfiltered). For this case, the inclusion of Z prevents enhancement of frequencies between 0.300 and 1.0 MHz as shown in Figure 8.

55-Line Cable Results, Z

The effect of Z on the 55-line cable was greatest when non-filterpin connectors were used. Comparison of the unshielded ER profiles with and without Z in place is shown in Figure 9 and reveals a gross increase in emanation levels over a fairly wide spread (i.e., 10 - 25 dB from 0.010 - 10 MHz). The increases were predominantly for frequencies below 10 MHz, with the exception of a 10 dB decrease near 60 MHz and a 15 dB increase near 150 MHz, both attributable to the exclusion of Z. This configuration, with all of the shields unterminated and without filterpins, was the most sensitive to the presence or absence of Z. Of the other configurations where filterpins were not used, some were far less sensitive. Even for the least sensitive unfiltered configuration (see Figure 10), large peaks were reduced by the inclusion of Z. In this configuration, the overall cable shield is open and the individual shields are grounded only at the source end. The frequencies of interest lie throughout the profile, with 10 and 15 dB increases near 5, 16, 20, and 60 MHz attributable to the omission of Z.

Where filterpin connectors were used with the 55-line cable, the effect of Z was less obvious. The more dramatic examples are configurations with the individual shields grounded at both ends and the overall cable shield open at one end. A comparison of these test

cases is shown in Figure 11. For these configurations, the increases were 6 - 15 dB in magnitude and occurred primarily for frequencies from 0.200 - 2.0 MHz. For the other configurations where filter-pin connectors were used, the presence or absence of Z was less critical. The least sensitive of the filtered configurations was with the individual shields grounded only at the source end and the overall cable shield grounded at both ends (see Figure 12) where the inclusion of Z reduced emanations from 4 - 9 MHz by 2 - 4 dB.

EFFECT of GROUNDING CONFIGURATION

The results of grounding cable shield terminations in various combinations are discussed below. These effects vary between the two cables and between test cases where filterpin and non-filterpin connectors were used. The simpler, 26-line cable tests are discussed first.

26-Line Cable Results, Shield Termination Configurations

For the singly-shielded, 26-line cable, the greatest shielding effectiveness resulted from grounding the shield at both ends. When non-filterpin connectors were used, grounding both ends of the shield was most effective for frequencies below 6 MHz compared to the unshielded profile as shown in Figure 13. Here, the very lowest decade (0.010 - 0.100 MHz) of emanations is completely eliminated. There is some shielding effectiveness above 10 MHz, but these frequencies are still at unacceptably high levels.

When non-filterpin connectors were used with the 26-line cable, grounding a single end of the cable shield was most effective below 1 MHz. Note the results of these test cases, also shown in Figure 13. There was a loss of shielding effectiveness (as much as 30 dB) from 1 to 20 MHz when only one end of the shield was grounded.

When the 26-line cable was connected using filterpins, the most effective grounding configuration using filterpins was where the cable shield was grounded

at both ends. Comparison of the graphs of Figure 14 shows attenuation as great as 38 dB for frequencies below 7 MHz. This eliminates the lowest decade (0.010 - 0.100 MHz) of emanations, and reduces the levels of the remaining emanations.

When filterpin connectors were used with the 26-line cable, grounding one end of the cable shield was most effective below 0.200 MHz (Figure 14). It made little difference which end was grounded, but grounding only a single end resulted in a loss of attenuation (as much as 40 dB) from 0.100 MHz to 10 MHz. In each instance, there was only a narrow band of frequencies from 0.300 - 0.600 MHz where mild enhancement (maximum of 8 dB) over the unshielded profile occurred. However, when these configurations were compared to similar configurations where filterpins were not used (Figure 13), they demonstrated a drastic loss of shielding effectiveness from 0.100 - 1 MHz when only a single end of the shield was grounded. This effect is apparently not the result of the grounding configuration alone, but of the sensitivity of these configurations to the presence of the filterpins.

55-Line Cable Results, Shield Grounding Configurations

The 55-line cable, having two (sets of) cable shields, realized its greatest shielding effectiveness when both the overall cable shield and the individual shields were grounded at both ends. Figure 15 depicts these results. When non-filterpin connectors were used, the unshielded profile extended up through 300 MHz. The lowest two decades (0.010 - 1.6 MHz) of emanations were eliminated by grounding all four shield terminations. Attenuation of the radiation profile at certain frequencies above 10 MHz exceeded 20 dB.

If the individual shields are grounded at both ends (non-filterpins still used), opening one end of the overall shield does not drastically reduce the attenuation. In fact, opening both ends of the overall cable shield (Figure 15) does not result in a gross loss of attenuation, provided that both ends of the individual shields are grounded. However, termination of the individual shields is far more critical. Even when both ends of the overall cable shield were grounded (and non-filterpins were used), opening one end of the

individual shields creates problems. Comparison of the graphs of Figure 16 shows a general loss of attenuation (especially from 1 - 10 MHz) and a slight increase in frequency spread. As the overall shield was opened at one end or the other, not only a further loss of attenuation was noted, but a drastic increase in frequency spread (greater than 1 decade in lower frequencies) as well. Figure 17 shows the radiation profile which occurs in the absence of any benefit of the overall cable shield (i.e., open at both ends). Grounding only a single end of the individual shields resulted in a slight decrease in emanation levels when just the source end was grounded and an increase in emanation levels at higher frequencies when just the load end was grounded. This enhancement of the higher frequencies occurred from 22 - 80 MHz with amplitude levels greater than those of the unshielded profile. Enhancement of emanations was a greater problem when filterpin connectors were used with the 55-line cable.

When the 55-line cable was connected with filterpins, the unshielded profile (shown in Figure 18) produced a greatly reduced radiation profile which extended only from 0.010 - 20 MHz. Several grounding configurations further attenuated these emanations, while several enhanced the emanations. This enhancement of emanations from 0.200 to 2 MHz is exhibited by some configurations where, at certain frequencies in the range of enhancement, there is an increase in emanation levels as great as 18 - 20 dB above those of the unshielded profile. These configurations were those where a cable shield was grounded at a single end, but neither the overall cable shield nor the individual shields are grounded at both ends. Note the affect on emanation levels. These grounding configurations were also the least effective from the standpoint of frequency spread. This enhancement does not result from the grounding configuration. Comparison of similar configurations where non-filterpin connectors were used (Figure 17) with the unfiltered, unshielded profile reveals that these configurations should attenuate emanations from 0.200 to 2 MHz.

Of the remaining configurations where filterpins were used, greater attenuation was effected by grounding both ends of the individual shields than by grounding both ends of the overall shield. Comparing the results showed improvements for frequencies below 6 MHz

excluding those between 1 and 2 MHz. The best grounding configurations are shown in Figure 19. These are the test cases where the individual shields were grounded at both ends and the overall cable shield was open at both ends or grounded at both ends. In these cases, there was both a large reduction of frequency spread as well as great attenuation of frequencies below 4 MHz (compare these with the unshielded profile). The addition of the overall cable shield resulted in the elimination of emanations between 2 and 4 MHz.

EFFECT of FILTERPIN CONNECTORS

Both cables were tested using filterpin connectors. The effect of these filterpins upon the ER profiles of the different grounding configurations is seen by comparing a filterpin test with its non-filterpin counterpart. For such comparisons, it is necessary to include certain bandwidth correction factors in order to account for the different bbandwidths used in collecting data. A correction factor of 12 dB should be added to the filterpin results when they are compared to the non-filterpin results within the frequency range of 0.900-30 MHz. The tests of the 26-line cable will be discussed first.

26-Line Cable Results, Filterpins

The most prominent and consistent effect of the filterpins was a general reduction of the overall frequency spread of the ER profiles as can be seen in Figure 20. When the 26-line cable was connected with non-filterpins , the ER profile spanned from approximately 0.010 - 300 MHz. Inclusion of the filterpins reduced this, allowing the profile to extend only to 20 MHz . For this configuration, with the cable shield open at both ends, the filterpins cause a slight enhancement (maximum of 9 dB at 500 kHz) of emanations from 0.100 - 2 MHz over the unshielded profile without filterpins. This is far more pronounced for other configurations.

In two instances shown in Figures 21 and 22, use of filterpins resulted in a gross enhancement of emanations between 0.100 - 2 MHz. When the cable shield was grounded at one end alone, these emanations were 10 - 40 dB higher (remember to include the bandwidth correction factor) than those of corresponding non-filterpin configurations.

When the cable shield was grounded at both ends, the filterpins caused an enhancement of the emanations from 0.250 - 4 MHz (see Figure 23). For this filterpin test case, emanations were first detected at 0.095 MHz versus 0.250 MHz. As in the other cases, the filterpins completely eliminated measurable emanations beyond 20 MHz. Also, the filterpins caused slightly less attenuation of the emanations near 16 MHz (approximately 22 dB) than the other filterpin configurations (28 - 30 dB). The overall levels near 16 MHz were about the same in all four cases shown in Figure 14.

55-Line Cable Results, Filterpins

When the 55-line cable was connected with filterpins, there was a large reduction in the frequency spread of the emanations, as well as frequent enhancement of the remaining emanations over those of corresponding unfiltered profiles. Figure 24 exemplifiess this. When filterpin connectors were not used, the unshielded ER profile spanned from approximatelv 0.010 - 300 MHz. The filterpin connectors limited the range of emanations to 16 MHz. (The correction factor of 12 dB must be added to all filterpin results between 0.900 and 30 MHz before comparison with non-filterpin tests.) In the configuration with both the overall shield and the individual shields open at both ends, this filterpin radiation profile was used as the basis of comparisons to determine enhancements attributable to the filterpins for the various permutations of sheild terminations.

The use of filterpins in all these grounding configurations increased emanation levels somewhat over those comparable cases where filterpins were not used. Of those effected, the two configurations which had the least enhancement were those where the individual shields were grounded at both ends and the overall cable shield was either open at both ends or grounded at both ends. (These results are shown in Figure 25 along with the corresponding unfiltered test configuration results.) In these cases, the use of filterpins resulted in emanations occurrino approximately one-half decade lower in frequency than the unfiltered test setup counterpart.

The greatest enhancement of low-frequency emanations occurred when filterpins were used in a configuration where shields were grounded only at a single end. In these cases, gross enhancement (10 - 35 dB) of emanations resulted over the decade of 0.100 - 1 MHz. Another point of interest can be made by examining the results of the filterpin test cases shown in Figure 18. The four cases of interest have a peak emanation occurring approximately at 0.250 MHz with levels 12 - 15 dB greater than those at the same frequency for the test case where no filtering and no shielding was used (see Figure 17). The interesting aspect of this is that 0.250 MHz is the frequency corresponding to the transitional rate of the data bits.

For all grounding configurations of the 55-line cable, the filterpin connectors attenuated emanations above 20 MHz so that they were no longer detectable. It may be worth noting that emanations near 16 MHz underwent varying degrees of attenuation. This attenuation ranged in value from 30 dB (Figure 26) to 36 dB (Figure 25). The filterpins have typical insertion losses of 25 - 30 dB near this frequency.

CONCLUSIONS

Use of Z with the 26-Line Cable

The 26-line cable, having wire-pairs of unspecified characteristic impedance, presented a potential mismatch at the source end of the cable, as well as at the load end. In every test configuration, inclusion of a 100-ohm matching resistor provided at least a minor reduction of emanation levels. When filterpin connectors were used, the benefits of Z become less obvious. It is suggested that the characteristic impedance of the filterpins (10 - 100 ohms) placed at both ends of the cable predominates in the transmission line parameters by reducing the impedance mismatch at both ends of the cable. However, because there is no certainty that the filterpins will be matched from connector to connector, or line to line, it is recommended that the 100-ohm matching resistor, Z, be connected across the differential pairs of the 26-line cable.

Use of Z with the 55-Line Cable

The 55-line cable, whose wire-pairs are specified as having a 100-ohm characteristic impedance, presented a potential mismatch at the load end of the cable. Omission of the 100-ohm matching resistor generally resulted in higher level emanations with no noteworthy increase in frequency spread. When filterpin connnectors were used, improvements arising from the inclusion of Z were less obvious. Again, it is believed that the characteristic impedance of the filterpins, imposed upon the cable prior to Z, reduces the impedance mismatch. However, because of the uncertainty of filterpin pairing (line to line and end to end), it is recommended that a 100-ohm matching resistor be placed across the differential pairs at the load end of this cable.

INFLUENCE OF SHIELD GROUNDING CONFIGURATION

26-Line Cable Shield Termminations

When using the singly-shielded, 26-line cable, it was always best to ground the cable shield at both ends. A great deal of attenuation was forfeited by grounding only a single end of the shield. Some attenuation was noted at the high frequencies present when non-filterpin connectors were used. However, any appreciable attenuation due to shielding effectiveness extended only to 6 or 7 MHz for the non-filterpin test cases. When filterpin connectors were used, attenuation of emanations by the shields extended only up to 0.300 MHz.

55-Line Cable Shield Terminations

The shields of the 55-line cable were most effective when the two shields were grounded at both ends of the cable. When non-filterpin connectors were used, the influence of different shield grounding configurations were discernable up through 100 MHz. The effectiveness of shield grounding was predominant at frequencies below 6 MHz. Grounding a single end of the shields caused a loss of attenuation. Termination of the individual shields was most crucial, probably due to greater capacitive coupling between the shields and wire-pairs.

When filterpin connectors were used with the 55-line cable, shield grounding was especially important. The worst configurations were those where a shield was grounded at a single end and neither the overall cable shield, nor the individual shields were grounded at both ends. These configurations actually resulted in enhancement of frequencies (from 0.2 - 2 MHz) over the unshielded profile. This enhancement was not noted for similar grounding configurations using non-filterpin connectors,and seemed attributable to the presence of the filterpins. The effects of grounding configuration were observable only up to 20 MHz because of the large reduction of frequency spread attributable to the filterpins. The greatest shielding effectiveness resulted from grounding all of the shields at both ends. The improvement of this configuration over others was discernable only to about 3 MHz.

EFFECT of FILTERPIN CONNECTORS

Lowpass filterpin connectors proved to be the single most effective method of reducing unwanted emanations. No configuration of shield terminations was nearly as effective as the filterpins. Even with the shields unorounded, major reduction of emanation levels and overall frequency spread were achieved through the use of filterpin connectors. From the EM shielding perspective, the advantages of this attenuation far outweigh the few disadvantages that surfaced.

From the systems perspective, the filterpin connectors are potentially undesirable in a balanced data transmission system where they may contaminate the system grounds with common-mode currents. While these currents were not actually measured, they seem to have been responsible for enhancement of emanations in some instances. When filterpin connectors were used with either cable, all shield termination configurations resulted in at least some increase in emanation levels from 0.150 - 1 MHz. Configurations where a shield was terminated at a single end were most sensitive. Use of filterpin connectors in these configurations resulted in emanation levels dramatically increased (for the above frequency range) over those of similar configurations where filterpins were not used. In fact, emanation levels of the more sensitive configurations with the filterpin connectors exceeded even those levels in the

0.1-1 MHz range of the test case where no filtering and no shielding were used. It is believed that these shield termination configurations create an effective E-Field radiator. In so doing, the shields act as an antenna, driven at either end by common-mode currents from the filterpins to ground. This effect, although extremely detremental to shielding effectiveness, can be avoided by grounding all cable shields at both ends.

Aside from the reduction of emanations by filtering, another advantage of filterpins became apparent when the effects of an impedance matching resistor, Z , were studied. Emanations resulting from a potential impedance mismatch were reduced by the presence of filterpin connectors. The filterpins are specified as having a characteristic impedance between 10 and 100 ohms. Placement of this impedance at both ends of the transmission line-pairs tends to reduce the VSWR. While they are not likely to be custom-matched from end to end, or line to line, all of the filterpins have a characteristic impedance of the same order of magnitude (also coincident with the output impedance of the RS-422 line driver).

In the final analysis, the advantages of filterpin connectors far outweigh the disadvantages. With the proper shield configuration, the inclusion of filterpin connectors results in outstanding attenuation of unwanted emanations. The shielding effectiveness of any of these termination configurations is, however, based on the use of an equipotential ground plane as suggested in MIL-HDBK-419.

The next obvious step in an evaluation of techniques to reduce radiation from cables is to drive multiple signal lines. For this test situation, a rise in radiated field strength is expected with the increase in the number of driven lines. This increase would be attributed to the fact that all the signal lines share a common shield.

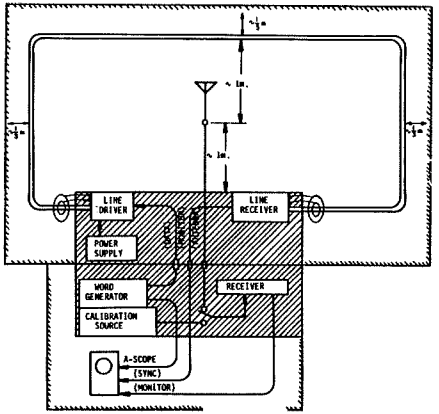

Figure 1. (U) Orientation of Cables, I/O Units, and Test Equipment

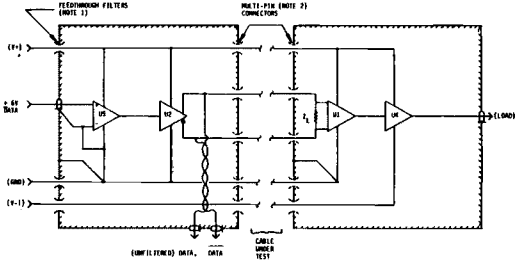
FEEDTHROUGH FILTERS (NOTE 1)
MULTI-PIN (NOTE 2) CONNECTORS
(GND)
(UNFILTERED) DATA,
DATA
CABLE UNDER TEST
U2 AM26LS1 DC QUAD HIGH SPEED DIFFERENTIAL LINE DRIVER
U3 AM26LS32 ACD QUAD DIFFERENTIAL LINE RECEIVER
U5 AM26LS32 ACD QUAD DIFFERENTIAL LINE RECEIVER
U4 AM26LS79 PC QUAD 3-STATE SINGLE-ENDED RS-423 LINE DRIVER
NOTE 1: BULKHEAD-MOUNT, FEEDTHROUGH FILTERS (3), SCI-51-311-322
NOTE 2: WHEN USED, FILTERPINS ARE AMPHENOL 682-22

Figure 2. (U) Representation of Line Driver and Line Receiver Unit

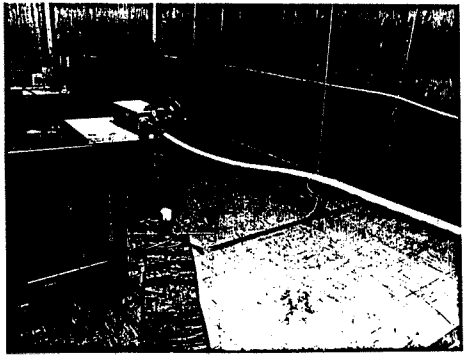

Figure 3. (U) Test Setup Depicting Relative Position of I/O Cable to the Antenna and Shielded Enclosure

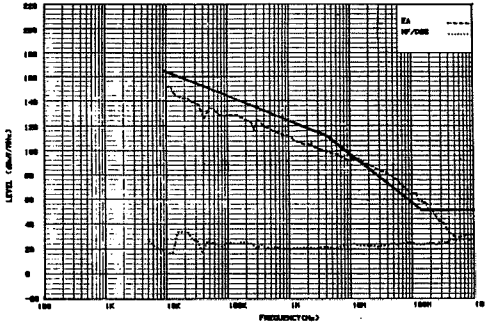

Figure 4. DSLC Test, Driver Baseband Output

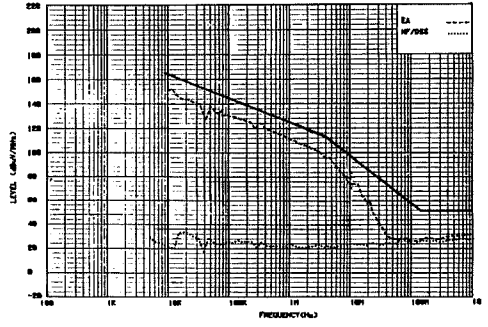

Figure 5. DSLC Test, Filterpin Baseband Output

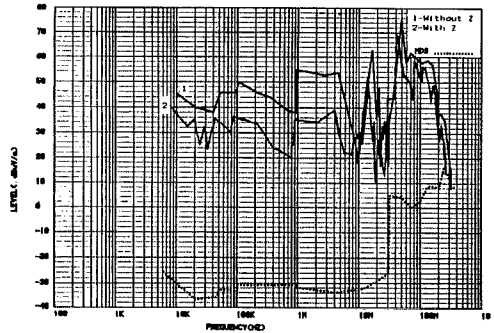

Figure 6. Affects of Z on the Radiation Profile of the Unshielded Cable.

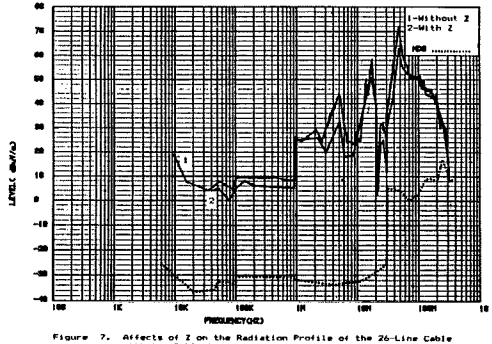

Figure 7. Affects of Z on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at the Source.

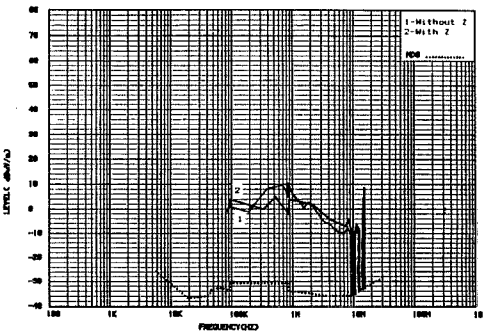

Figure 8. Affects of Z on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at Both Ends and Filterpin Connectors Used.

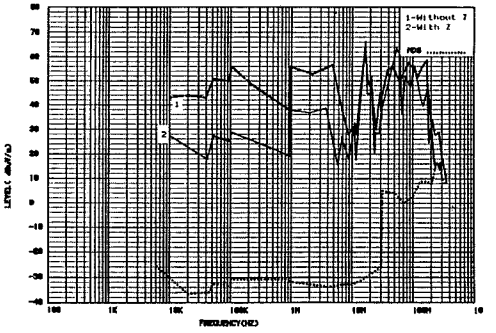

Figure 9. Affects of Z on the Radiation Profile of the Unshielded 55-Line Cable.

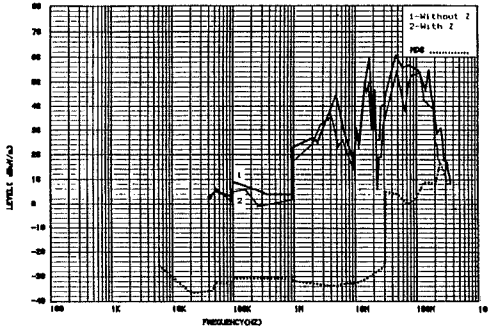

Figure 10. Affects of Z on the Radiation Profile of the 55-Line Cable with the Overall Shield Unterminated and the Individual Line-pair Shield Terminated at the Source.

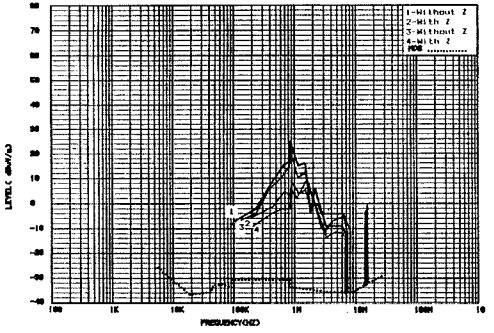

Figure 11. Affects of Z on the Radiation Profile of the 55-Line Cable with Filterpin Connectors Used. Here the Individual line-pair shield is terminated at both ends and the overall shield is terminated at either the Source (1 and 2) or Load (3 and 4).

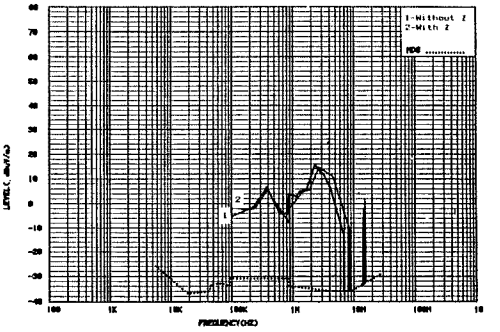

Figure 12. Affects of Z on the Radiation Profile of the 55-Line Cable with the Filterpin Connectors Used. Here the Individual line-pair shield is terminated at the Source only and the overall shield is terminated at both ends.

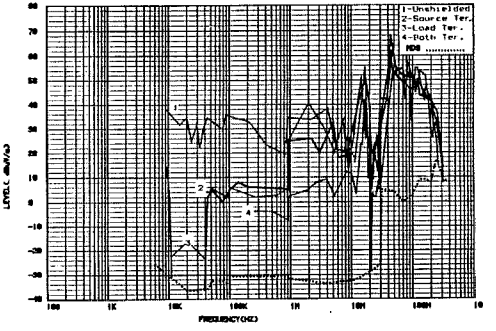

Figure 13. Affects of Shield Termination Configurations on the Radiation Profile of the 26-Line Cable.

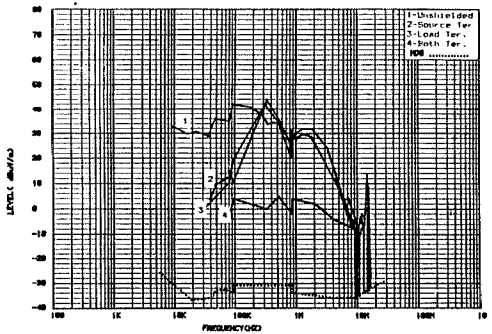

Figure 14. Affects of Shield Termination Configurations on the Radiation Profile of the 26-Line Cable with Filterpin Connectors Used.

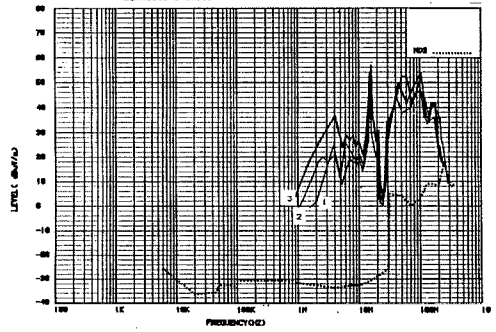

Figure 16. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable. Here the profile resulting from both shields terminated at both ends (1) is compared to the cases where the line-pair shield is terminated only at the Source (2) or the Load (3) and the overall shield is terminated at both ends.

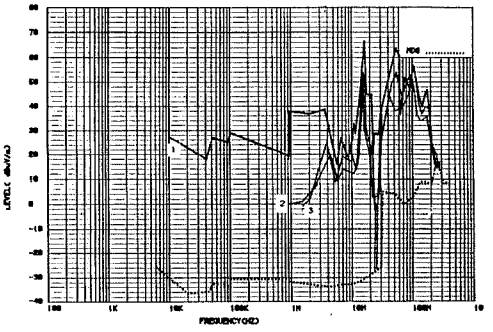

Figure 15. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable. Here the unshielded profile (1) is compared to the cases where just the line-pair shield is terminated at both ends (2) and both shields are terminated at both ends (3).

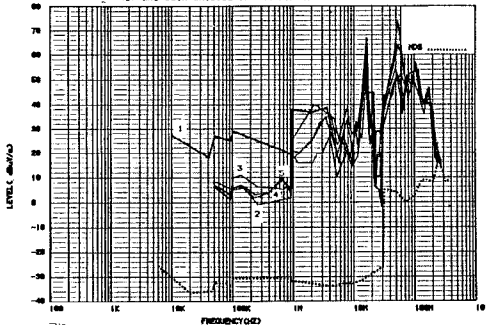

Figure 17. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable. Here the unshielded profile (1) is compared to the cases where the line-pair shield is terminated at just the Source (2 and 5) or the Load (3 and 4) and the overall shield is left unterminated (2 and 3), terminated at just the Source (4), or terminated at just the Load (5).

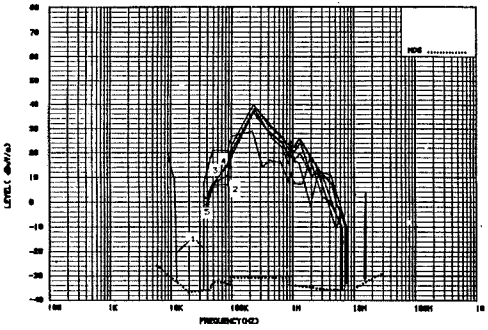

Figure 18. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable with Filterpin Connectors Used. Here the unshielded profile (1) is compared to the cases where the line-pair is terminated at just the Source (2 and 5) or the Load (3 and 4) and the overall shield is left unterminated (2 and 3), terminated at just the Source (4), or terminated at just the Load (5).

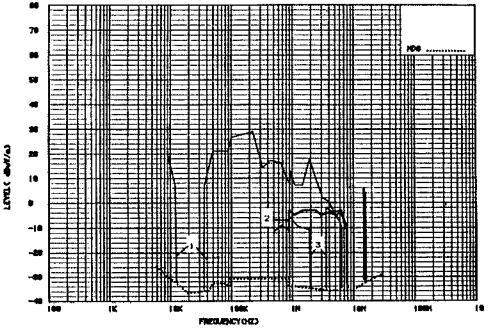

Figure 19. Affects of Shield Termination Configurations on the Radiation Profile of the 55-Line Cable with Filterpin Connectors Used. Here the unshielded profile (1) is compared to the cases where just the line-pair shield is terminated at both ends (2) and both shields are terminated at both ends (3).

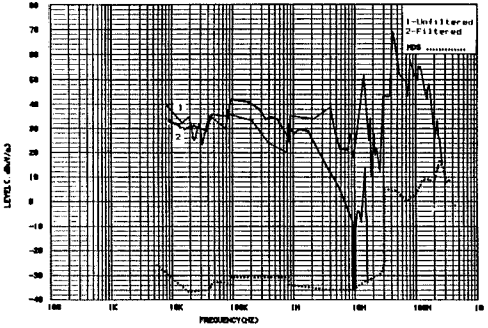

Figure 20. Affects of Filterpin Connectors on the Unshielded Radiation Profile of the 26-Line Cable.

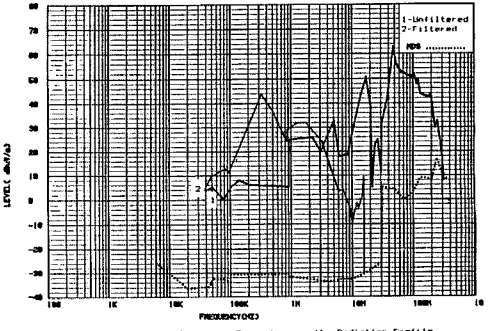

Figure 21. Affects of Filterpin Connectors on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at Just the Source.

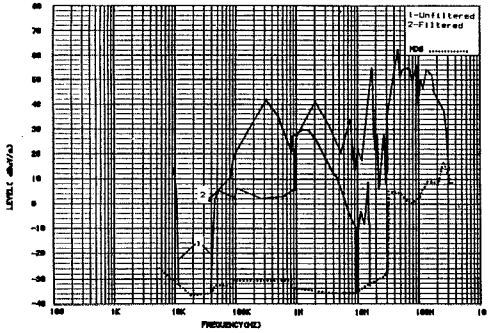

Figure 22. Affects of Filterpin Connectors on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at Just the Load.

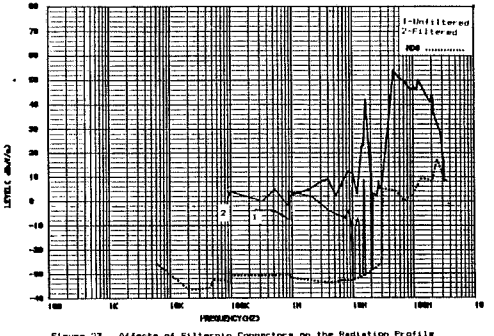

Figure 23. Affects of Filterpin Connectors on the Radiation Profile of the 26-Line Cable with the Cable Shield Terminated at Both Ends.

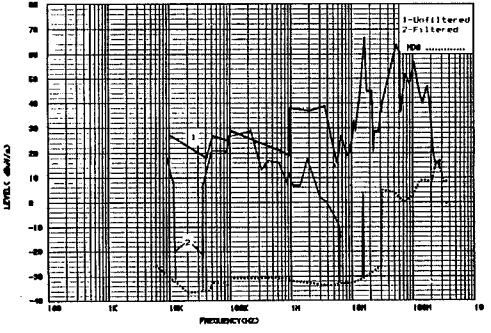

Figure 24. Affects of Filterpin Connectors on the Unshielded Radiation Profile of the 55-Line Cable.

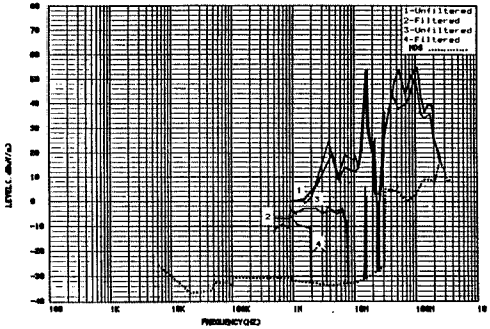

Figure 25. Affects of Filterpin Connectors on the Radiation Profile of the 55-Line Cable. Here the cases shown are with just the line-pair shield terminated at both ends (1 and 2) and with both shields terminated at both ends (3 annd 4).

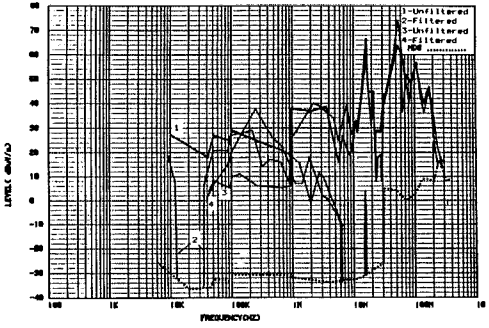

Figure 26. Affects of Filterpin Connectors on the Radiation Profile of the 55-Line Cable. Here the cases shown are for the unshielded profiles (1 and 2) compared to the profiles resulting from only the line-pair shield being terminated at the Source (3 and 4).

NEW INSIGHTS INTO 'OLD' NETWORK ANALYSIS TECHNIQUES

by
Lorenzo Freschet
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Network Analyzers have been commonly used in the characterization of linear components such as filters, amplifiers, attenuators, switches, semiconductors, transmission lines and antennas over the RF and microwave frequency range. They measure the energy reflected from and transmitted through the device under test (DUT). By analyzing the amplitude ratios and phase differences between incident and the reflected and transmitted waves, the complete impedance and transmission characteristics of the DUT can be determined. Network analysis techniques started with slotted lines and gain-phase voltmeters at CW frequencies, but became popular as swept frequency characterization came about.

A network analyzer will always have four key parts:

1. A swept frequency source that provides the stimulus to the DUT.
2. A signal separation device that samples the incident, reflected, and transmitted signals to be measured.
3. A reciever to measure the amplitude and phase of the separated signals.
4. A display to show the data in rectilinear (Cartesian), polar or Smith Chart format.

See Figure 1. Network Analyzer Diagram

More recent network analyzers combine these elements into integrated packages for better performance and add significant enhancements. The following measurement applications areas are used to illustrate these new capabilities.

Filters

The high performance RF systems being designed are placing significant requirements on filter measurement accuracy.

One of the key elements is the frequency accuracy. Analog swept sources have great difficulty in measuring many modern filters (e.g. crystal and SAW) both because of their frequency accuracy and residual FM. Synthesizer sources are required, but at the expense of speed since they step along at CW intervals. Other techniques use a frequency counter to help guarantee accurate frequency information. Now network analyzers

incorporate swept synthesizers which offer the convenience of analog sweep and the precision of synthesizers at the same time.

SAW filter measurements are particularly difficult. Due to the different paths signals can take in the device, distortion in the frequency domain can occur which is very difficult to detect. These are called spurious time-domain responses. With their inverse Fourier transform ability, network analyzers can measure both the frequency and time-domain responses.

See Figure 2. SAW Filter Measurement in Frequency and Time Domain

Group delay measurement is often required to check for distortion. Previously, additional equipment was required that passed a modulated signal (FM or AM) through the DUT. Not only was this technique cumbersome, but often of unsuitable accuracy and repeatability from system to system. Deviation from linear phase was rarely used as a distortion parameter since it was almost impossible to equalize out the linear component of phase by simple methods. Now that network anlyzers incorporate a built-in computer, they can determine the DUT's group delay response more precisely from the phase information. This technique is fast and utilizes the accuracy enhanced data for the most accurate and repeatable results. In addition, deviation from linear phase is simple now with built-in electrical length control to balance virtually any length offset.

See Figure 3. Group Delay and Deviation from Linear Phase

Transistor S-Parameter Measurements

High frequency transistors are commonly used by RF engineers in their own designs. For the most part, they rely on manufacturers' measurements on an individual device. Typically, the set of S-parameter measurements are often incomplete leaving the user to measure his own. For these, the system measurement uncertainty can often be large. The errors due to imperfect couplers and non-ideal mismatches can add significantly. Using fixtures, adapters and cables only compounds the problem. Only by analyzing the errors and making worst-case assumptions does the designer know the uncertainties of his measurements. If these errors are large, they force him into designing with unnecessarily large safety margins. This can unnecessarily complicate things and also keep the end product from meeting its performance objectives.

Previously, the only alternative was to reduce the measurement errors by obtaining better hardware and reducing the number of adapters and cables between the measurement instrument

and the device. Generally, this isn't enough. Tuners can be employed at a particular frequency, but not over the wide bandwidths needed. Only until automatic network analyzers, driven by computers, could these uncertainties be further reduced. They offered a calibration technique called vector accuracy enhancement which used external calibration standards (open, short, load) to actually measure the measurement uncertainties and vectorially subtract them from the measurement data for very high accuracy. This was a popular technique with disadvantages of requiring a programmable network analyzer, a computer, and quite slow measurements.

Now complete vector accuracy enhancement techniques using short, open, and load calibration standards are built inside network analyzers to provide the low levels of uncertainty needed for the best device characterization. Once integrated inside, the measurement speed increased substantially allowing users the speed to see the measured parameters in real time. This technique also has the advantage of allowing very accurate measurements after adapters and in different connector types.

See Figure 4. Transistor Measurement Before and After Accuracy Enhancement

Antennae Measurements

When measuring antenna gain, match or patterns, extraneous or reflected signals can alter the data, giving erroneous results. This is why anechoic chambers usually are used to attenuate the unwanted signals.

Modern network analyzers now have the ability to transform their frequency domain data into time domain reponses using the inverse Fourier transform. With this, the unwanted reflections can be viewed and analyzed. If a particular portion of the time domain is all that is desired, a GATING function can mathematically filter out the undesired signals in time. This gated response can then be transformed back and allow analysis of the measurement in the frequency domain with the effects of unwanted reflections removed. This technique often can give results comparable to those obtained in anechoic chambers.

See Figure 5. Antenna Measurement in Frequency and Time Domain

See Figure 6. Antenna Measurement After GATING Unwanted Signal in Time and Frequency Domain

Fiber Optic Measurements

Fiber optic media is commonly used to transmit high speed

digital information. To characterize the transmission path and the components, pulse dispersion techniques using high speed pulse generators and high speed oscilloscopes are used.

Now that network analyzers can mathematically transform measured frequency domain information into the time domain, the same network anlyzer can be used to quantify the dispersion of pulses.

In summary, as the need for better network analysis by design engineers grows, so do the techniques available. Only recently have those techniques described here existed inside commercially-available network analyzers. They represent the latest steps in the steady improvement of measurement equipment to assist engineers with their design tasks.

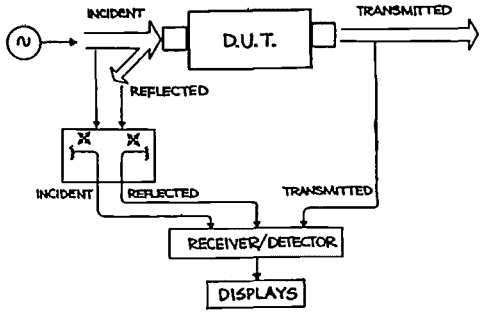

FIGURE 1. NETWORK ANALYZER

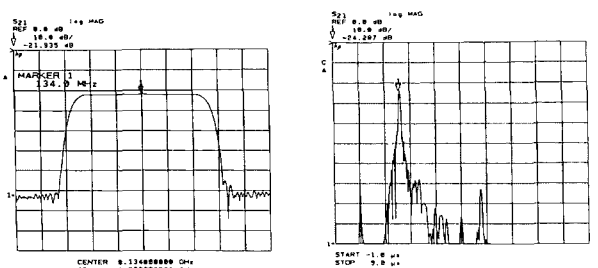

FIGURE 2. SAW FILTER MEASUREMENT IN FREQUENCY AND TIME DOMAIN

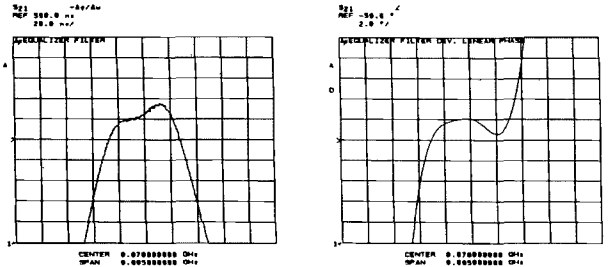

FIGURE 3. GROUP DELAY AND DEVIATION FROM LINEAR PHASE

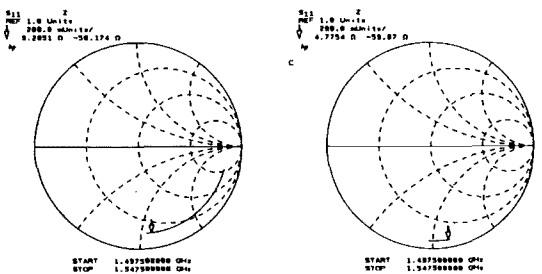

FIGURE 4. TRANSISTOR MEASUREMENT BEFORE AND AFTER ACCURACY ENHANCEMENT

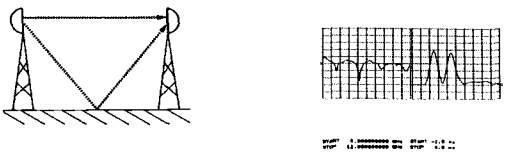

FIGURE 5. ANTENNA MEASURMENT IN FREQUENCY AND TIME DOMAIN

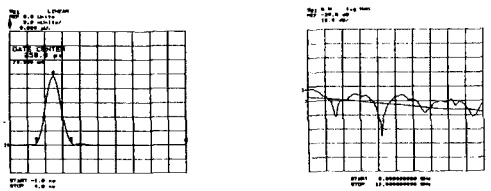

FIGURE 6. ANTENNA MEASUREMENT AFTER GATING UNWANTED SIGNALS IN TIME AND FREQUENCY DOMAIN

A BROADBAND LUMPED ELEMENT VARIABLE ATTENUATOR

by

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A bridged-T variable attenuator was realized in the 1 MHz to 500 MHz band with an attenuation range of about 13dB and a minimum return loss of 21 dB. Due to its small size, broadband operation and good match at both the ports a bridged-T attenuator was chosen.

In a bridged-T network (Fig.1.a) the two variable resistors have to satisfy the following condition for a good match at both the ports : $R_1 R_2 = Z_o$, where Z_o = characteristic impedance. PIN diodes can be used as current controlled variable resistors with resistance typically varying from 10 K ohms to 1 ohm above 20 Hz. Since the forward current in a diode is an exponential function of the voltage drop across the diode, when PIN diodes are used in the bridged-T circuit the product R_1R_2 will be an exponential function of (V_1+V_2) [1].

$$R_1R_2 = K_1 \ e^{KT/(V_1 + V_2)},$$

where K_1 is a constant.

Hence for good match the sum of the voltage drops across the diodes has to be held constant. The DC circuit achieving this function is shown in Fig.1 (b). A_1 is a voltage follower stage which maintains a constant voltage drop across the diodes. A_2 and A_3 form control voltage stages, which vary the currents through the diodes for changing the attenuation.

Two important RF considerations in the realization of a broadband variable attenuator are (1) the design of proper layout to reduce parasitics (2) proper design of broadband DC to RF isolation elements. The attenuator was realized as per the layout shown in Fig.2 on a 31.25 mil thick Teflon fiberglass substrate with 50 ohms input and output microstrip lines. In this layout, the size of patches P_1 and P_2 has been minimised to reduce parasitics. M/S. Salford Electronics Ltd., core types P and K10 were used to realize the low frequency (1 MHz to 150 MHz) and high frequency (150 MHz to 500 MHz) chokes. One each of these high and low frequency chokes were used in series to obtain the broadband (1 MHz to 500 MHz) RF to DC isolation. Siemens type BA379 PIN diodes were used along with M/S. Johanson Chip capacitors and M/S. Pyrofilm 50 ohms chip resistors, to reduce the size. This attenuator had a minimum attenuation range of 0.8 dB to 13.8 dB with $\leq$1.2 dB response over 1 MHz to 500 MHz frequency range. It had a minimum return loss of 21 dB over the 1 MHz to 500 MHz band. The measured performance of the attenuator is given in Table I.

Table I. Measured Performance of the Bridged-T Attenuator

Freq. (MHz)	I/L (dB)	R/L (dB)	I/L (dB)	R/L (dB)	I/L (dB)	R/L (dB)
1	0.5	27	6.0	28	15.0	25
50	0.5	27	6.0	28	15.0	25
100	0.6	26	6.0	29	15.0	24
150	0.6	26	6.0	30	14.9	24
200	0.6	26	6.0	31	14.7	24
250	0.6	25	6.0	34	14.7	23
300	0.7	25	6.0	30	14.5	23
350	0.7	25	6.1	29	14.4	23
400	0.7	24	6.1	28	14.2	22
450	0.7	24	6.1	28	14.0	21
500	0.8	24	6.1	27	13.8	21

Reference: (1) Need a PIN diode attenuator ? R.S Viles
Electronic Design, pp.100, Vol.25, No.7,
March 29, 1977.

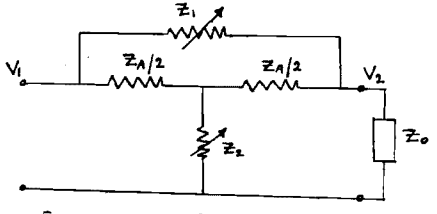

FIG.1(a). BRIDGED-T NETWORK

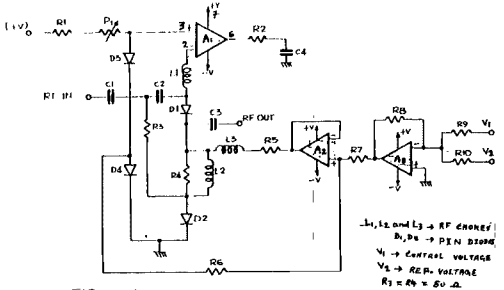

FIG 1(b). BRIDGED-T ATTENUATOR WITH D C CONTROL CIRCUITRY.

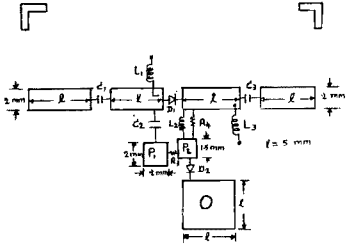

FIG. 2. RF CIRCUIT OF THE BRIDGED-T ATTENUATOR

APPLICATION NOTES FOR DOUBLY ROTATED QUARTZ CRYSTALS

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SUMMARY

Piezoelectric crystal resonators are used primarily for precise frequency control and tuning. The most frequently used piezoelectric material is alpha quartz (silicon dioxide). A quartz crystal acts as a stable mechanical resonator which, by its piezoelectric behavior and high Q, determines the frequency generated in an oscillator circuit. These bulk wave resonators are available in frequency ranges from approximately 1.0 KHz to 500 MHz.

For nearly half of a century two common crystallographic cuts, called AT and BT cuts, have been used extensively for most oscillator and filter applications. The electrical parameters and frequency vs temperature characteristics of these cuts are well known in the technical community.

Recently however, the dominance of the AT cut has been challenged by the newer doubly rotated crystal designs, especially in applications demanding precision frequency control. These doubly rotated designs are known as the IT and SC cuts.

INTRODUCTION

While retaining the more important advantages of the AT cut crystal, the doubly rotated units have proven to be superior in many ways. The doubly rotated cuts show less sensitivity to shock, vibration, acceleration, thermal shock and thermal hysteresis. Less sensitivity to processing and application variables such as electrode and mounting stress, and, more importantly, drive levels, have also given the doubly rotated cuts a significant advantage over the AT cut.

Many excellent papers with valuable data have been presented in preceding years, but the data was usually obtained from small quantity experimental groups. The data contained in this paper is based on larger quantities of 100 or more units of each frequency listed, and comprise only cylindrical type cold weld enclosures.

VIBRATIONAL SENSITIVITY

Although several papers have previously reported on the various influences on vibrational sensitivity, much of this initial work was performed on crystal resonators enclosed in a crystal holder known as a "ceramic flatpack".

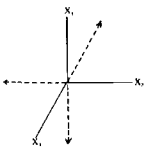
All of the crystals used for this paper were sealed in one of three types of *cold weld enclosures: HC-35/u, HC-37/u or HC-45/u.* All of these enclosures utilize a four point mounting configuration spaced at 90 degrees. From previous work, this mounting method appears to be optimum and correlates well with previous data from government sponsored ceramic flatpacks. Also, the static measurements of "g-tipover" on any given resonator typically correlate to less than 1×10^{-9}/g to its vibrational sensitivity measurement.

Vibrational sensitivity is a vector quantity in three dimensions, different in all axes. Measured differences can be as great as 10 to 1, but typically range from 2×10^{-9} to 1×10^{-8}. These differences are principally due to the moment of inertia acting upon the elastic coefficients of the quartz. Consistency in vector direction appears to have little correlation within a group. We have not found process differences, other than mounting and resonator geometry, to have any appreciable effect on sensitivity.

The quartz crystal resonator is, in reality, a mechanical device which, when mounted in a holder, is subject to mounting resonances. Further, oscillator design engineers must be aware of the possibility of resonances within the oscillator itself. Assuming an internal resonances within the crystal, the oscillator, or the system, the vibration gamma is flat up to 2000 Hz.

Much of our data is provided in the form of customer feedback, and is greatly appreciated for its value in comparison type measurements. Measurement techniques vary considerably from user to user, and differences in resultant gamma can arise dependent on whether the measurements were of the crystal itself, within an oscillator, or within a larger system.

CALCULATION OF VIBRATIONAL SENSITIVITY GAMMA



$$\Gamma = \sqrt{X_1^2 + X_2^2 + X_3^2}$$

$$X_1 = (F_1 - F_2)10^{-9}$$

Difference between frequency in one direction to its 180° (opposite) direction.

VIBRATIONAL SENSITIVITY MEASUREMENTS

FREQUENCY/MODE/CUT	g-SENSITIVITY
HC-35 HOLDER TYPE:	
5 Mhz/Fundamental/SC	3.0×10^{-9}/g +/- 1.0×10^{-9}/g
60 MHz/3rd Overtone/SC	3.5×10^{-9}/g (worst axis)
80 MHz/3rd Overtone/SC	$.95 \times 10^{-9}$/g (average)
95 MHz/5th Overtone/SC	1.9 to 7.7×10^{-9}/g
100 MHz/5th Overtone/SC	1.0 to 5×10^{-9}/g
100 MHz/3rd Overtone/SC	5 to 8×10^{-9}/g (worst axis)
116 MHz/5th Overtone/IT	3×10^{-9}/g (worst axis)
135 MHz/5th Overtone/IT	5.5×10^{-9}/g
HC-37 HOLDER TYPE:	
5 MHz/Fundamental/SC	$.41 \times 10^{-9}$/g
10.000 MHz/3rd Overtone/SC	Measurements have ranged from 3 to 6×10^{-9} gamma to 1.5×10^{-9} gamma
HC-40 HOLDER TYPE:	
10.000 MHz/3rd Overtone/SC	1.5×10^{-9}/g
5.000 MHz/3rd Overtone/SC	1.3×10^{-9}/g

PHASE NOISE

The doubly rotated cuts demonstrate still another area of superiority when utilized in a precision oscillator: phase noise and frequency stability.

It is well known that noise originates not only in the oscillator circuit but in quartz resonators undergoing oscillation. Such "intrinsic" noise is believed to occur at various levels in all quartz resonators. While the mechanisms whereby this intrinsic phase noise is generated have yet to be identified and catalogued in their entirety, it is known that resonator Q (which is higher in the doubly rotated units) and frequency stability are inversely related in a statistical sense.

The phase noise of a signal can be measured only by a system which has equal or better noise performance. Relatively little has been published on the comparative noise performance of the AT cut vs doubly rotated resonators of similar fabrication, due in part to the fact that most crystal manufacturers are not equipped to measure the phase noise of quartz resonators. As a result, phase noise requirements appear on very few crystal drawings or specifications. However, the phase noise of crystal oscillators is intrinsically determined by the performance of the resonator. Therefore, phase noise measurements of the crystal oscillator circuits may be used to examine the phase noise performance of the crystals.

The close in phase noise of the crystal oscillator circuit is improved by the extremely high Q's developed in SC cut resonators. Also, the doubly rotated cuts may be operated, without damage or significant degradation, at substantially higher power than the AT cut, thereby directly facilitating a corresponding suppression of the white noise floor by approximately 10 dB/Hz.

Typically AT cuts will exhibit the tendency to "mode hop" or break up over the temperature vs frequency curve at drive levels in the area of 2 Mw. However, SC cuts designed for radar (XPD applications operate at 8 Mw, and have immensely added to radar sensitivity.

Generally speaking for SC cut resonators, phase noise is 3 to 10db better *than similarly prepared AT cuts. An example of a superior SC cut crystal* oscillator appears below.

PHASE NOISE MEASUREMENT

5MHZ, 3RD OVERTONE, HC-40/U HOLDER TYPE:

Hz FROM CARRIER	NOISE LEVEL (dBc/Hz)
5	132.5
10	136.5
20	141.5
100	147.5
1,000	153.5
10,000	159.5
25,000	160.5

Figure 1 shows a comparison of measurements using 3rd overtone AT cuts and a 5th overtone AT cut AT 100 MHz with an average SC cut 3rd overtone performance curve.

Figure 2 shows a phase noise comparison of several 3rd overtone SC cut crystals with measurements made in different oscillators at different times with crystals from different manufacturers. Greater than 10 dB/Hz difference occurs within the phase noise performance of the SC cut oscillators vs that of the AT cut oscillators.

Conclusions to be drawn would indicate a considerable difference in oscillator design, crystal design, or both.

AGING

Aging studies on AT and SC cuts (processed using similar manufacturing techniques) show that the SC typically ages into its final aging rate 5 to 10 times faster than the AT. The SC typically exhibits an improvement of 2 or 3 times in final aging rate. A 5.0 MHz, 3rd overtone SC cuts will typically reach 1×10^{-9}/day in less than 14 days.

A group of 10 MHz, 3rd overtone SC cuts, together with a group of similarly prepared 10 MHz, 3rd overtone AT cuts were subjected to repeated cold shock experiments. Soak times were approximately 10 hours of -30°C. The AT cuts showed frequency changes in parts in 10^{-7} and their subsequent aging rates were an order of magnitude poorer than prior to the cold soaks. The SC cuts however showed frequency shifts of parts in 10^{-9} and 10^{-8}, and the aging rate was not impaired.

SHORT TERM STABILITY

10 MHz/3rd Overtone/SC cut/HC-37/u Holder Type:
500 second stability 1×10^{-9}

10MHz/3rd Overtone/SC-cut/HC-40/u Holder Type:
1 second stability 5×10^{-9}
.1 second stability 5×10^{-9}

CONCLUSIONS

Piezo Crystal Company has been investigating the advantages of doubly rotated cuts for more than ten years, and successfully manufacturing these units for the past five years. The proprietary manufacturing and testing systems developed by Piezo Crystal Company have virtually eliminated the production problems once associated with the doubly rotated cut crystals. Over 8,000 doubly rotated resonators have been fabricated to date, exclusive of several thousand "blanks only" provided for customers' final processing.

The development of the doubly rotated cuts has allowed the frequency control industry to expand its previous limitations hundredfold. The acceptance of this "new" technology in the RF world has been overwhelming. We at Piezo Crystal Company are committed to continuing the research and advancement of this technology, and sharing our gained knowledge with the technical community.

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1. D.J. Healey III and S.Y. Kwan, "*SC-cut Quartz Crystal Units in Low-Noise Oscillator Applications at VHF*", Proc. 35th Annual Symposium on Frequency Control, 1981.
2. Raymond L. Filler, John A. Kosinski, and John R. Vig, "*The Effect of Blank Geometry on the Acceleration Sensitivity of AT and SC-cut Quartz Resonators*", Proc. 36th Annual Symposium on Frequency Control, 1982.
3. Raymond L. Filler, John A. Kosinski, and John R. Vig, "*Further Studies on the Acceleration Sensitivity of Quartz Resonators*", Proc. 37th Annual Symposium on Frequency Control, 1981.
4. Grant Moulton, "*Analysis and Prediction of Phase Noise in Resonators and Oscillators*", RF and Microwave Measurement Symposium and Exhibition, 1984.
5. Lynn C. Heidman, "*A Review of Progress Related to Doubly Rotated Quartz Crystals*", Sixth Quartz Devices Conference and Exhibition, August, 1984.

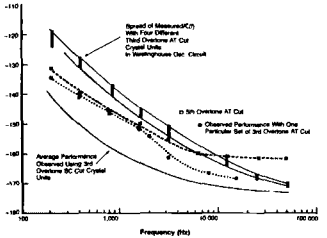

Spread of Measured ℒ(f) With Four Different Third Overtone AT Cut Crystal Units in Westinghouse Osc. Circuit
5th Overtone AT Cut
Observed Performance With One Particular Set of 3rd Overtone AT Cut
Average Performance Observed Using 3rd Overtone SC Cut Crystal Units
ℒ(f) dBc/Hz
Frequency (Hz)

Figure 1. Comparison of ℒ(f) Displayed by Oscillator Using SC Cut and AT Cut Units Approximately 100 MHz

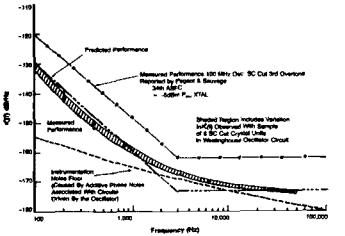

Predicted Performance
Measured Performance 100 MHz Osc. SC Cut 3rd Overtone Reported by Prosser & Sauvage 34th ASFC - Author's Xtal
Measured Performance
Shaded Region Includes Variation In ℒ(f) Observed With Samples of 6 SC Cut Crystal Units in Westinghouse Oscillator Circuit
Instrumentation Noise Floor (Created By Additive Phase Noise Associated With Circuits Driven By the Oscillator)
ℒ(f) dBc/Hz
Frequency (Hz)

Figure 2. ℒ(f) Characteristics of Third Overtone SC Cut Crystal-Controlled Oscillators at Approximately 100 MHz

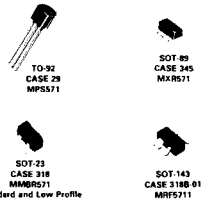
RF PLASTIC PACKAGE COMPARISON STUDY

KAMIL GRESKO

MOTOROLA INC.

SEMICONDUCTOR PRODUCTS SECTOR

DECEMBER 1985



Most manufacturers today are rapidly turning to use surface-mount components to utilize the full benefits of this relatively new technology. SMT's popularity has been accelerated by the development and availability of small outline semiconductor packages and device availability in these packages. Major manufacturers such as IBM, AT&T, GM and FORD are making significant investments in SMT.

The advantages and disadvantages between SMT and other technologies are already well known.

The objective of this article is to show the design engineers and other users some of the different aspects of SMT, make them aware of possible trade-offs and help them make the right decision.

Commonly cited advantages of SMT are:

- Space savings allowing smaller PC boards and total system size reduction
- Lower cost in high quantity
- Increased automation capability and wide choice of automated production equipment
- More reliable construction, better shock resistance and less sensitivity to vibrations
- Better high-frequency operation due to shorter lead lengths and *interconnections*

However, with decreased component and PC board size, an important factor which must be considered is thermal dissipation. Usually, the same die type is used in surface mounted devices as with conventional, "thru-hole" devices. The same bias conditions as used with the conventional devices will result in a higher die operating temperature for surface mount devices.

Consequently, miniaturization leads to thermal concentration.

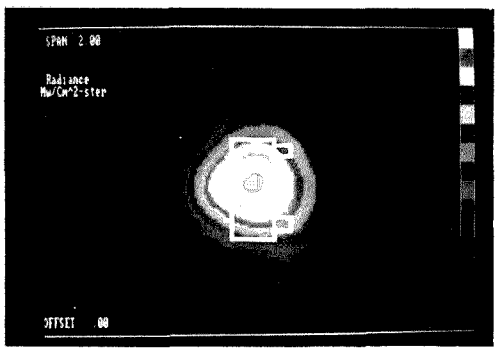


Fig. 1 Constant temperature zones surrounding SOT-23 transistor mounted on FR-5 PC board. Die temperature is 150°C.

The trade-off between the increase in component density and the concentration of thermal energy must be evaluated to avoid thermal collapse. Some of the most important information every design engineer needs to know is the thermal resistance of the package. The smaller the package is, the more important the die size consideration becomes. The following graphs, available in Motorola data sheets, describe thermal resistances for two different packages - SOT-23 and SOT-89.

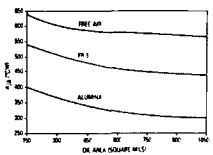


Fig. 2 Thermal resistance Θ_{JA}

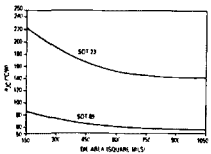


Fig. 3 Thermal Resistance Θ_{JC}

All these factors may have an influence on the choice of PCB material, number of layers, and the thickness of the BCB because Θ_{JA} is influenced by PCB material, thickness, etc.

The heat transfer from the die to the package, from the package to the PC board and then away from the board should be considered very cautiously in the design stage.

Things to be considered before starting are:

- Availability in a particular package.
- Package electrical-thermal consideration, to guarantee electrical and thermal requirements.

For example: If design of oscillator requires minimum f_T of 7.5Ghz the designer will probably refer to curve #18, which meets the requirement at collector current of 50mA. If V_{ce} is 10V the device will require power dissipation of 500 mW, obviously SOT-23 or SOT-143 are not suitable due to their power dissipation rating. The designer will have to chose between SOT-89 or TO-92 package.

Regardless of previous application devices like #12, 13, 14 curves will allow the designer to choose any package if electrical requirements are satisfied. Curve #11 shows that SOT-23 or SOT-143 is the most suitable package because a minimum power dissipation is required.

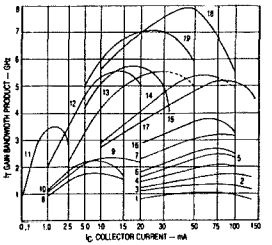


Fig. 4 Electrical parameter f_T versus collector current I_C

Other factors besides placement system and soldering methods are post assembly cleaning, visual inspection and test availability.

There are always a number of questions which must be answered in order to determine the optimal solution.

The purpose of this comparison is to find out the relative differences in performance that a particular transistor exhibits when encapsulated in the TO-92, SOT-23, SOT-89 and SOT-143 plastic packages. Package parasitic capacitances, lead frame construction and wire inductances are important factors in determining the ultimate application performance of the encapsulated transistor.

Fig. 5 TO-92 Internal Construction (Maximum die size 60 mil X 60 mil)

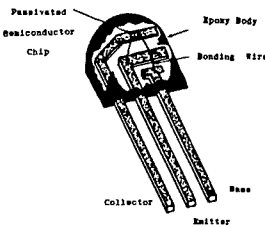


Fig. 6 SOT-89 Internal Construction (Maximum die size 60 mil X 60 mil)

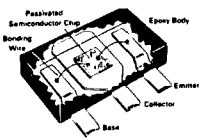


Fig. 7 SOT-23 Internal Construction (Maximum die size 30 mil X 30 mil)

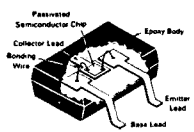
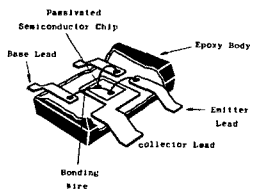


Fig. 8 SOT-143 Internal Construction (Maximum die size 30 mil X 30 mil)



An RF NPN bipolar chip which has relatively high gain and low noise characteristics at RF frequencies was chosen for this investigation. In silicon NPN transistors are usually preferred, since the electron mobility is higher than mobility of holes.

There were wafers selected from two different wafer lots and devices from each wafer were assembled in each of the four package. The intent was to obtain encapsulated transistors which were not only representative of the wafer line but which were similar enough that chip-to-chip variation was not a major question when the results were compared.

After DC testing, these four package groups of ten devices each were subsequently used for RF measurements.

RF transistors are represented by two-port networks and characterized by scattering, also known as S-parameters. S-parameters completely describe the behavior of two-port networks at RF and microwave frequencies. S-parameters are popular because they are easy to measure with modern Network Analyzers, their use in RF and microwave transistor amplifier design is conceptionally simple and they provide meaningful design information. All parameters mentioned in further consideration are measured in a 50 Ohm system, but a 75 Ohm system can be used as well. Of course, the values obtained using a 75 Ohm system measurement will not be identical to using a 50 Ohm system. It's up to the design engineer what measurement system serves his application.

Statistical processed data can be used for more advanced CAD design. On the other hand, it is very important to keep the parameters consistent over a long period of time, to guarantee the proper operation of circuit which design was based on that information. The reason to keep parameters consistent is the fact that the size of SMT PCB's is getting smaller and less space is left for relatively expensive and space consuming adjustment components.

Today's manufacturers, including Motorola, are implementing new process control methods to guarantee these parameters to full customer satisfaction.

The S-parameters for a transistor are reflection and transmission coefficients describing the input and the output in terms of power.

Transmission coefficients S_{12} and S_{21} are commonly called gains or attenuations. Reflection coefficients S_{11} and S_{22} relate to return loss, SWR and impedances.

The S_{12} parameter is the reverse transmission coefficient. Increasing magnitude of S_{12} with frequency indicates negative gain or loss due to package parasitics. In other words, S_{12} represents the output to input feedback of the transistor.

The S_{21} parameter is the forward transmission coefficient. As the frequency increases the magnitude of S_{21} decreases which indicates a decrease of insertion gain.

S_{11} parameter is the input reflection coefficient. As the magnitude of the reflection coefficient decreases the return loss and SWR improves. S_{11} indicates how well the input of a transistor matches to particular measurement system impedence. S_{11} measured in common emitter configuration is plotted in the reflection coefficient plane at specific bias conditions.

S_{22} is the output reflection coefficient. S_{22} is measured and plotted in the same manner as S_{11} except the input and the output are interchanged.

Many other parameters can be derived from S-parameters. Two figures of merit are commonly used by manufacturers to describe the transistor performance - Cut off frequency f_T and maximum frequency of oscillation f_{max}.

f_T - Cutoff frequency is the frequency where the short circuit gain $h_{fe}(\omega)$ approximates unity. The f_T is related to physical structure of a transistor by delay time τ_{ec}, which represents the sum of four delays encountered sequentially by the carriers as the flow from the emitter to the collector. Decreasing the base thickness will increase the f_T.

The other possibility to increase f_T is narrowing the collector region. However, there is always corresponding decrease in breakdown voltage by decreasing the collector width.

Therefore, every transistor is a result of compromise between high frequency operation and high breakdown voltage. The following formula is used to determine the frequency:

$$f_T = \frac{-2\,|S_{21}|}{(1-S_{11})(1+S_{22})(S_{12}S_{21})} f_m$$

S-parameters were obtained at measurement frequency f_m usually 100 MHz or 1 GHz.

f_{max} - maximum frequency of oscillation. It is a frequency where the maximum available power gain of the transistor G_{Amax} is equal to 1. G_{Amax} is the maximum power gain that can be realized without external feedback. G_{Amax} and f_{max} are measured by conjugately matching the source to the transistor input and the load to the transistor output impedance.

G_{Amax} - maximum available power gain. G_{Amax} is actually the ratio between power available from network and power available from source and is higher than the transducer gain $|S_{21}|^2$ because of the matching conditions and stability factors.

The following formula is used to determine G_{Amax} from S-parameters:

$$G_{Amax} = \frac{|S_{21}|}{|S_{12}|}(K + \sqrt{K^2 - 1})$$

A condition that a two-port network can be simultaneously matched with a positive real source and load is:

$K > 1$ or $C < 1$

C = Linvill factor

$$K = \frac{1 + |D|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}\,S_{21}|}$$

Where $D = S_{11}S_{22} - S_{12}S_{21}$

G_{Umax} - maximum unilateral power gain. G_{Umax} is based on the magnitude of S_{21} and the contributions of the conjugate matched networks to the input and output of the transistor.

$$G_{Umax} = \frac{|S_{21}|^2}{\left(1 - |S_{11}|^2\right)\left(1 - |S_{22}|^2\right)}$$

Where S_{11} 1 and S_{22} 1

or in logarithmic form,

$$G_{Umax} = 10\log \frac{1}{1 - |S_{11}|^2} + 10\log|S_{21}|^2 + 10\log \frac{1}{1 - |S_{22}|^2}$$

In all these unilateral assumptions, the S_{21} is set equal to zero, which makes the design procedure much simpler.

Three basic considerations are:

* Gain equal G_{Umax} regardless of noise figure
* Maximum possible gain at minimum N_F
* Design of an amplifier covering the frequency band with maximum gain and noise figure less than permissible by specification.

The meaning of f_T, f_S, and f_{max} is illustrated in the following figure. The gain rolls off at the rate of 6dB/octave.

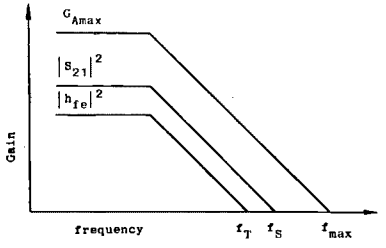


Figure 9 Frequency characteristics of G_{Amax}, $|S_{21}|^2$ and $|h_{fe}|^2$

Another parameter allowing qualitative comparison between Bipolar Junction Transistors (BJT) is the Noise Figure (NF). Expressed in dB, NF is a measure of the degradation in signal to noise ratio with passage of the signal through a given transistor.

Two sources of noise in a BJT are thermal noise and shot noise.

Thermal noise is caused by the vibration of the carriers in the ohmic resistance of the emitter, base and collector, due to their finite temperature. Some of the vibrations have spectral content within the frequency band and contribute noise to the signal.

Shot noise is a current dependent effect caused by the quantized and random nature of current flow. Current is not continuous but quantized being limited by the smallest unit of charge $q = 1.6 \times 10^{-19}$C. Particles of charge also flow with random spacing. Shot noise depends upon bias conditions.

From all that has been mentioned to this point, it is evident that right starting material and actual chip design are the most significant factors determing the transistor performance.

For better understanding of RF transistor characteristics it is necessary to use a model including all additional parasitic resistance, inductances and capacitances, which will depending on package, degrade the performance to a certain extent.

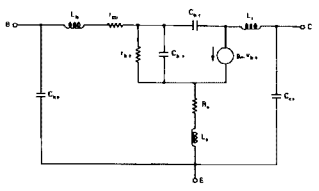


Fig. 10 A BJT common emitter model including parasitics

The resistance $r_{bb'}$ represents the base to emitter resistance. The $C_{b'e}$ capacitance is due to the junction from base to emitter. Emitter resistance R_e produces an inductive reactance across the base to emitter terminal, with increasing frequency, due to complex $h_{fe}(\omega)$. Since resistance associated with each region of transistor affect the various RC charging times, it is important to keep them to a minimum. Therefore, the metallization patterns contacting the emitter and base region must not present significant series resistance. There is always some contact resistance, but for simplicity will be left out of further consideration.

The package capacitance and wire inductance contributes most to coefficients variations at the higher frequencies. The meaning of the parasitic elements

L_b, L_e, L_c, C_{be} and C_{ce} is self-explanatory.

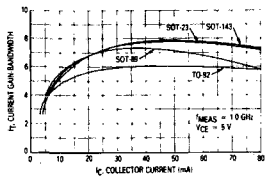
All of them are package dependent and will be determined by:

- size of a package
- material used
- lead frame construction
- lead frame material
- bonding method
- size of bonding wire

The transistor input and output capacitances are figures of merit that are commonly used and are easy to measure. Capacitance is a function of either emitter-base C_{iB}, collector-base C_{OB}, or collector-base with emitter AC wise shorted C_{CB} reverse voltages measured at 1 MHz.

All of these parameters and measurement results are compared and evaluated for all the packages in the following graphs and tables.

Current Gain-Bandwidth Product versus Collector Current



F_T VS. I_C

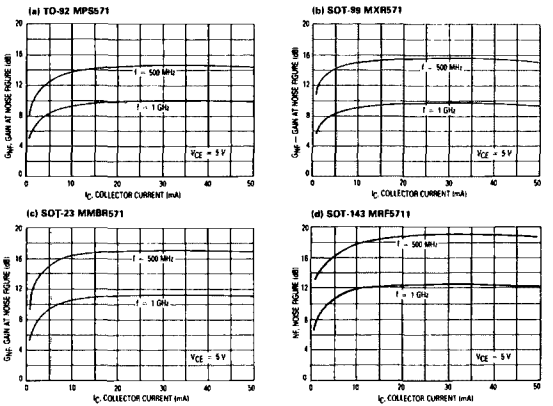
This graph shows the relationship between the current gain-bandwidth product and collector current (I_C) @ V_{CE} = 5.0V. The F_T values are calculated from S-parameters measured at 1.0 GHz.

The graph shows that the SOT-23 and SOT-143 packages have the highest F_T values of all the package types and are essentially equal over the entire range of I_C. The curves are basically flat from 30 to 60 mA and have a value of approx. 7.8 GHz @ 50mA. The slight "roll off" starts after I_C reaches approximately 60 mA.

The SOT-89 package shows an intermediate value of F_T with a value of approx. 7.2 GHz @ 50 mA. The curve "rolls off" or decreases in value with an increase in I_C from 30 to 80 mA. The "roll off" is generally caused by the decrease of effective base thickness at higher current levels.

The TO-92 package shows the lowest value of F_T as a function of I_C with F_T equal to 6 GHz at 50 mA. This is approximately 2 GHz down from the SOT-23 and SOT-143 and approx. 1 GHz down from the SOT-89. The curve is flat from 30 to 80 mA. No rolloff is seen with increasing I_C, possibly due to package power handling capability.

Gain at Noise Figure versus Collector Current



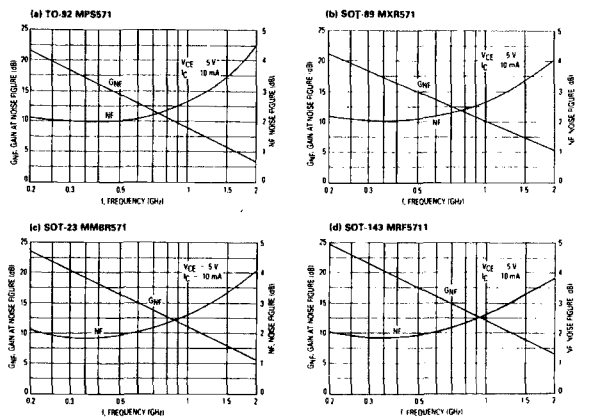
G_{NF} VS. I_C

These curves show the relationship between the gain obtained at minimum noise figure (G_{NF}) as a function of collector current (I_C) measured at the frequencies of 500 MHz and 1.0 GHz. In general, the curves show that the gain is flat for collector currents greater than 20 mA and that the gain at 500 MHz is obviously higher than the gain at 1.0 GHz for all packages.

Considering the family of curves at 500 MHz, the SOT-143 shows the highest gain with G_{NF} equal to 19 dB @ 30 mA. The SOT-23 is next in value with a G_{NF} of 17 dB @ 30 mA. The SOT-89 is next in value with a G_{NF} of 15.5 dB @ 30 mA followed closely by the TO-92 which is just under 15 dB @ 30 mA. There is a 4 dB difference between the lowest curves TO-92/SOT-89 and the highest SOT-143, with the intermediate curve SOT-23.

At 1.0 GHz, SOT-143 again shows the highest gain with a G_{NF} of approx. 12.5 dB @ 30 mA. SOT-23 is the next highest in value with a G_{NF} of approx. 11.5 dB @ 30 mA. Again, the TO-92 and SOT-89 have the lowest values of G_{NF} with TO-92 equal to approx. 10 dB and SOT-89 equal to approx. 9.5 dB @ 30 mA. It is significant to note that the family of curves at 1.0 GHz are more "compressed" than at 500 MHz; there is a spread of only 2 dB between the lowest and highest valued curves at 1.0 GHz compared to the 5 dB spread at 500 MHz.

Gain at Noise Figure and Noise Figure versus Frequency



G_{NF} VS. FREQUENCY AND N_F VERSUS FREQUENCY

Straight LINES in the graphs show the decrease in G_{NF} with frequency for all four packages with the collector current fixed at 10 mA.

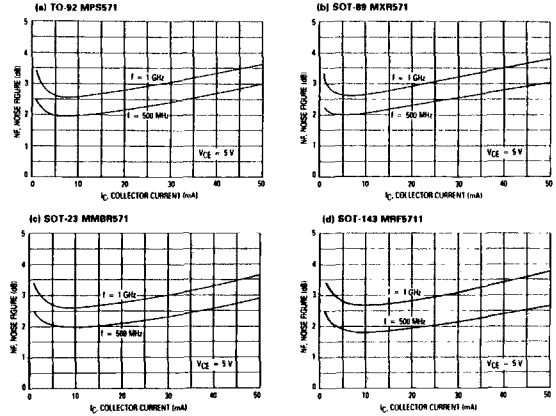
At this level of collector current, the SOT-143 shows the highest value of G_{NF} as a function of frequency although the SOT-23 is within approx. 1 dB of the SOT-143 over the range of frequencies measured to 1.5 GHz. The graph shows a value of approx. 12 dB for the SOT-143 and approx. 11 dB for the SOT-23 @ 1.0 GHz.

At frequencies less than 500 MHz, the TO-92 shows a slightly higher gain than the SOT-89. These packages reverse relative positions at frequencies greater than 500 MHz with the TO-92 having a slightly lower gain than the SOT-89. At 1.0 GHz, the SOT-89 shows a value of approx. 10 db while the TO-92 shows a value of approx. 9 dB. Over the entire range of measured frequencies, all the curves are within a 3 dB band.

CURVES in graphs show the variation of noise figure N_F with frequency for all four packages at a fixed value of collector current (10 mA). The curves show the expected result that N_F is basically flat for frequencies less than 500 MHz and increases steadily with frequency beyond 500 MHz.

All four package types are within a relatively narrow band of 0.2 dB or less over the measured range of frequencies. From all this it is evident that N_F is determined by wafer process, resistivity of starting material, and is most likely not package dependent.

Noise Figure versus Collector Current



N_F VS. I_C

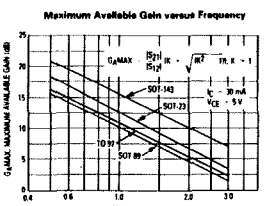
These graphs show the variation of noise figure with collector current for all four packages at the two fixed frequencies of 500 MHz and 1.0 GHz.

This family of curves shows the expected decrease in N_F with increasing I_C at relatively low current levels (less than 5 mA), a minimum in the region of 5 to 10 mA, and a steady increase in N_F with increasing I_C greater than 10 mA. The curves also show the expected result that the transistor N_F is higher at higher frequencies.

At both frequencies measured, the SOT-89 package appears to have a slightly higher N_F than the other packages. At a given frequency, the packages are within a maximum of 0.2 dB of each other.

At 500 MHz, the curves show a value of approx. 2 dB with I_C = 10 mA. For 50 mA, the curves show a value of approx. 3 dB for all four packages.

At 1.0 GHz, the curves show a value of approx. 2.6 dB with I_C = 10 mA. For 50 mA, the curves show a value of approx. 3.7 dB.



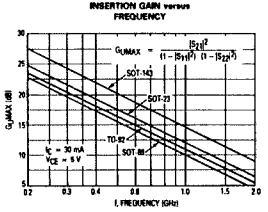
G_A MAX VS. FREQUENCY

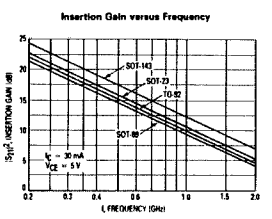
Maximum available gain G_AMAX is a gain which is calculated from S-parameters. The defining equation is shown on the graph. The curves show the expected decrease in G_AMAX with frequency.

The SOT-143 package shows the highest value of G_AMAX over frequency. The curve shows a value of approx. 21 dB @ 500 MHz.

The SOT-23 package shows the next highest G_AMAX and appears to have a slightly greater slope than the SOT-143. The curve shows a value of approx. 18 dB @ 500 MHz. Over the frequency range actually measured (500 MHz to 2.0 GHz), the SOT-23 is approximately 3 dB down from the SOT-143.

The TO-92 is the next curve down although it is very close to the SOT-89 curve. The curves are 0.8 dB apart. From the curves, the TO-92 has a G_AMAX of approx. 16.5 dB and the SOT-89 approx. 15.3 dB @ 500 MHz. The SOT-23 is approx. 2.5 dB higher than the TO-92 and SOT-89 @ 500 MHz, and approx. 1.5 dB higher than the TO-92 and SOT-89 at 2 GHz.





G_{Umax} VS. FREQUENCY

Maximum unilateral power gain G_{Umax} is slightly lower than maximum available gain G_{Amax}.

Formula defining G_{Umax} is simpler compared to G_{Amax} because it does not take stability factors into consideration. Compared to $|S_{21}|^2$ the unilateral gain is higher because input and output mismatches are taken into account deriving this number.

Again, the package performance curves are in the same order as G_{Amax}.

SOT-143 package shows the highest value of G_{Umax} over frequency, and value of approximately 20 dB at 500 MHz.

The next is SOT-23 with approximate value of 17.5 dB at 500 MHz followed by TO-92 16.5 dB and SOT-89 approximately 16 dB at 500 MHz. The curves are abut 4 dB apart.

$|S_{21}|^2$ VS. FREQUENCY

The insertion gain $|S_{21}|^2$ is a gain parameter calculated from the forward transmission coefficient S_{21} of the transistor. The quantity is less than G_AMAX since the gain (or decrease in loss) of the transistor achieved by input and output matching is not considered. The graph shows the decrease of insertion gain with increasing frequency.

All of the curves are approximately parallel which means that $|S_{21}|^2$ decreases at a constant rate with frequency for all four package types. The SOT-143 shows the highest value of $|S_{21}|^2$ followed by SOT-23, TO-92, and SOT-89 in decreasing order.

Considering the SOT-143 curve as a reference, the SOT-23 is approx. 2 dB down, the TO-92 is approx. 2.4 dB down, and the SOT-89 is approx. 2.8 dB down.

DYNAMIC PARAMETERS SUMMARY

Parameter	Conditions	Unit	Package			
			TO-92	SOT-89	SOT-23	SOT-143
f_T	50 mA 1.0 GHz	GHz	6.0	7.2	7.7	7.8
G_{NF}	10 mA 500 MHz	dB	13.6	14.9	16.4	17.8
	10 mA 1.0 GHz		9.4	9.3	10.6	12.0
	30 mA 500 MHz		14.6	15.4	17.0	19.1
	30 mA 1.0 GHz		9.9	9.5	11.3	12.1
N_F	10 mA 500 MHz	dB	2.0	2.1	2.0	1.8
	10 mA 1.0 GHz		2.6	2.7	2.6	2.7
	30 mA 500 MHz		2.4	2.6	2.4	2.3
	30 mA 1.0 GHz		3.0	3.2	3.0	3.1
G_AMAX	30 mA 500 MHz	dB	16.1	15.5	18.4	20.8
	30 mA 1.0 GHz		10.5	10.2	11.9	15.5
	30 mA 2.0 GHz		5.4	5.4	6.9	10.0
$\|S_{21}\|^2$	30 mA 500 MHz	dB	15.2	14.6	16.0	17.5
	30 mA 1.0 GHz		9.7	9.1	10.5	12.0
	30 mA 2.0 GHz		4.6	4.2	5.3	6.8
C_{cb}	1.0 V 1.0 MHz	pf	2.5	1.4	1.9	2.2
	2.0 V 1.0 MHz		2.0	1.2	1.4	1.6
C_{ecb}	5.0 V 1.0 MHz	pf	0.8	0.8	0.9	0.7
	10.0 V 1.0 MHz		0.7	0.8	0.8	0.5

The next series of graphs are S-parameter plots for each of the four packages.

The scattering parameters are plotted as functions of frequency for a collector current value of 30 mA and a collector-emitter voltage of 5V. S-parameters for every package are listed in table form below the SMITH CHART and Polar Plot.

In the discussion that follows, each of the four S-parameters (S_{11}, S_{22}, S_{21}, S_{12}) will be considered separately.

S_{11}

This parameter is the input reflection coefficient of the transistor. This parameter, along with S_{22} which is the output reflection coefficient, can be plotted in the reflection coefficient plane as complex impedances known as a SMITH CHART.

An examination of the SMITH CHARTS for all the packages shows that SOT-89 and TO-92 have similar resistance components with a magnitude of 26 to 32 Ohms over the frequency range of 0.2 to 2 GHz. Both devices have capacitive reactance approximately equal in value for frequencies under 500 MHz. At 500 MHz and up, the reactance becomes inductive with the TO-92 increasing at a faster rate than SOT-89. At 2.0 GHz, the TO-92 has a inductive reactance of 46 Ohms while the SOT-89 has a reactance of 31 Ohms.

The SOT-23 has a resistance of 21 to 22 Ohms from 200 MHz to 2.0 GHz. The SOT-23 has a capacitive reactance of 12.5 Ohms @ 200 MHz which decreases in magnitude with frequency becoming zero at just over 500 MHz. At higher frequencies, the inductive reactance of the input impedance increases to a value of 17 Ohms @ 2.0 GHz.

The SOT-143 has the lowest value for the resistance of all the packages ranging in magnitude from 11.5 to 13.5 Ohms from 200 MHz to 2.0 GHz. The capacitive reactance with a value of 12 Ohms at 200 MHz decreases in magnitude to zero at just over 500 MHz. As the frequency increases the inductive reactance increases to a value of 18 Ohms @ 2.0 GHz.

The differences in resistive portions of input impedance are very possibly due to bonding wire length (TO-92 vs. SOT-23). Since SOT-143 uses two bonding wires for the emitter leads the resistive portion is even lower than the SOT-23.

S_{22}

As mentioned previously, S_{22} is the output reflection coefficient which can be mapped on to the SMITH CHART as a complex impedance.

The TO-92 has a resistance which decreases in value from 55 to 40 Ohms from 200 MHz to 2.0 GHz. The reactance is capacitive at 200 MHz with a value of 28.5 Ohms and decreases in magnitude reaching zero at just over 1.0 GHz. The reactance increases in inductance with frequency to a value of 22 Ohms @ 2.0 GHz. The TO-92 is the only package of all the package types which shows a positive (inductive) reactance; all other packages remain capacitive to 2.0 GHz.

The SOT-89 has a constant resistance component of approximately 50 Ohms from 200 MHz to 500 MHz. Above 500 MHz, the resistance abruptly decreases in value with frequency reaching a value of 36.5 Ohms @ 2.0 GHz. The capacitive reactance is 23 Ohms at 200 MHz and decreases in magnitude to 5.5 Ohms @ 2.0 GHz.

The output impedance of the SOT-23 has a resistance component which decreases in value from 45 Ohms @ 200 MHz to 41 Ohms @ 2.0 GHz. The reactance remains capacitive over the entire frequency range which changes in value from 25 Ohms @ 100 MHz to 3 Ohms @ 2.0 GHz.

The SOT-143 has the lowest resistance of all four package types decreasing in value from 36 Ohms @ 200 MHz to 31.5 Ohms @ 2.0 GHz. The reactance component remains capacitive over the frequency range which change sin value from 27.5 Ohms @ 100 MHz to 6 Ohms @ 2.0 GHz.

S_{21}

The S_{21} parameter is the forward transmission coefficient of the transistor. The magnitude of S_{21} as mentioned before decreases with frequency at the rate of 6 dB per octave.

The SOT-143 package has the highest value for the magnitude of S_{21} over the entire frequency range. The SOT-23 is next in value followed by the TO-92 with the SOT-89 having the lowest value. All the package types show the largest decrease in value from 200 MHz to 500 MHz.

At 1500 MHz, all of the packages have a magnitude for S_{21} between 2 and 3. The SOT-143 has highest value of 2.74 while the SOT-89 has the lowest value of 2.02. The SOT-23 has a value of 2.29 and the TO-92 a value of 2.11.

At 2.0 GHz, the SOT-143 is the only package with a magnitude for S_{21} greater than 2 (2.20). SOT-23 shows a value of 1.84, followed by TO-92 with a value of 1.70. The SOT-89 is the lowest with a value of 1.62.

The phase of S_{21} decreases for all packages with TO-92 showing the greatest overall change. It changes from 99° @ 200 MHz to 11° @ 2.0 GHz. The TO-92 phase angle is close in value to the SOT-89 for frequencies up to 500 MHz. Above 500 MHz, the phase angle for the TO-92 decreases faster than the SOT-89. Over the entire frequency range, the phase angles for the SOT-23 and the SOT-143 packages stay close together in value.

S_{12}

The S_{12} parameter is the reverse transmission coefficient. Roughly speaking, S_{12} represents the output to input feedback of the transistor. It is desirable to keep this low value at minimum.

At 200 MHz, all packages show a similarity in magnitude for S_{12}. The SOT-143 is the lowest with a value of 0.03 followed by SOT-23 which will have a value of 0.04. Both the TO-92 and SOT-89 have a magnitude of 0.05.

As the frequency increases to 500 MHz, the magnitudes all increase and begin to diverge in value. Both TO-92 and SOT-89 increase to 0.11, while the SOT-23 increases to 0.09. The SOT-143 remains the lowest in value with a magnitude of 0.05.

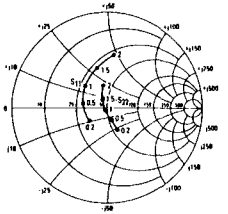
Above 500 MHz, the SOT-143 shows the smallest increase in magnitude going 0.09 @ 1.0 GHz to 0.16 @ 2.0 GHz. The SOT-23 shows the next smallest increase in magnitude going from 0.16 @ 1.0 GHz to 0.30 @ 2.0 GHz. The TO-92 and SOT-89 show the largest increase in magnitude of S_{21} from 1.0 to 2.0 GHz. They also remain very close in value. Both packages go from 0.21 or 0.22 @ 1.0 GHz to 0.36 or 0.38 @ 2.0 GHz, with the SOT-89 having the slightly larger magnitude.

Considering the phase of S_{21}, both SOT-23 and SOT-143 show the pattern of going from an initial low value @ 200 MHz, increasing @ 1.0 GHz, and reaching a lower than the initial value @ 2.0 GHz. The phase of S_{21} goes from 54° @ 200 MHz to 62° @ 1.0 GHz to 52° @ 2.0 GHz, for the SOT-143. For the SOT-23, the phase goes from 68° @ 200 MHz to 70° @ 1.0 GHz to 60° @ 2.0 GHz.

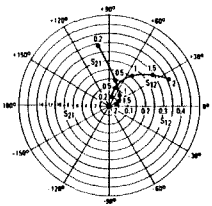
The TO-92 and SOT-89 show a different pattern. Both packages show a steady decrease in value for the phase of S_{21} as frequency increases with the TO-92 showing the largest decrease of the two. For the SOT-89, the phase of S_{21} goes from 74° @ 200 MHz to 66° @ 1.0 GHz to 49° @ 2.0 GHz. For the TO-92, the sequence is 75° @ 200 MHz to 55° @ 1.0 GHz to 23° @ 2.0 GHz.

TO-92 MPS571

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA

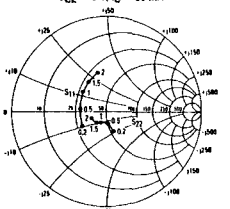


COMMON EMITTER S-PARAMETERS

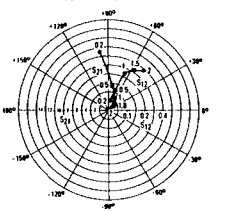
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\lvert S_{11}\rvert$	$\angle\phi$	$\lvert S_{21}\rvert$	$\angle\phi$	$\lvert S_{12}\rvert$	$\angle\phi$	$\lvert S_{22}\rvert$	$\angle\phi$
5	5	200	0.62	- 80	6.22	122	0.07	56	0.63	- 44
		500	0.40	- 148	4.52	87	0.11	50	0.36	- 58
		1000	0.39	155	2.51	54	0.16	48	0.23	- 78
		1500	0.48	122	1.86	32	0.23	42	0.15	- 114
		2000	0.59	100	1.50	14	0.31	33	0.14	173
	15	200	0.33	- 121	12.88	105	0.05	67	0.37	59
		500	0.28	175	5.62	79	0.10	65	0.18	- 67
		1000	0.32	143	2.99	53	0.19	55	0.08	- 94
		1500	0.40	117	2.14	32	0.27	42	0.07	171
		2000	0.55	95	1.74	17	0.35	30	0.198	117
	30	200	0.23	- 143	13.85	99	0.05	75	0.26	- 62
		500	0.23	169	5.75	76	0.11	70	0.13	- 68
		1000	0.30	130	3.05	50	0.21	55	0.04	- 136
		1500	0.41	106	2.11	28	0.28	38	0.12	130
		2000	0.56	85	1.70	11	0.36	23	0.26	102
	50	200	0.21	- 158	13.96	96	0.05	79	0.21	- 61
		500	0.23	162	5.82	75	0.11	72	0.11	- 86
		1000	0.30	128	3.09	49	0.21	56	0.03	- 149
		1500	0.41	105	2.11	28	0.29	39	0.12	127
		2000	0.56	84	1.70	11	0.36	23	0.27	100

SOT-89 MXR571

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA

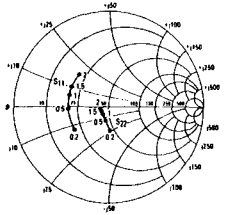


COMMON EMITTER S-PARAMETERS

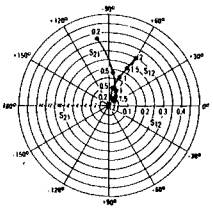
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\lvert S_{11}\rvert$	$\angle\phi$	$\lvert S_{21}\rvert$	$\angle\phi$	$\lvert S_{12}\rvert$	$\angle\phi$	$\lvert S_{22}\rvert$	$\angle\phi$
5	5	200	0.60	- 84	7.84	120	0.08	56	0.58	45
		500	0.38	- 152	4.17	86	0.11	54	0.34	56
		1000	0.39	161	2.32	62	0.19	58	0.27	- 71
		1500	0.44	132	1.64	45	0.26	55	0.25	- 90
		2000	0.49	106	1.33	31	0.32	52	0.26	- 106
	15	200	0.33	126	11.89	101	0.06	67	0.32	- 63
		500	0.29	178	5.13	81	0.11	69	0.18	73
		1000	0.33	148	2.75	62	0.22	65	0.15	- 99
		1500	0.37	123	1.93	47	0.30	66	0.16	118
		2000	0.42	100	1.55	34	0.37	49	0.17	- 139
	30	200	0.26	- 149	12.74	97	0.05	74	0.23	69
		500	0.27	174	5.37	78	0.11	73	0.13	82
		1000	0.32	144	2.85	62	0.22	66	0.13	- 112
		1500	0.36	120	2.02	47	0.31	67	0.15	132
		2000	0.40	98	1.62	35	0.38	49	0.17	- 152
	50	200	0.26	162	13.03	94	0.05	77	0.18	- 71
		500	0.27	169	5.43	78	0.12	75	0.11	85
		1000	0.32	142	2.88	62	0.22	67	0.12	- 117
		1500	0.36	119	2.02	47	0.31	67	0.15	- 137
		2000	0.40	97	1.60	35	0.38	49	0.17	- 155

SOT-23 MMBR571

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA

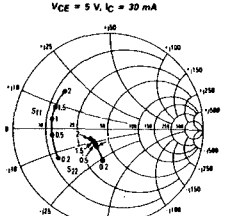


COMMON EMITTER S-PARAMETERS

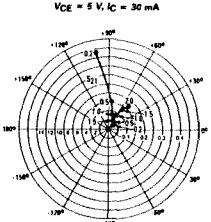
V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\lvert S_{11}\rvert$	$\angle\phi$	$\lvert S_{21}\rvert$	$\angle\phi$	$\lvert S_{12}\rvert$	$\angle\phi$	$\lvert S_{22}\rvert$	$\angle\phi$
5	5	200	0.68	82	8.41	126	0.07	53	0.61	−45
		500	0.52	142	4.62	93	0.10	46	0.35	−80
		1000	0.50	179	2.57	72	0.14	53	0.26	−71
		1500	0.51	161	1.82	57	0.19	58	0.24	−77
		2000	0.52	143	1.48	45	0.24	59	0.22	−86
	15	200	0.46	−125	13.65	108	0.05	60	0.35	−73
		500	0.43	−169	6.03	66	0.09	66	0.17	−94
		1000	0.44	168	3.20	72	0.16	67	0.14	−111
		1500	0.45	152	2.21	58	0.22	64	0.11	−118
		2000	0.46	137	1.80	48	0.29	59	0.10	−131
	30	200	0.42	−148	14.79	102	0.04	68	0.26	−87
		500	0.41	177	6.31	64	0.09	72	0.14	−115
		1000	0.42	165	3.35	71	0.16	70	0.12	−135
		1500	0.44	151	2.28	59	0.23	65	0.11	−144
		2000	0.44	135	1.84	48	0.30	60	0.10	−157
	50	200	0.41	−159	15.14	98	0.04	73	0.21	−96
		500	0.42	179	6.38	63	0.09	75	0.13	−124
		1000	0.43	163	3.35	70	0.16	71	0.12	−143
		1500	0.44	148	2.32	58	0.23	66	0.10	−151
		2000	0.45	134	1.84	48	0.30	60	0.09	−163

SOT-143 MRF 5711

INPUT/OUTPUT REFLECTION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA

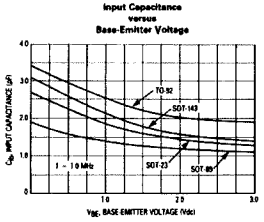


FORWARD/REVERSE TRANSMISSION COEFFICIENTS versus FREQUENCY
V_{CE} = 5 V, I_C = 30 mA



COMMON EMITTER S-PARAMETERS

V_{CE} (Volts)	I_C (mA)	f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
			$\lvert S_{11}\rvert$	$\angle\phi$	$\lvert S_{21}\rvert$	$\angle\phi$	$\lvert S_{12}\rvert$	$\angle\phi$	$\lvert S_{22}\rvert$	$\angle\phi$
5	30	200	0.60	−150	17.22	106	0.03	54	0.34	−87
		500	0.62	−177	7.52	85	0.06	60	0.24	−130
		1000	0.62	167	4	72	0.09	62	0.22	−144
		1500	0.64	154	2.74	59	0.13	56	0.24	−148
		2000	0.63	138	2.2	46	0.16	52	0.24	−157



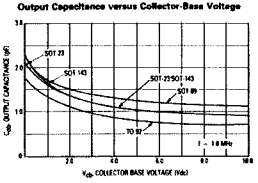
Cib VS. V_{BE}

These curves show the inverse relation of input capacitance Cib with emitter-base voltage V_{BE}.

TO-92 has the highest input capacitance while SOT-89 has the lowest due to the position of E-B lead frame surfaces which are not facing each other directly as the TO-92. The SOT-143 and the SOT-23 are intermediate in value with the SOT-143 having a greater value of Cib than SOT-23 at any given voltage. The lead frame surfaces are still facing each other, but there is less "common plates" area compared to TO-92, due to lead frame thickness.

At 0.5, the TO-92 is approx. 3 pf, the SOT-143 is approx. 2.6 pf, the SOT-23 is approx. 2.3 pf, and the SOT-89 is approx. 1.6 pf for Cib.

Of all the curves, SOT-89 has the smallest slope changing only 0.5 pf from 0.5V to 3.0V. The SOT-143 shows the greatest change in value of 1.2 pf from 0.5 to 3.0V. Both the TO-92 and SOT-23 show an approximate change of 1.0 pf from 0.5 to 3.0V.



Cob VS. Vcb

This graph shows the inverse relation of output capacitance (Cob) with collector-base voltage Vcb.

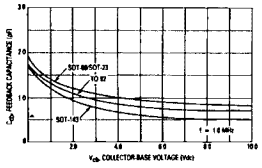
The graph shows that the SOT-89 has the highest value of Cob and TO-92 has the lowest at a given value of Vcb. The SOT-23 and SOT-143 show intermediate and essentially identical values of Cob.

At 2V, the curves show the following values: for SOT-89, approx. 1.5 pf, for SOT-23 and SOT-143, approx. 1.4 pf, for TO-92, approx. 1.1 pf.

Considering the slopes of the curves, the TO-92 shows the least change in value of 0.3 pf from 2V to 8V. Both the SOT-23 and the SOT-143 show the greatest change in value of 0.45 pf from 2V to 8V. The SOT-89 shows an intermediate decrease of 0.35 pf.

All the curves are within a 0.5 pf band.

Feedback Capacitance versus Collector-Base Voltage



Ccb VS. Vcb

This graph shows the inverse relation of feedback capacitance Ccb with collector-base voltage Vcb with emitter AC grounded using .1 pf capacitor.

The SOT-89 and SOT-23 curves are identical and show the highest value of Ccb of all the packages at any given value of Vcb. The SOT-143 has the lowest valued Ccb curve while the TO-92 curve is intermediate in value.

The SOT-143 shows the greatest change in value of Ccb of 0.45 pf from 2 to 8V. The SOT-23 and SOT-89 packages show the least change of 0.35 pf. The TO-92 shows an intermediate change of 0.4 pf from 2V to 8V.

All of the curves are within a 0.4 pf band.

All of these parameters Cib, Cob, Ccb and slope differences are lead frame construction dependent. Refer to figures 5, 6, 7 and 8.

CONCLUSION

The most significant difference between the four package types is the gain performance. Both as a function of frequency and collector current, the SOT-143 shows the highest gain. The SOT-23 is next in gain performance. The SOT-89 and TO-92 packages show similar but lower gain performance than the SOT-23.

Generally, RF performance is package dependent and is determined by parameters mentioned before such as size of package, lead frame construction, etc.

There are no significant differences in noise figure performance between the package types investigated. The variations measured between the different package types are small and lie within the range of variation that can be reasonably attributed to measurement error.

The input and output capacitances Cib, Cob and Ccb will vary from package to package. These variations are primarily due to internal construction of the device. These parameters are easily measured making them useful for outgoing and incoming inspections.

On the other hand S-parameters require a relatively complicated test setup and special fixturing. The S-parameters give the most comprehensive information of package differences most useful for designers. The results of these measurements can be used to calculate many other useful design parameters.

In spite of the variations in gain noted, all four packages show good RF performance. Other factors, aside from RF performance alone, such as power dissipation, cost, and board layout among others are undoubtedly relevant considerations when faced with the problem of determining which package type is best for a particular application.

ACKNOWLEDGEMENTS

I would like to thank Matt Zamora for the invaluable support he has given me by providing the vast number of measurements upon which this investigation was based. I would also like to extend my sincere appreciation to Lance Ulik and Jim Fogie for their advice and technical expertise in helping to complete this paper.

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RELIABLE OBSTRUCTED PATH COVERAGE DETERMINATION

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ABSTRACT

When the VHF or UHF terminals of a proposed circuit are so widely separated that the line-of-sight communication is not possible, the presence of a sharp, ridgelike obstruction between the terminals may improve the signal to the point where reliable communication is achieved. The strength of the received signal results from diffraction over the sharp obstacle, and varies with the signal frequency, the elevation of the circuit terminals, the location and elevation of the obstacle, and the shape of the obstacle peak. In many instances, the strength of the diffracted field exceeds the strength of a normal path field and has the added advantage of being essentially free from fading.

This paper will assist in showing how to determine the best obstructed path coverage when this is a viable alternate means to free path communication.

GENERAL COMMENTS

In the conventional use of VHF radio relay equipment, circuits have been considered satisfactory only when the path was unobstructed and stations were close enough, or sufficiently elevated, to be within radio line of sight. Under these conditions, both range and reliability were thought to be at a maximum. However, experience indicates that satisfactory communication usually can take place over a range appreciably greater than the radio line of sight, and that both range and reliability may actually be extended by the existence of an elevated obstacle in the radio path, similliar to passive repeaters used in microwave communications.

In situations where a terrain feature, such as a sharp mountain ridge of sufficient elevation, lies between the transmitter and the receiver, improved signal levels--relatively free from fades--have been observed. This phenomenon is referred to as the knife-edge effect. Circuits near or beyond the radio line of sight can be categorized as follows:

(1) The normal circuit; this may cover all types of intervening terrain, except no single terrain feature predominates. (Figure 1A)

(2) The obstructed circuit; one predominant terrain feature appears as the obstacle in the radio path. (Figure 1B)

Techniques of predictions and computation have been developed for used on obstructed radio paths for distance up to approximately 300 miles. Many obvious advantages accrue from this extension of the normal 25 to 30 mile range--

(1) No intermediate relay points are necessary; thus requirements for equipment and operating personnel are reduced.

(2) Installation and supply problems are alleviated because relatively inaccessible mountaintop locations need not be used.

(3) High circuit reliablity can be relaized, since properly engineered obstacle gain paths show a much lower fade rate than comparable line of sight paths.

(4) Operational dependability is increased, because fewer pieces of equipment are required.

(5) Large numbers of completely independent circuits can be established over the same path.

(6) Fewer frequencies are required for operation over long distances.

(7) Decreased chance of interference results, because of the directional characteristics of propagational path.

PLANNING OBSTRUCTED PATHS

The planning of an obstacle gain path necessarily entails detailed study of all intervening terrain. The planning and engineering of these paths is accomplished as follows:

1. Locate the desired terminal areas on suitable topographic charts (Use Geographic Quads 1X2 to start for long paths and 30, 15 or 7.5 min. for short paths).

2. Draw a line between the two most desirable points selected for the transmitter and receiver locations.

3. Locate the highest point (mountain peak or ridge line) in the intervening terrain. This high point should be as close as possible to the line drawn in 2 above.

4. Draw path profiles along the lines that connect the high point selected and each of the two desired terminals. If the profile shows multiple obstacles, repeat steps 2 and 3 above until, by slight shifts in the position of the terminals or by using other high points, only one obstacle intervenes between terminals. Then locate the tentative terminal sites.

5. Determine the expected transmission loss of the path (Figure 2).

6. From a tabulation of equipment characteristics, select an equipment combination that satisfies the service requirements as well as the propagational requirements given in 5 above.

7. Make a radio signal strength survey in one terminal area.

8. Choose a maximum signal location close to the proposed terminal site and experiment with different antenna heights to obtain the best signal strength.

9. Install station equipment at the desired site.

10. Repeat 8 and 9 above for other terminal.

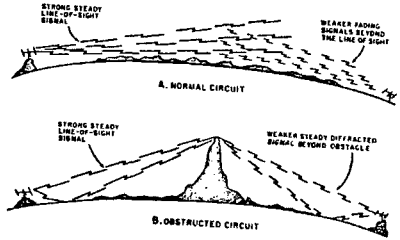
STRONG STEADY LINE-OF-SIGHT SIGNAL
WEAKER FADING SIGNALS BEYOND THE LINE OF SIGHT
A. NORMAL CIRCUIT
STRONG STEADY LINE-OF-SIGHT SIGNAL
WEAKER STEADY DIFFRACTED SIGNAL BEYOND OBSTACLE
B. OBSTRUCTED CIRCUIT

FIG 1. NORMAL & OBSTRUCTED PATHS

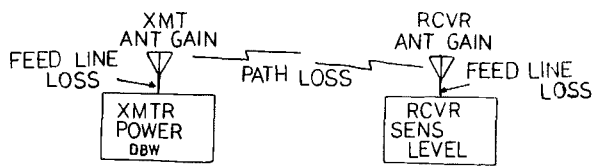

FIG 2 PATH COMPONENTS

PRELIMINARY PATH STUDIES

On a topographic map, identify the areas between which communication is desired. This map should have an altitude contour interval of no more than 100 feet. In selecting the terminal areas, consider the accessibility of the site to roads, power sources, and telephone circuits.

Determine whether a mountain peak or ridge exists between the two tentative terminal locations and whether or not it is of higher altitude than the surrounding terrain in the direction of the terminal areas. Several alternate terminal locations should be selected in the two terminal areas, such as sites A through F in Figure 3. If no such ridge or peak exists between any of the tentative sites, it may be necessary to install a relay station, and obstructed path cannot be used effectively.

Draw a line between the two tentative site locations that appear to be the most desirable. For example, if sites B and E were both terminal or relay stations in existing communications networks then they would be the most desirable due to the availability of existing services and roadways. Draw lines from each terminal location through the peak or ridge which brings the line as near as possible to terminal sites tentatively selected at the other end of the circuit. In Figure 3, for example, a line from C to F or from A to D would not cross the ridge at its sharpest point, while lines from C to D and from A to F do cross the sharp ridge crest. Lines A to F, B to E, and C to D are appropriate tentative paths for this circuit.

PROFILE PREPARATION

After selecting the path that apparently fulfills the requirements, profile drawings should be made to check the path for obstructions between each terminal and the major obstacle. To allow for the normal refraction of radio waves by the atomsphere, these profiles should be drawn on a 4/3 earth graphic scale.

Figure 4 is a graphic scale for 4/3 earth radius. This scale can be used with overlay paper on paths extending up to

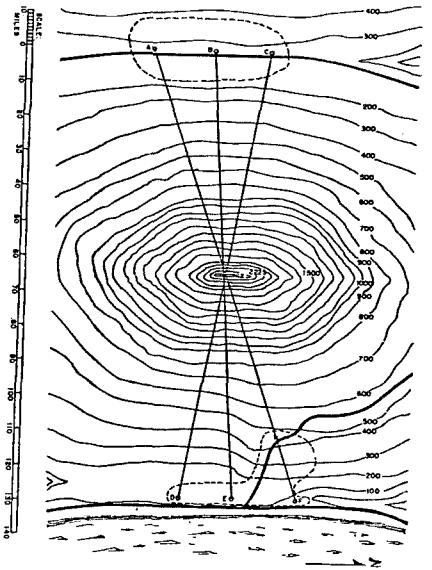

FIG.3 CONTOUR MAP PROBLEM

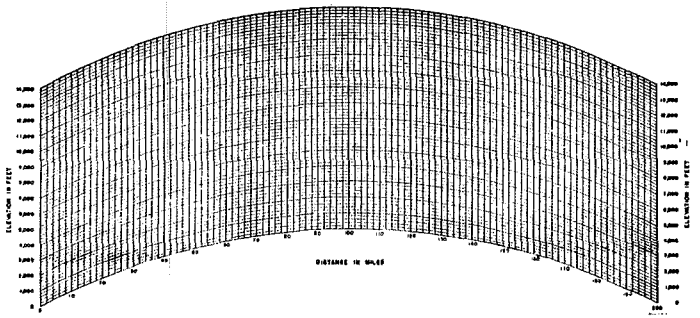

FIG 4 GRAPHIC SCALE 200MI 4/3 EARTH

200 miles. Paths over 200 miles can be profiled in the same manner as tropospheric scatter paths.

Plot the profile for path B to E, Figure 3. This profile is shown in Figure 5. From this profile drawing, it is determined that the path from terminal site B to the obstacle is clear, but that the path from terminal site E to the obstacle is shielded by a slight rise some 10 miles to the west of terminal E, and that the antenna would have to be elevated approximately 200 feet to use this terminal location. To move the terminal away from the highway, the 10 miles necessary for installation on the intervening rise would make the terminal site too inaccessible. Other paths should be investigated.

Plot the profile for path A to F (Figure 6). From this profile, it is determined that the path from A to the obstacle is clear, but that the path from terminal site F to the obstacle again is shielded by a continuation of the same rise that shielded terminal E. However, in this case, the rise is near the northwest branch of the highway, and the terminal can be located at point X along the straight line propagational path.

If no possible terminal locations were acceptable along the straight line path across the obstacle, then terminals slightly to one side or the other could be selected; however, the closer they are to the straight line path, the better the results will be. In the example, tentative eltee should be selected at points A and X (Figures 3 and 6).

In selecting terminal site locations for single obstacle paths, the terminal sites should not be located too close to the obstacle (Figure 7A). Even though the profile shows only one obstacle, gently rounded obstacles (Figure 7B) attenuate the signal more than do sharply defined obstacles. Multiple obstacle paths should be avoid if at all possible since their attenuation is much greater and their path prediction is extremely critical. In Figure 7C, thepath T to Q might possibly work, since the second obstacle is near grazing. But if the obstacle were only slightly higher, or the point Q were slightly lower, the path might not be usable. Where a choice of equally sharp obstacles of different heights is available, the lower obstacle usually produces less attenuation, and is to be preferred.

The shape of the obstacle at right angles to the transmission path is unimportant, except that mountain peak

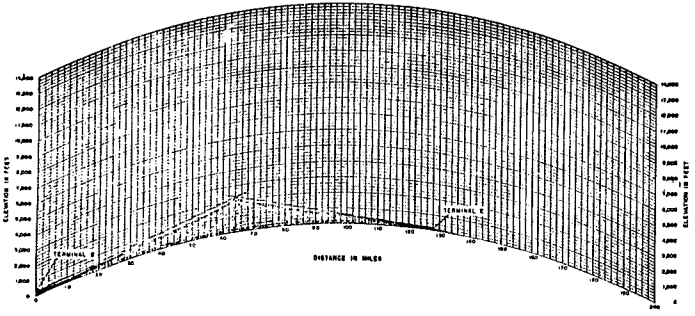

FIG. 5. PROFILE OF PATH B-E, FIG. 3

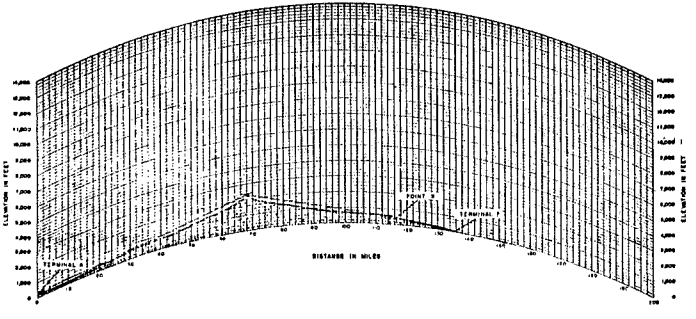

FIG 6 PROFILE PATH A-F, FIG 3

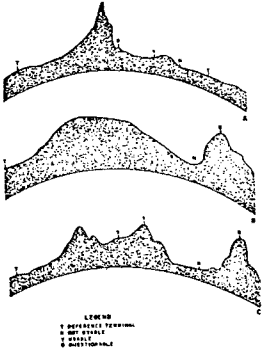

FIG 7 PROFILES

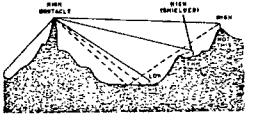

FIG 8 SITING POSITIONS

obstacles produce a more direct effect in the terminal area than do ridge obstacles. This effect is caused by the peak offering only one obstacle path, directly over the crest which is the sharpest point of the obstacle. However, a ridge may retain its curvature at the crest for a considerable distance, thus, the portion that produces the diffraction process is not critical as to position.

The obstacle height is the height of the obstacle above the average altitude of the two terminal sites. For example, if one terminal site is situated at an altitude of 300 feet above sea level and other terminal site is at 500 feet above sea level, the average altitute of the terminals is 400 feet. If the obstacle height is 2,500 feet above sea level then the actual effective obstacle height is 2,100 feet (2,500-400=2,100 feet).

Antenna tower heights must be such that the terminal to obstacle path has adequate clearance above the average terrain and the antenna must be above any heavy foreground foliage (any obstruction within the first Freenel Zone). The following points should be considered when selecting terminal sites:

1. Neither terminal should be located closer to the obstacle than approximately two miles per 1,000 feet of obstacle height.

2. If possible, avoid terminal to obstacle paths that are over water.

3. Locate terminals at low points, unless a high elevation can be found that is shielded from any reflected paths (Figure 8). The midpath height should not be excessive.

4. Avoid any foreground obstacles, such as trees, buildings, steel towers, and guy wires.

Antenna heights must be adjusted to provide free-space clearance between each terminal and the obstacle. This clearance is determined by considering the top of the main obstacle to be a broadband relay station. Then the path from each terminal to this relay station (obstacle peak is considered in turn as a line of sight path in accordance with the criteria for determining free-space path clearance.

EXPECTED TRANSMISSION LOSS

After determining the obstacle height and path distance from the profile and contour maps, a perfromance estimate can be made for the proposed path.

The operating frequency, obstacle height, and path length must be known to compute the estimated path loss. The nomogram in Figure 9 can be used to make this estimate.

The nomogram (Figure 9) is used in the following manner:

1. Draw a line connecting the operating frequency on scale F with the path distance on scale D.

2. Connect the point where this line crosses the unscaled line X with the obstacle height on scale H.

3. Read the estimated path loss at the point where this second line intersects scale L.

This estimated path loss then is compared with the maximum acceptable path loss of the proposed equipement.

EQUIPMENT SELECTION

Equipment requirements for obstacle gain paths are determined by computing the maximum allowable path loss of the particular type of equipment and comparing this result with the expected path loss. If the maximum allowable path loss for the equipment is larger than the expected path loss, the system is good and an operable circuit should result.

The first step in computing the equipment capability is to findtherequired receiver input. The following formula is used to determine this factor:

IR=ND+NF+FM+TQ

IR= THE REQUIRED RECEIVER INPUT IN DB BELOW FREE SPACE;

ND= THE EFFECTIVE NOISE INPUT DUE TO THE RECEIVER ACCEPTANCE BANDWITH IN DB;

NF= THE RECEIVER NOISE FIGURE IN DB; AND

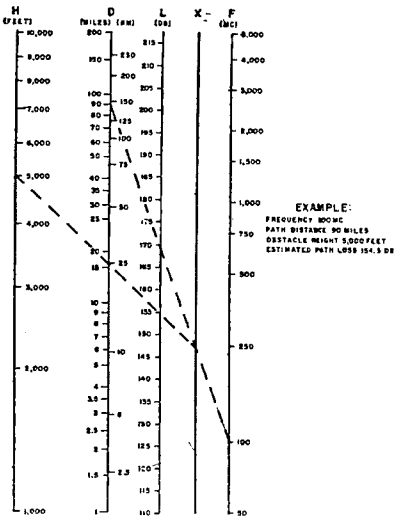

FIG.9 ESTIMATED PATH LOSS NOMOGRAPH OBSTACLE GAIN PATH

FORMULA:

$$L = 20\log(H) + 20\log(F) + 20\log(D)$$

D = PATH DISTANCE MI.
F = FREQ. MHZ
H = OBSTRUCTION HEIGHT FT.
L = EST. PATH LOSS OBSTACLE GAIN

TQ= THE RECEIVER QUIETING THRESHOLD IN DB.

Noise input. The effective noise input is directly related to the acceptance bandwidth of the receiver, and can be determined from the nomogram in Figure 10. The actual acceptance bandwidth of the receiver often is not specified, and must be approximated from data given in the equipment specifications or manual.

For direct FM receivers, the effective acceptance bandwidth can be approximated by the formula:

$$B=1.25(2M+2D)$$

where:

B= THE EFFECTIVE ACCEPTANCE BANDWIDTH;

M= THE HIGHEST FREQUENCY OF THE MODULATING SIGNAL; AND

D= THE MAXIMUM DEVIATION OF THE TRANSMITTER.

The factor 1.25 in the formula adds 25 percent to the required minimum acceptance--this 25 percent is an approximation of the safety factor built into most receivers to allow for oscillator drift or other circuit variations during operation.

In systems using PCM (pulse code modulation) FM, the receiver acceptance bandwidth is computed by the following formula:

$$B=2.5(M)$$

where:

M= THE BANDWIDTH OF THE MODULATING SIGNAL.

Noise Figure. A conservative noise Figure for most receivers is 12 dB. Other noise Figures can be found in the equipment manufacturer's manuals or specifications.

Fade Margin. The system fade margin is an arbitrary figure set by the results of many experiments and measurements on operational systems. Normal VHF and microwave paths usually require a fade margin of

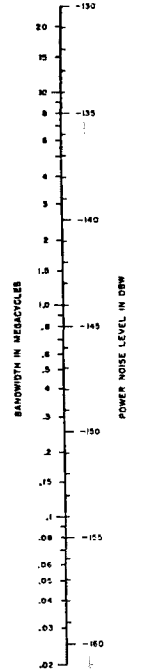

FIG 10— BANDWIDTH TO NOISE LEVEL

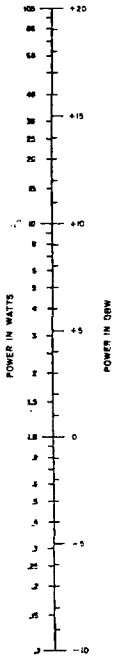

FIG 11— POWER TO DBW

approximately 20 dB. But the obstacle gain path exhibits relatively slight fading, and the necessary margin to protect against fading is only 10 dB.

Quieting threshold. The quieting threshold represents the signal level which must be maintained to provide a usable signal over the incoming noise. For most receivers, the threshold indicates an allowance of 12 dB in this formula.

For example a radio receiver has a required receiver input of -118.5 dB, computed as follows

IR=ND+NF+FM+TQ

=-153.5+12+10+12

=-118.5 dB.

Equipment combinations.

Various combinations of equipment in the system will have different values for *the maximum allowable* loss on the propagational path. The maximum allowable loss with any particular combination of equipment is computed by the following formula:

LM=PT+GP-LX-IR

where:

LM= the maximum allowable lose;
PT= the transmitter power in dB referred to 1 watt (dBw);
GP= the path antenna gain in dB;
IR= the required receiver input in dB.

Maximum transmission loss. The maximum allowable transmission lose is the greatest value of attentuation that the particular equipment combinations must overcome to provide the system with a usable circuit. This value is compared with the estimated path loss to determine whether or not the computed equipment combination will provide sufficient gain to overcome the predicted path losses.

Transmitter power. The transmitter power, referred to 1 watt, may be obtained from the nomogram in Figure 11. As an example assume a transmitter with a nominal power output of

40 watts. The nomogram shows a value of 16 dBw for this power. If the nomogram does not cover the required power Figure, then the value must be computed by the following formula:

$$PT=10\log PW$$

where:

PT= the power gain in dBw; and
PW= the maximum transmitter output power in watts.

Path Antenna Gain. This expression in the basic formula combines the apparent gains of the transmitting and receiving antennas. For example, two yagi arrays one transmitting has a gain of 6 dB and one receiving has a gain of 9 dB; the path antenna gain is the sum of both antenna gains thus the path antenna gain is 15 dB in this case.

Transmission line loss. The attenuation of the transmission line at each end of the system is computed in accordance with criteria given. The total of the losses in the transmitting and receiving transmission lines then is substituted for the factor LX in the formula.

Required Receiver Input. The value of I_R, as computed above, is substituted in this formula. Note that the computation in above results in a negative number of decibels, which must be subracted in the formula for maximum allowable loss. This entails a change of sign.

SIGNAL STRENGTH SURVEY

After the tentative transmission paths have been selected and the frequency of operation has been determined, a signal strength survey should be conducted on the sites.

The exact location of the tentative terminal site must be determined in the field. If there are prominent landmarks such as road intersections, then the location of the exact site is simplified; otherwise, experience surveyors should locate the tentative site as accurately as possible from the Quads used.

Determine the azimuth of the transmission path from one terminal location and install a temporary fixed station, with directional antenna at this site. This station is used to transmit to mobile receiving equipment at the other site. Maximum transmitter power should be utilitized during this survey.

The survey can be conducted on the exact or a relatively close frequency within 10 MHz to determine if the path as theorically determined exists. It has been my experience that in some cases (especially marginal path to equipment gain ratio cases) a path does not exist although it should, and a different path does exist most likely to a different terminal site.

Spectral Shaping of Radio Frequency Waves

by
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ABSTRACT

This paper presents a method[1] of spectrally shaping a Quadrature Phase Shift Keyed, QPSK, signal using baseband techniques applied to an RF signal. This method does not require the use of linear modulators or amplifiers or expensive bandpass crystal filters. It results in a constant amplitude signal allowing the use of Class "C" amplification without spectrum spreading, intermodulation distortion or intersymbol interference. This technique is presently used to transmit 340K bps of data in a 350F9 classification. (99% of the transmitted energy is contained in 350 kHz of bandwidth). This method is applicable to FSK and some forms of PSK when used for digital data transmission.

[1]The theory and techniques described in this paper were developed by Martin H. Beauford and Jerry J. Morton for the OPSEIS® 8600 System with patents pending. For more information about this technology or the OPSEIS® 8600 System contact Applied Automation, Inc., Geophysical Systems Division, Bartlesville, OK 74004.

INTRODUCTION

1. Any modulation (changing the carrier) of a R.F. wave spreads the spectrum.

2. The amount of spreading is a function of:

   a) the way the carrier is changed; (type of modulation);
   b) how much the carrier is changed; (amplitude of modulation);
   c) how fast the carrier is changed; (frequency of modulation);

3. Most regulatory agencies have limits on amount of spectrum spreading.

4. Digital modulation, squarewaves, cause excessive spectrum spreading over what is needed to convey the information.

5. Present methods of spectral shaping largely consist of:

   a) filtering the modulating waveform before modulating, (baseband filtering)
   b) filtering the RF spectra after modulating. (RF bandpass filtering)

6. Both methods have serious drawbacks because of physical hardware limitations when implementation is attempted.

Presentation:

A signal frequency signal with a constant amplitude is called a CW (continuous wave) signal. It occupies zero bandwidth and does not contain any time-variant information.The only information that is carried by this signal is amplitude and frequency both of which are constant with respect to time (by definition). Because the modulation varies the signal with respect to time additional frequencies are generated.

The amount that the spectrum is spread is a function of three variables.

a) The way the carrier is changed, (type of modulation),
b) the amount the carrier is changed, (the amplitude of modulation),
c) the rate the carrier is changed, (the frequency of modulation).

Of these three, the rate at which the carrier is changed, or frequency of modulation has the greatest effect on the amount of spreading. If items a & b are held constant, the amount of bandwidth required is essentially directly proportional to the rate.

Essentially, when a CW signal or carrier (fc) is modulated with a single frequency (fm), a pair of sidebands are generated. The frequencies of these sidebands are the carrier frequency plus and minus the modulating frequency (fc $\pm$ fm). Non-linear and/or exponential forms of modulation such as phase and frequency modulation generate additional sidebands at (fc $\pm$ Nfm) (and sometimes others). N is an integer from 1 to infinity.

A complex wave form consists of many frequencies of various amplitudes and phases all of which may be changing with respect to time. Modulating with a complex waveform generates many sidebands of varying amplitudes and frequencies.

Digital modulation (modulation with square waves) causes excessive spectrum spreading over what is needed to actually convey the information, primarily because the harmonics of the squarewave also generates sidebands.

Most regulatory agencies (FCC for example) have limits on how much spectrum can be occupied and also some limits on spectral distribution. The FCC defines "occupied bandwidth" as the bandwidth which contains 99% of all the transmitted power. The reason for this definition is because the FCC is primarily concerned with adjacent channel interference, not how the user actually distributes energy within a given bandwidth (Figure 1). This definition of bandwidth is obviously much wider than the 3 dB or 6 dB bandwidth described or used in most textbooks but occupied bandwidth is probably the most important specification that all of us are concerned with in any design.

The spectral distribution of any signal must be evaluated in terms of occupied bandwidth instead of the "3 dB bandwidth". Therefore, analysis of all factors and specifications is necessary in order to determine the optimum configuration for any given application. It is possible that in some applications, the amount of spectrum used is not a restriction; however, I have never ever experienced the luxury of unlimited bandwidth. Almost every application is somewhat bandwidth limited, that is a lot of information must be crammed in a relative narrow bandwidth. Other factors such as cost, complexity, error rate, acquisition time, etc., may prevent the most efficient bandwidth technique from being employed.

In many applications, a fixed data transfer rate is the primary consideration. In simpler terms; the FCC has allocated "BW" bandwidth and I must cram "BPS" bits per second of data in that bandwidth. The ratio of BW/BPS is what might be called the "bandwidth efficiency factor". If this

factor is a relative large number, 6-10 or more, almost any form of modulation will work. It is only when the factor becomes small that circuitry becomes complex. For small factors (F < 3) it is necessary to perform some form of spectral shaping to meet FCC specifications.

Figure 2 shows a carrier at 100 MHz, AM modulated 50% with a squarewave of 50 kHz representing 100K BPS data. Observe the occupied bandwidth. The first pair of sidebands contain all the information that is necessary. The additional sidebands are not necessary and only improve the shape of the received signal. If the square wave is passed through a simple RC low pass filter turning it into a triangular wave, we obtain Figure 3. Notice the reduction in occupied bandwidth by this simple shaping. Figure 4 shows modulation by a sinewave (all harmonics removed). Note again the bandwidth reduction over the triangular waveform.

Figures 5A, 5B and 5C show an FM modulation by the 50 kHz squarewave, triangular, and sinewave using a modulation index of 1.0 (deviation divided by modulating frequency equals 1.0). Again note the bandwidth reduction by spectrally shaping the modulating waveform before applying it to the modulator.

Figure 6A shows a binary PSK modulated spectrum using same parameters as in Figure 3 (AM) and Figure 5A (FM). Note that the spreading of the spectrum is even worse for PSK than for either FM Or AM. Figure 6B shows how these sidebands don't fall off very much even at 5 MHz away; (only about 40 dB reduction). Obviously shaping the modulating waveform before modulating would show a significant improvement in bandwidth reduction, but this technique requires a linear modulator. Distortion in the modulator will cause the spectrum to spread similar to the squarewave. Linear modulators are a "PAIN", because nothing is really linear. A linear modulator is only more linear than a non-linear modulator. Feedback around a modulator is sometimes used to improve the linearity. Therefore all "linear modulators" will cause more spectrum spreading than the expected amount.

Another way to reduce spectrum spreading is to filter after modulating. Invariably this technique is more difficult to accomplish because:

a) Very sharp cut-off filters are needed.
b) They must be applied at the RF frequency.
c) They introduce phase distortion (phase is not linear over the pass band).
d) They usually ring when an impulse is applied. (They cause amplitude distortion.)

Let us now digress for a minute into some of the "other" factors previously mentioned. Most of the time an error rate is specified at a given range, power level or who-knows-what, requiring the receiver to operate at the minimum signal level. In the application I will describe later this was the case. A certain receiver-sensitivity/error-rate specification along with a minimum data rate within a predetermined bandwidth had to be met, regardless of complexity or cost. In applications such as this one, PHASE MODULATION (PM) gives the lowest error rate at a given signal level compared to other forms of modulation.

But from the standpoint of occupied bandwidth or spectrum spreading, phase modulation is probably the worst form of modulation. Figures 7A & 7B show a phase modulated spectrum generated with clocked data from a pseudo-random

data generator (repeating at 255 bits), instead of a 1/0/1/0/1/0 repeating pattern as in figure 6A & B. The first nulls occur at ± clock (or ± BPS). All the needed information is contained in the main lobe (between the first nulls). All the other lobes could be eliminated as they are not necessary to convey information. They waste power and clutter up the spectrum. It is easily seen from these pictures why PSK must have some form of spectral shaping to be acceptable to the FCC.

Phase shift keying with binary digital data can use any angle of phase shift (± x degrees from 0 degrees carrier). ± 90° gives the lowest error rate because the carrier is at a null and all of the energy is in the sidebands. It is also the worst spectrally and the most complex to demodulate for precisely the same reason. No carrier exists, and to accomplish demodulation some form of a pseudo carrier must be generated. The name bi-phase PSK is often used to describe ± 90° PSK modulation.

Let us consider a different form of bandwidth compression. Assuming we have a serial stream of data being transmitted over an RF link, at "B" bits per second rate. Instead of transmitting these bits serially one at a time, suppose we take consecutive pairs of bits (1&2, 3&4, etc) and store that pair and examine the binary representation for that pair of bits or symbol which will be (00, 01, 10, 11), and then transmit this pair of bits or symbol at one of four levels.

In the case of AM it is one of four amplitude levels; for FM one of four frequencies; or for PSK one of four phases. Because the symbol rate is one half the bit rate, the bandwidth is reduced by a factor of two, therefore bandwidth compression. This technique can be extended to eight or 16 or more levels although the complexity of the receiver to detect one of sixteen levels makes it almost impossible to achieve reliable operation. I've heard of 16 level systems but I have never seen one and have no knowledge of how well they perform.

Generally doubling the number of levels of bandwidth reduction results in a net loss of slightly greater than 3 decibels. Most articles explaining these techniques show the same error rate for QPSK as PSK but careful attention should be given to the scales. Note one scale is "Eb/No" or Energy per bit divided by noise power density. In a four-level system because the signal is two parallel bit streams, each stream has half the energy per bit as a single stream for the same RMS signal level; which is a 3 dB loss per bit. Just remember: Mother nature will not let you get something-for-nothing. If the transmitter has 10 watts output, half the energy goes to each channel.

A four level PSK is known as QPSK (Quadra Phase Shift Keying) and can transfer twice the amount of data in the same bandwidth as binary PSK.

The penalties are:

1. 3 dB loss in receiver sensitivity for the same error rate.
2. Somewhat more complex and costly transmitter.
3. Considerably more complex and costly receiver.

Advantages are:

1. Twice the data rate in the same bandwidth, or
2. 1/2 the bandwidth for the same data rate.

Essentially QPSK is two (orthogonal) bi-phase PSK signals occupying the same spectrum. Because the channels are orthogonal, their spectral envelopes are identical for random data. Their nulls and peaks occur at the same frequencies. Therefore Figures 7A & B are the spectra for QPSK and binary PSK. A pseudo-random data pattern (255 bits long) is used as the modulating signal, with both channels clocked at the same rate. It is obvious that spectral shaping will be required in order to meet FCC specifications in most applications.

Because they are orthogonal, the two channels (called the I & Q channels) are independent. Different clock and data rates can be used in each channel, in which case spectrum will be different from Figure 7. If the clock and data rates in the I and Q channels are the same, the clock (or data) phases can be different. This condition is called offset or staggered QPSK. Because the channels are independent and orthogonal, the spectrum for staggered (or offset) QPSK is the same as for non-staggered QPSK. Typically the amount of stagger or offset is 1/2 bit period but the amount of stagger or offset doesn't affect the spectrum. Figure 8 shows a QPSK modulator used for either form. Figure 9 shows how the vector sums are generated.

We will now make a comparison between standard QPSK and offset QPSK with step function changes in data and phase. In QPSK, the transmitted phase can be any one of four phases, 0°, 90° 180° or 270°. The phase change between adjacent symbols can be any amount because both channels change at the same time. When both bits change at the same time the phase change is 180°. When neither bit changes, there is no phase change and when only one bit changes the phase change is either plus or minus 90 degrees. The 180° phase change is a problem. The fastest way to change the phase 180 degrees is to go through zero amplitude. A 180 degree phase change is really an amplitude change from +A to -A. As a result QPSK is considered a form of amplitude modulation.

Normally QPSK phase shifts are 0°, 90°, 180° and 270° but some other systems advance the phase an additional small amount. However when used with RF links this technique can offset the center frequency which would make the FCC unhappy.

This step function change in amplitude (also 180° phase) causes all kinds of problems when passing through narrow band filters. The filters tends to ring changing both amplitude and phase. A phase change means the channels are not orthogonal which is interchannel interference. Also because of the amplitude changes, linear amplifiers are required to obtain high power levels.

Offset QPSK (Figure 10B) changes only one bit at a time, and therefore the phase change is either 0 or 90 degrees; never more. As a result the amplitude changes are less. A phase change (or none) occurs at each 1/2 bit cell. Also note that the rate of change of phase is the same for either form of QPSK, that is the degrees per bit cell is always 180° or less and the spectrum for both is the same. These characteristics lead us to a better way of spectral shaping that has many advantages.

modulated output is connected to a tracking PLL. The output from the VCO is the spectrally shaped output. The VCO in the PLL tracks the phase change from the QPSK modulator. The low pass tracking filter bandpass characteristics are tailored, allowing the tracking oscillator to lag the phase change from the modulator, thus the rate of change of phase of the oscillator is carefully controlled to obtain the desired spectrum. The result of this PLL technique is somewhat similar to MSK (minimum shift keying) except the phase vector is allowed to rotate more rapidly in that it has acceleration and deceleration for each shift (MSK has a constant rotational velocity). It must essentially be "stopped" each time a transition comes along. The phase then starts rotating; speeds up, and as it approaches the correct phase it slows down and stops before the next bit change occurs. If the RC time constants are adjusted to give the same rotation velocity as for MSK, (it just gets there in time for the next change), intersymbol errors exist and the main lobe is widened considerably past the first nulls.

Several problems had to be overcome before the oscillator would track at the desired rate without overshoot or too much lag. The first problem is the frequency vs phase response of the transistor amplifier. The transistor finally selected has an cutoff frequency of over 400 MHz. A high cutoff frequency allows a data rate of hundreds of kHz without excessive phase shift that would cause the tracking VCO to hunt. In the tracking mode the PLL acts somewhat similar to a first order loop, acquiring lock immediately on power up. The frequency response of a first order loop is a function of loop gain and as a result the loop gain affects the spectrum, and therefore the gain must be held constant at the correct value for the filter parameters chosen. Because a level change in either the reference or VCO output could cause phase detector gain variations; a saturating (limiting) isolation amplifier keeps the drive level to the phase detector constant. A temperature and voltage compensated VCO along with regulated supply voltages and temperature compensated bias voltages are used to eliminate other possible sources of gain variations and undesirable frequency drift.

Because all other circuit variations are eliminated, the loop filter becomes the determining factor in the spectral response.

We found some very unusual characteristics to the loop filter. A second order loop filter (figure 11A & B) was tried first. As the cut-off frequency was lowered, and damping decreased, the spectral response was improved. However, serious intersymbol and interchannel interference developed. It was found that in order not to have any interference, the main lobe (between the first nulls could not be altered. Decreasing R_2 had the greatest effect on spectrum and interference. It soon became apparent that the FCC specifications could not be met without excessive intersymbol and interchannel interference. Various other circuit modifications were tried with no avail until the question was asked "What is really needed in the loop". The answer is of course, reduced loop gain at some discrete frequencies. A series L-R-C circuit from collector to base was tried and is the answer.

This L-R-C will put a notch in the frequency response reducing the gain at that specific frequency thereby putting a notch in the spectrum. It also turns out that several notches can be incorporated and they are all essentially independent. After adding the notches, more rolloff at about 2-3 MHz was required so a single small capacitor (C2) was added between base and collector to further reduce gain at higher frequencies. Figure 13A shows the QPSK output at the intermediate frequency of 30 MHz with the maximum single R_1-R_2-C_1 filtering usable without any interference (altering the main lobe). Compare 13A against Figure 7A & 8 to note spectral improvement. Figure 13B is with C_2 (High Frequency rolloff) added. Note about 10 dB improvement over 13A at 2-3 MHz.

In Figure 14A the horizontal scale of 1 MHz has been expanded to 500 kHz/division to better observe the effects adding a notch. Figure 14B shows a single high frequency notch added at the 2nd lobe giving about a 10 dB reduction in the 2nd lobe.

Figure 15 is the same as Figure 14B except the horizontal scale has been changed (to 200 kHz/cm) to better observe the effects of the low frequency notch.

Figure 16A shows the notch for the 1st lobe added but tuned below the first lobe, actually into the main lobe. Note that the main lobe has been slightly widened and the first notches are deepened and spread out from Figure 15. When tuned to the lowest frequency, intersymbol and interchannel interference are generated. In Figure 16B the notch is tuned out near the 2nd lobe reducing it more. The notch is sufficiently wide that it still reduces the 1st lobe somewhat. Lowering the frequency of the notch to the high side of the 1st lobe gives Figure 16C which is well within the FCC specifications. Actually Figure 15 just barely meets FCC specs but any variations in component values due to production tolerances could make some units not meet the FCC specifications. It was deemed necessary to incorporate the two notches in order that all production units would fully comply without any problems. Figure 17 shows the final shape compared to a clear carrier. Figure 18 shows a before-after picture of the spectrum reduction.

This technique is a powerful technique in certain applications but is somewhat costly to implement. However, it is much cheaper than some other techniques such as the use of crystal filters.

Figure 21 shows the VCO correction voltage during modulation with the two L-R-C circuits disconnected. When connected severe overshoot and ringing occur but the demodulated data has a lower error rate.

Figure 22A shows decoded data with only the RC & C circuits added to the PLL to modify the spectrum. Adding the L-R-C notches adds ringing to the demodulated signal as shown in Figure 22B. The error rate is actually improved slightly by adding the notches.

The offset QPSK eye pattern is considerably diferent than the non-offset QPSK. Because only 90° phase can be changed at any given time, the eye pattern is a square rotated 45° (diamond) with the decision points midpoint on each side (Figure 19). Added noise (poorer S/N ratio) simply smears out the decision points along with the whole pattern. As the noise

gets worse the whole eye starts filling in. No noise gives almost perfect square. The rounded corners are because of bandwidth limiting in the IF amplifier. Intersymbol interference can be detected because the decision points are not on the ±45° axis. Differences in I & Q amplitudes must he resolved before intersymbol interference can be identified.

Ringing causes small circles and loops around the decision points.

Summary:

The purpose of this presentation is to make others aware of some of the problems involved in system analysis and present one solution to excessive spectral spreading. Each system is different, and an analysis is required to correctly delineate all required system performance specifications before system design can be attempted.

Some forms of modulation (transmission of information) are more bandwidth efficient than others. Some forms have lower error rates for the same signal to noise ratio than others. Error rate and bandwidth efficiency are not necessarily exclusive. However, when both are required system complexity and cost will increase. The amount of complexity, cost, error rate, bandwidth efficiency and path loss need to be evaluated and compromises must be made to optimize the system. The actual system configuration will be a result of the weight given to each parameter when the analysis is performed.

Various users will probably assign different weights to the parameters. Other parameters not mentioned previously will obviously include battery life (power consumption), susceptibility to interference, governmental regulations, number of channels, amount of data to be gathered and others. All of these must be taken into account during the evaluation phase. Often when an analysis is performed, during the analysis the user probably will change priorities or weights assigned to the parameters because much difficulty is experienced in assigning a dollar value to a parameter value. How much is a dB worth?

The technique described herein allows a maximum data rate QPSK system to be implemented at lower cost, with a better error rate and with less occupied bandwidth than other better known techniques. It is not a cure-all and will probably not be the optimum technique in most applications. I hope this presentation has opened some new doors, given new insight or possibly been of benefit to some of the participants of this conference.

REFERENCES

A "minimum" bibliography is included to give only a place to start. Too many references exist to list more than just a few. The ones listed will refer the reader to additional material if desired.

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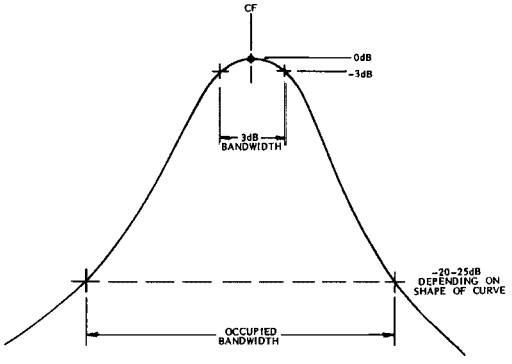


MODULATION SPECTRUM
3dB VS OCCUPIED BANDWIDTH

FIGURE 1

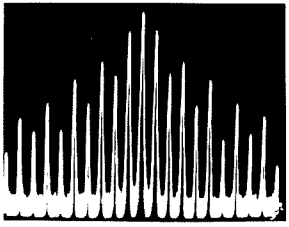


FIGURE 2
100kHz/DIV AM MODULATION 50%
SQUARE WAVE 50 kHz (100 KBPS)

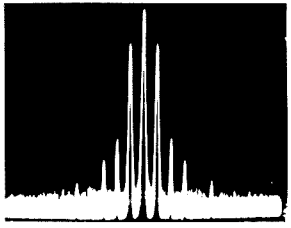


FIGURE 4
AM MODULATION 50%
SINEWAVE 50 kHz (FULLY SHAPED)
100 kHz/DIV

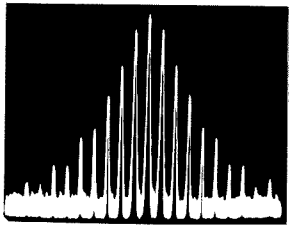


FIGURE 5B
FM MODULATION (M=1.0)
50 kHz TRIANGULAR WAVE
100 kHz/DIV

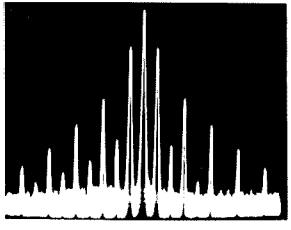


FIGURE 3
AM MODULATION 50%
TRIANGULAR WAVE 50 kHz (100 BPS shaped)
100 kHz/DIV

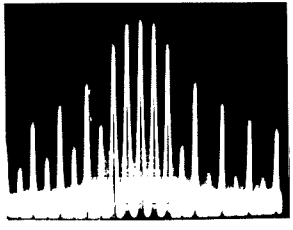


FIGURE 5A
FM MODULATION MODULATION INDEX = 1.0
50 kHz SQUAREWAVE
100 kHz/DIV

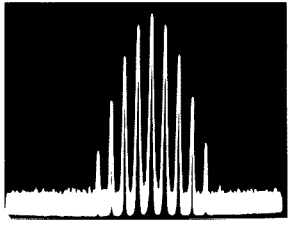


FIGURE 5C
FM MODULATION (M=1.0)
50 kHz SINEWAVE 100 kHz/DIV

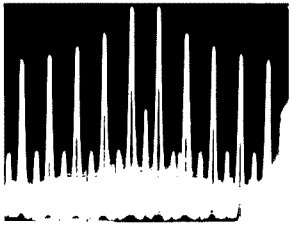


FIGURE 6A
BINARY PSK ± 90° 50 kHz SQUARE WAVE
100 kHz/DIV

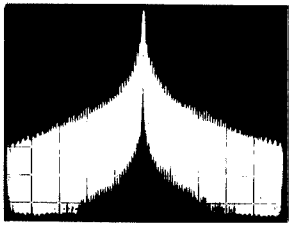


FIGURE 7A
BINARY PSK + 90°
2 MHz/DIV HORIZONTAL
DATA RATE 170 KBPS

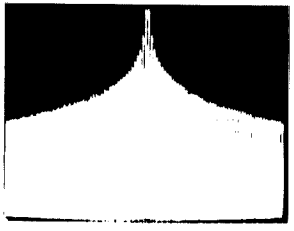


FIGURE 6B
SAME AS 7A EXCEPT 1 MHz/DIV

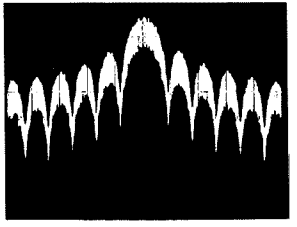


FIGURE 7B
BINARY PSK + 90°
200 kHz/DIV HORIZONTAL
DATA RATE 170 KBPS

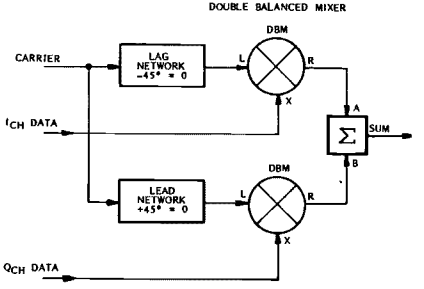


FIGURE 8
QPSK MODULATOR

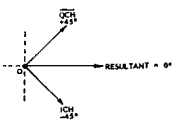


FIGURE 9A

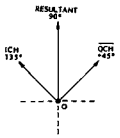


FIGURE 9B

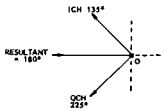


FIGURE 9C

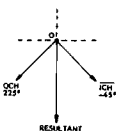


FIGURE 9D

$\overline{ICH}$ means "Not ICH" or ICH DATA = LOGIC 0

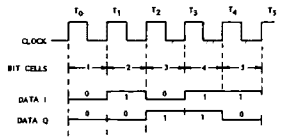


FIGURE 10A
NON-STAGGERED (STANDARD) QPSK

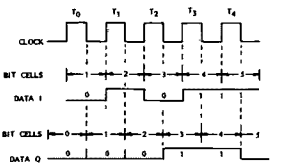


FIGURE 10B
STAGGERED (OFFSET) QPSK

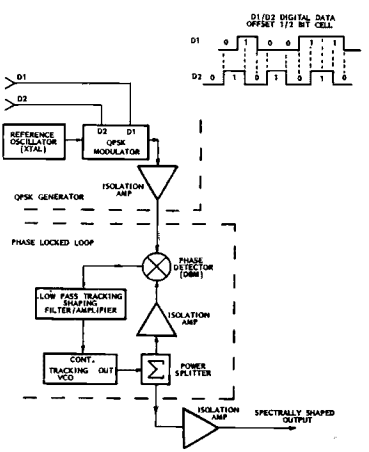


FIGURE 11

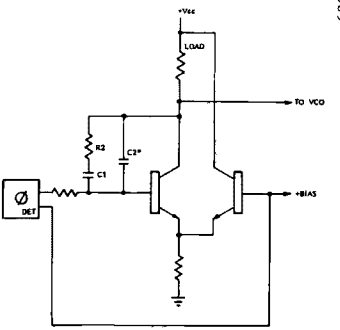


FIGURE 12
BASIC PLL LOOP FILTER/AMPLIFIER

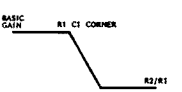
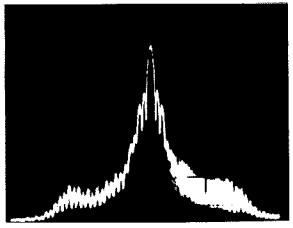


FIGURE 12A
LOOP FILTER RESPONSE

620



Refer to Figure 12

FIGURE 13A
Compare to Figure 7A & B

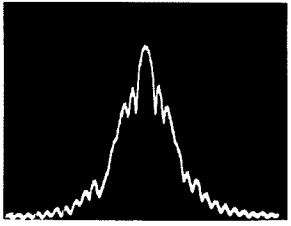


FIGURE 14A

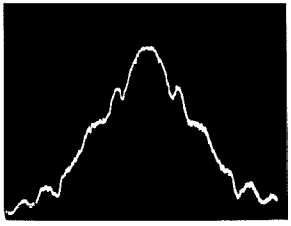


FIGURE 15
SAME AS 14 EXCEPT SCALE CHANGE

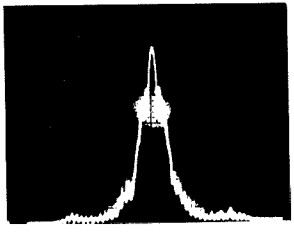


FIGURE 13B
ADDITION OF C2 REDUCTION OF 2-3 MHz TRACK

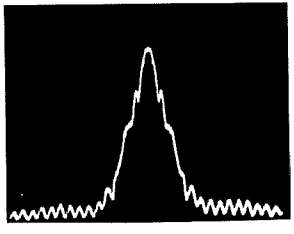


FIGURE 14B
SAME AS 14A EXCEPT 1 SERIES NOTCH ADDED

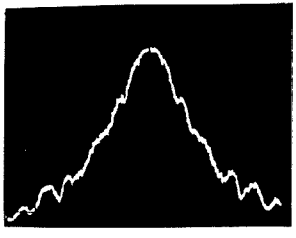


FIGURE 15A
NOTCH 2 ADDED TO LOOP FILTER

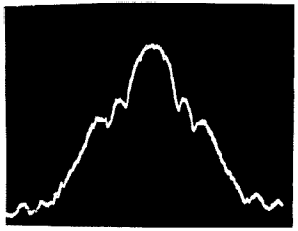


FIGURE 16B
NOTCH TUNED TO HIGHEST FREQ.

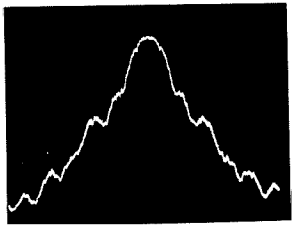


FIGURE 16C
NOTCH TUNED TO REDUCE FIRST LOBE

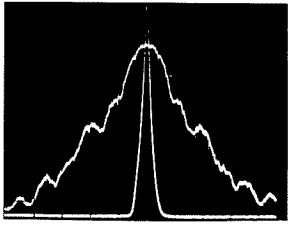


FIGURE 17
COMPARISON OF CLEAR CARRIER WITH SHAPED SPECTRUM

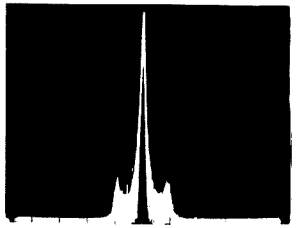


FIGURE 1A
AFTER USING SPECTRUM REDUCTION TECHNIQUE

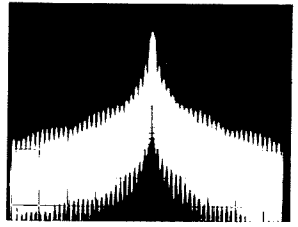


FIGURE 1AB
BEFORE SPECTRUM REDUCTION TECHNIQUE

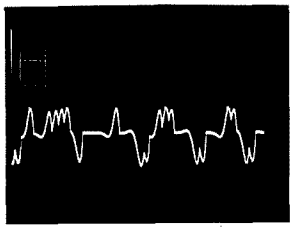


FIGURE 21
VCO CORRECTION VOLTAGE

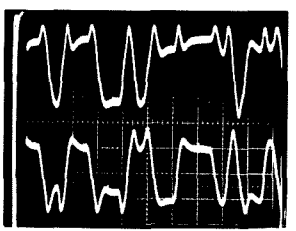


FIGURE 22 (ONE CHANNEL)

*Data made a change in the other channel during this bit period (2t).

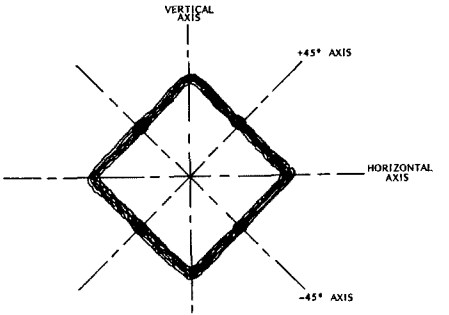


FIGURE 19
EYE PATTERN OFFSET QPSK

BROADBAND HF ANTENNA TESTING

by

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Abstract

Evaluating HF (2-30 MHz) antenna performance has historically been a difficult test problem. In recent years computer modeled approximations have typically been substituted for test data, particularly to define an antenna pattern in terms of directivity and power gain under ideal conditions. These numerical approximations work well for developing a common reference frame to evaluate the relative performance of a majority of common antenna types (monopole, dipole, sloper, vee, rhombic), but are less accurate predictors of how these antennas will perform when they interact with a real ground environment. It is well recognized that current numerical electromagnetic modeling programs are limited in their treatment of ground interactions in the HF region. Therefore, the relative comparison problem is very significant when buried or ground interactive antennas are addressed. In these special cases, antenna comparison by setting modeling conditions to an idealized ground can indicate unrealistically high relative gain expectations for standard near surface antennas and overly pessimistic values for buried antennas. In fact, some modeling conditions will indicate that the buried antenna cannot work at all!

To address the requirement of making accurate performance comparisons as well as providing design feedback, a broadband antenna test system (BATS) was developed. The system, at its current stage of development, supports computer-controlled, integrated test protocols for the evaluation of all basic antenna parameters. The BATS particularly emphasizes pattern profiles, using swept frequency techniques employing fiber-optically isolated aerial platforms as well as single frequency helicopter towed beacons. Typically, 1 to 20 full-scale antennas can be measured simultaneously in a pattern test, and then compared to each other or reference standards to produce graphic plots in terms of dBr or traceable dBi. The system reduces the complete measurement period of an antenna from months to a few weeks and provides overall accuracy on the order of +/- 1 dB.

Selected References

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9. R. G. FitzGerrell, "The Gain of a Horizontal Half-Wave Dipole Over Ground," IEEE Transactions on Antennas and Propagation, Vol. AP-15, No. 2, pp 569-571, July 1967.

10. B. Edward, "Radial Systems for Ground Mounted Vertical Antennas," QST, pp 28-30, June 1985.

11. J. W. Ames and W. A. Edson, "Gain, Capture Area, and Transmission Loss for Grounded Monopoles and Elevated Dipoles," RF Design, Part I, pp 44-45, 47, 48, 50-55, Nov/Dec; Part II, pp 12-14, 16, 17, 20, 22, 23, Jan/Feb.

12. Field Antenna Handbook, ECAC-CR-83-200, Department of Defense Electromagnetic Compatibility Analysis Center, Annapolis, Maryland, June 1984.

Selected Figures - Similar or identical to presentation slides and the figures of the paper.

Figure 1 - The broadband antenna test system components are shown in the context of three basic antenna evaluation modes.

A closed-loop, swept frequency mode drives an antenna under test and records its matching characteristics as a function of frequency. At one or more precisely located points, an electrically small broadband antenna picks up the radiated field from the antenna under test and returns it to the test van via an analog fiber optic link. The field pickup is recorded in a manner that allows direct comparison with matching data. The acquisition instrument for a closed-loop test is either a spectrum analyzer with a tracking generator or a network analyzer with an s-parameter test set.

The open-loop mode evaluates the pattern of an antenna under test by far field illumination at a series of discrete frequencies with a stable beacon transmitter having a well-defined polarization and pattern characteristic. This pattern measurement technique allows simultaneous evaluation of typically 20 full-scale reference and test HF antennas in operationally realistic environments. The absolute power gain (in dBi) of the antenna under test is tied to the predicted gain of a carefully constructed horizontal 1/2 wavelength dipole reference antenna. The dipole reference gain in the horizontal plane is transferred to a vertically polarized 1/4 wavelength monopole reference antenna by rotating the beacon axis 90 degrees and comparing the monopole versus the dipole signal levels (adapted from FitzGerrell 1967).

The open-loop mode also can be used to evaluate signals propagated from distant communications stations. Comparisons can be made between antennas in terms of signal strength and signal-to-noise ratio. If calibrated reference antennas are employed, comparisons of gain can be suggested from the data. Test antennas can be evaluated in both transmit and receive modes.

Figure 2 - This is a test configuration and a typical raw data set for a closed-loop measurement mode with a 2- to 32-MHz sweep. The FWD and REV traces (solid and short dash lines) represent the forward and reverse power levels detected by a dual directional coupler located near the feed point of the antenna under test. The SWR trace in the lower plot is calculated from the FWD and REV traces. The third trace (broken line starting at 5.50) is the field strength level received by a broadband, calibrated monopole antenna located 100 meters from the transmitting test antenna's feed point. The monopole is located on the test antenna's main beam axis at ground level (0 degrees relative azimuth, 0 degrees elevation).

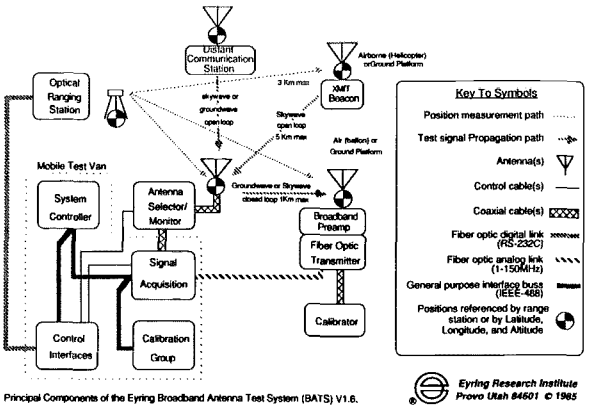
The antenna under test is a 2-element, low-profile, rapid deployment, broadband tactical HF antenna occupying an area of 25 x 200 feet with a maximum height of 2 feet above ground level. This particular antenna configuration has a usable bandwidth of over 30 MHz with an SWR of 2:1 or better.

A full correction to this data set accounts for the errors associated with cable losses, directional coupler calibration factors, and the broadband monopole response. In this example, the FWD trace corrections will produce a flat antenna input power level trace of about 18 dBm. The inflection points and slope of the FIELD trace will also change moderately. The value and units of FIELD will change significantly in converting to a corrected value in dBV/m.

Figure 3 - These are typical flight paths for antenna pattern measurements. Three types of overlapping, cross-correlating flight paths are shown. The circular flight paths are flown at flight levels that obtain azimuth patterns for four elevation angles. The slant range from the beacon to the range finder is maintained greater than or equal to 1 km (e.g., 2.3 km at 30 degrees) and is then corrected to a 1-km reference sphere centered at the antenna under test. The correction process allows comparisons to other flight levels and paths for the same antenna or between different antennas. The vertical rise and descent columns are flown at three reference points to measure antenna elevation patterns from 0 to 40 degrees. The horizontal flyover paths are flown at a constant 1-km altitude above the ground. These paths complement the vertical column flights by providing pattern information from 30 degrees to 90 degrees (zenith). Each path is flown with from one to three polarization attitudes of the beacon to allow complete response characterization (e.g., azimuth flights are flown with vertical and horizontal beacon attitudes).

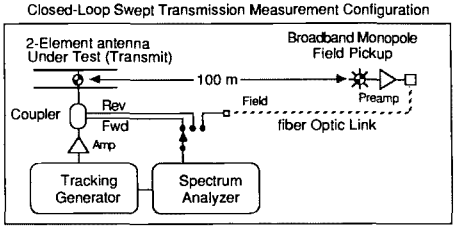
Figure 4 - The beacon that is suspended below the helicopter is shown along with its three standard flight attitudes. The beacon design is patterned after the "xeledop" concept developed by Stanford Research Institute (Barnes 1965, Barker 1973). The pattern is that of an ideal elementary dipole, which allows correction of flight data amplitude as a function of beacon pattern positioning relative to each antenna under test. The beacon attitudes are described relative to the helicopter's flight path. Therefore, to measure an azimuth pattern with horizontal polarization, the beacon would be towed horizontally on azis (HOA) in a circular path. To obtain a continuation of a vertically polarized, vertical ascent elevation pattern, the overlapping flight path would be a flyover with an HOA beacon altitude.

The beacon flight attitudes diagrammed in this figure are shown without a weight harness. In practice, a weight is suspended below the beacon to provide flight stability for towing velocities to in excess of 75 knots.



Principal Components of the Eyring Broadband Antenna Test System (BATS) V1.6.

Fig - 1



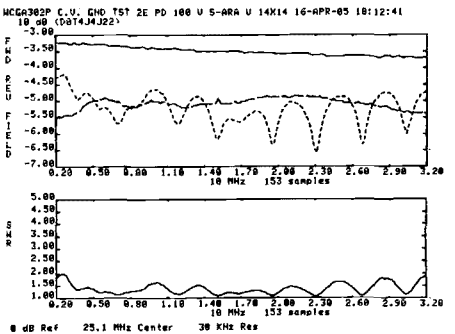


Fig - 2

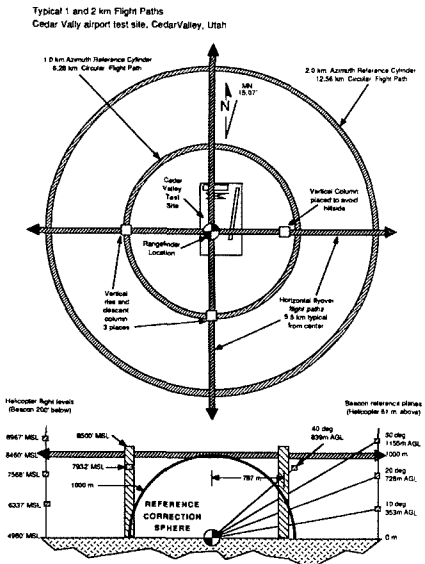
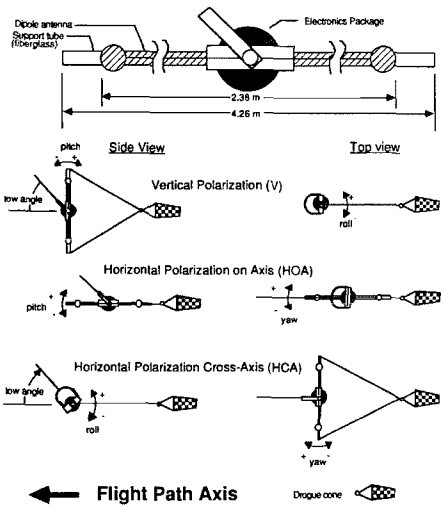


Fig - 3

Beacon Mechanical and Flight Attitudes



Airborne test terminal basic package
and flight modes for three polarization attitudes.

Fig - 4

Figure 5 - This is a plot of the azimuth response at a 30-degree elevation angle of a horizontal dipole illuminated by a 6.17 MHz horizontally polarized beacon flown in a 2-km circle about the test site location. The 1/2-wavelength (75.8 feet) dipole is positioned 2/10 of a wavelength (31.9 feet at 6.17 MHz) above the center of a ground screen (120 x 148 feet), approximating an ideal reflecting surface. The predicted power gain for this antenna at 30 degrees is 3.95 dBi (FitzGerrell 1967). The pattern approximates 3 dBi at a 90-degree azimuth (interpolated value 4.5 dBi) and 5 dBi at a 270-degree azimuth (interpolated value 5.5 dBi). The data set includes 163 samples with a point taken about every 2.3 degrees. Note the path overlap between the 125- and 140-degree azimuth positions.

Figure 6 - This figure is a complement to Figure 5. The 0-degree elevation position is the 90-degree azimuth point of Figure 5. The gain at a 30-degree elevation is 4 dBi toward the 90-degree azimuth point and 6 dBi toward the 270-degree point. These values are close to the Figure 5 values.

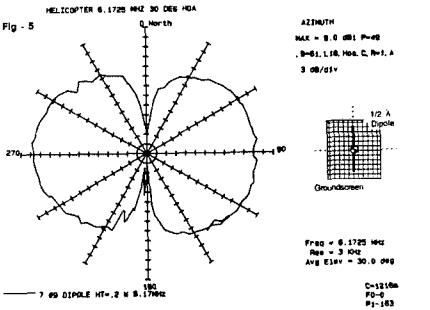


Figure 7 - This is a plot of the azimuth response pattern at a 30-degree elevation angle for a 1/4 wavelength monopole constructed with 36 radials 100 feet long (approximately 0.7 wavelength at 6.17 MHz) and 36 radials 50 feet (approximately 0.35 wavelength). At 6 MHz, the surrounding soil had a conductivity on the order of 0.006 Siemens/meter and a dielectric constant of 12.

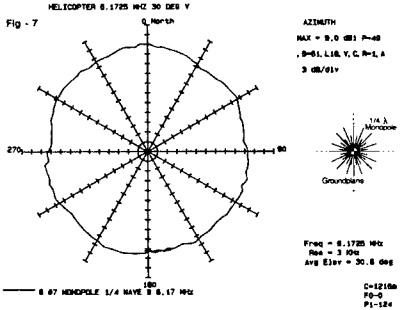
Figure 8 - This is a plot of the elevation response pattern from 0- to 40-degrees for a 1/4-wavelength monopole illuminated by a vertically polarized dipole beacon rising from the 180-degree azimuth position. This pattern suggests a response maximum of 1 dBi over an elevation angle range of 20 to 40 degrees. This is in reasonable agreement with the Numerical Electromagnetic Code modeling predictions of Edward (1985). The measured value is about 1.5 dB lower than the maximum predicted gain for the optimum elevation angle of about 23 degrees. This plot is a complement to Figure 7 which outlines the monopole configuration and environment.

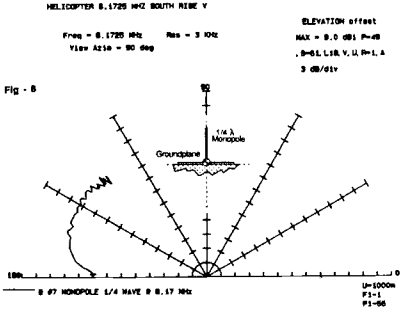
Figure 9 - This is a plot of the vertically polarized azimuth response pattern at a 30-degree elevation angle for a 500-foot long vertical half-rhombic antenna. The rhombic is supported in the center by a 46-foot steel pole. This is a typical broadband tactical antenna with a 600-ohm balun feed and a 600-ohm resistive termination. It is similar in construction to the antenna described in the Field Antenna Handbook (ECAC, 1984, pp 57-58). The antenna has a 2-dBi power gain and a beamwidth of 27 degrees and a 14-dB front-to-back ratio.

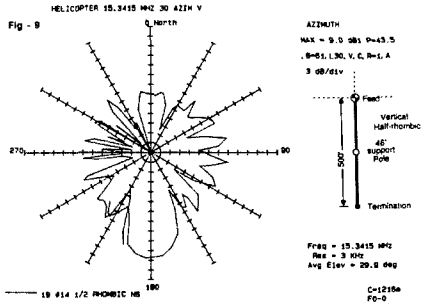
Figure 10 - This is a plot of the vertically polarized azimuth response pattern at a 30-degree elevation angle for an 8-element, low-profile, rapid deployment, broadband tactical antenna. This antenna is less than 2 feet high and is deployed in a 145 x 150 foot area. This configuration has a 2-dBi power gain, a beamwidth of 25 degrees, and a 3-dB asymetry in its bidirectional pattern. Directional deployment can produce front-to-back ratios in excess of 10 dB.

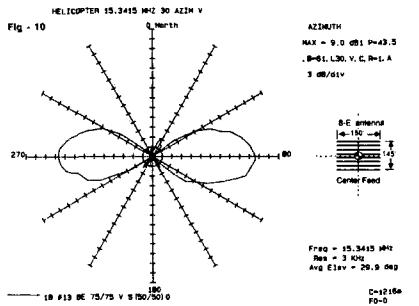
Figure 11 - This is a plot of the vertically polarized elevation response measured for an ascent column located at the 180-degree azimuth position. The peak power gain over a 0- to 40-degree elevation range is -2 dBi for this 35-foot monopole with a high performance tuner.

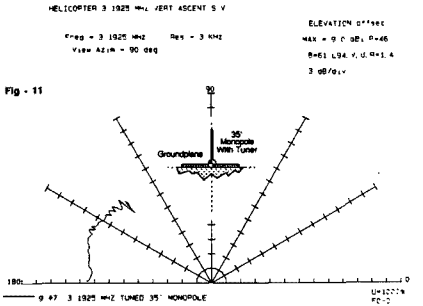
Figure 12 - This is a plot of the vertically polarized elevation response acquired in the same test as the monopole of Figure 11. The power gain of this 8-element, low-profile antenna has been optimized by asymetric deployment to match the tuned monopole power gain within 1 dB from 0 to 20 degrees. From 20 degrees to 90 degrees, it exceeds the monopole without a null and with a peak gain of -1.5 dBi.

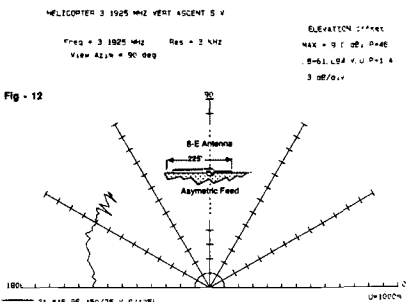





HELICOPTER 15.3415 MHZ 30 AZIM V
Fig - 9
0 North
270
90
180
AZIMUTH
MAX = 9.0 dBi P=43.5
B=61, L30, V, C, R=1, A
3 dB/div
Feed
Vertical Half-rhombic
46' support Pole
50'
Termination
Freq = 15.3415 MHz
Res = 3 KHz
Avg Elev = 29.8 deg
C=1216e
F0-0
P1-121
19 #14 1/2 RHOMBIC NS


HELICOPTER 15.3415 MHZ 30 AZIM V
Fig - 10
0 North
270
90
180
AZIMUTH
MAX = 9.0 dBi P=43.5
B=61, L30, V, C, R=1, A
3 dB/div
8-E antenna
150
145
Center Feed
Freq = 15.3415 MHz
Res = 3 KHz
Avg Elev = 29.9 deg
C=1216e
F0-0
P1-121
19 #13 8E 75/75 V S750/5010


HELICOPTER 3 1925 MHz VERT ASCENT 5 V
Freq = 3 1925 MHz
Res = 3 KHz
View Azim = 90 deg
ELEVATION Offset
MAX = 9 0 dBi P=46
B=61 L94 V, U R=1 A
3 dB/div
Fig - 11
90
35' Monopole With Tuner
Groundplane
180
0
9 #7 3 1925 MHZ TUNED 35' MONOPOLE


HELICOPTER 3 1925 MHz VERT ASCENT 5 V
Freq = 3 1925 MHz
Res = 3 KHz
View Azim = 90 deg
ELEVATION Offset
MAX = 9 0 dBi P=46
B=61 L94 V, U R=1 A
3 dB/div
Fig - 12
90
8-E Antenna
225
Asymetric Feed
180
0
21 #16 8E 150/75 V S'125'

HOW TO BUILD SIMPLE

AND NOT-SO-SIMPLE

TEST EQUIPMENT IN YOUR OWN LAB

By: Jim Weir
VP Engineering, RST
Sierra College Faculty

ABSTRACT

Design data and test results on 6 pieces of test equipment intended for "home-brew" RF measurements is given. Construction details and component sources are provided for low-level crystal detectors, low-power signal splitters, resistive low-power VSWR bridges, microstrip medium-power VSWR bridges, R + jX meters, and RF front-end noise generators.

INTRODUCTION

It has not always been possible to go down to Joe's Used Equipment Emporium and buy a Q-meter or VSWR bridge that would work at 200 MHz. In matter of fact, before Bill and Dave got into the act, quite a few RF designers had to first design and build their own test equipment, and then use this home-made gear to test their new products.

It is also true that of any random group of RF engineers, over 50% will some day start their own company. A new enterprise such as this is not always flush with venture capital; at times it becomes a matter of economic necessity to "roll your own" test gear. While not quite as pretty as store-boughten test equipment, these boxes have served their intended function in my personal company for over 20 years. Although the photos (for the most part) show nice neat construction, you must remember that these particular boxes were constructed of easy-to-obtain components and manufactured for the photographs in this paper. The original pieces of gear would gladden the heart of those of you fond of webs spun by stoned spiders.

Finally, to those of you offended by my admittedly simplistic and anachronistic concepts, I commend to you the wisdom of the philosopher who said, "Those of us who do not remember the ways of the past are surely condemned to repeat them." Those of you who have been around this business for a significant fraction of a century know full well that these designs are not new. I claim neither invention, advancement of the state of the art, nor brilliant insights into these products; I, like you, am a poor workaday sluggard trying to keep the company one step ahead of the wolf in IRS clothing. Enjoy.

THE SIMPLE CRYSTAL DETECTOR

Crystal detectors have been with us since that unknown experimenter first jabbed a chunk of lead sulfide (galena) with Junior's diaper pin and noted that all of a sudden that his baby got rhythm. Further investigation showed that if any semiconductor (galena, germanium, silicon, gallium arsenide, selenium, etc.) was alloyed either by pressure (catswhisker) or by diffusion, the resultant JUNCTION would pass current in one direction only, and thus make a very good amplitude or envelope detector. In the ensuing years, we have done little other than refine the manufacturing techniques of the crystal diode, and to this day, there is no better generally available detector than the old faithful catswhisker germanium diode.

RADIO SYSTEMS TECHNOLOGY
13281 GRASS VALLEY AVENUE
GRASS VALLEY, CA 95945
(916) 272-2203 123.3MHz

Admittedly, you can't really call a crystal detector design that uses a diode available in the late 1940's the cutting edge of technology. However, as a lab partner, I would consider this design as my most-used piece of test gear. Although the design appears to be cut-and-dried, there are a couple of subtleties that you ought to be on guard for. (See Schematic 1). AUTHOR'S NOTE — 1N270 and 1N34 are interchangeable in all the designs in this paper.

First, the input is terminated in 47 ohms in order to work in a 50 ohm system. Yes, if you have 51 ohms in the stockroom, that would be a better match, but my company only keeps the 10% values on the shelf. Be sure that you use a carbon composition or carbon film resistor to keep the reactive part of the resistor to a minimum. I think it is obvious that if you need any other input impedance, just change the resistor to any value you please. The intrinsic impedance looking into the unterminated input is not measurable easily; the best I can say is that it is above 5K ohms (the limits of my equipment.)

The input coupling capacitor is a .001 uF. If I had intended for this detector to be used much above 150 MHz, I would have reduced this capacitor to 100 pF or so. Although at 150 MHz the .001 is well above it's self-resonant frequency, the input impedance of the diodes is so high (5K ohms) that a little jX doesn't seem to make much difference.

The diodes are the aforementioned World War II design 1N34 (or 1N270) germanium parts. Yes, I've tried hot-carrier and Schottky barrier devices and I cannot get them to do as low a level of detection as the good old germanium diodes.

50 pF was used as the bypass capacitor simply to keep any self-resonance above 200 MHz. (A 50 pF disk ceramic with 3 mm leads has a self-resonance at about 250 MHz.). BE CAUTIOUS of fooling with the 10K - 50 pF time constant. This author grabbed what he thought was 50 pF (and what turned out to be a miniature .005 uF) to make a detector and then spent DAYS trying to figure out why his AM transmitter was both audio frequency sensitive and would not modulate worth a hill of beans.

Photo 1 shows the old-faithful open-board design. While somewhat primitive, this little rascal has been my bench companion for over 20 years. I will caution you, though, that this open-board construction bit me on the behind a couple of years ago. I was working on a 20 watt 125 MHz. transmitter, and had about 30 dB of padding between the transmitter output and this detector. One day the modulation would look crisp and clean, and the next day the whole modulation envelope was garbage. After redesigning the modulator, the output bandpass filter, the final stage feed network, the driver, and several miscellaneous stages, I noticed that simply repositioning the crystal detector made all the difference in the world. Placing tinfoil all around the detector cleared up all the distortion! The high-power RF stage had been radiating directly into the detector diode leads, and the phase of the directly radiated signal combining with the attenuated signal was a function of how far the detector was from the finals. Photo 2 shows the solution to this little problem. One question may be where to buy the brass tubing for the shield. Any hobby model shop worth their salt has a large selection of thinwall brass tubing that will fit the BNC connectors as a slip fit.

This detector can be built for less than a dollar in components for the open-faced version and less than three dollars for the closed-in version (including connectors for the closed version).

SIGNAL SPLITTER

With most transmitter projects, I like to look at the swept frequency response, the spectral analysis (for unwanted birdie products), and have a counter on the output in case I want to set a spot frequency. Without some sort of splitter, I am forever swapping coax connectors from the transmitter output to one piece of test equipment or another.

The type of splitter I have found most useful is one that is matched at the input to 50 ohms and splits the signal equally between two outputs. I also demand that the outputs be isolated from one another so that if I need to take one of the test instruments off the line for a quick check of some sort that it does not upset the other measurement. The third output I have found to be most useful is a -20 dB. coupling of the input for a frequency counter or

deviation meter. Usually, I have the transmitter padded down to the +10 dBm level by the time it hits this splitter, so power dissipation is not a real problem.

Photo 3 and Schematic 2 show the construction of a "Wilkinson" style hybrid splitter constructed from two pieces of 75 ohm coaxial cable and one balancing resistor. The -20 dB. coupler is comprised of two resistors.

As you can see from the test results on the schematic, the coupling to the output ports is remarkably constant over two octaves, but the isolation and input VSWR is rather sharply tuned. The design center frequency of this particular splitter was 125 MHz., and both input return loss and output isolation remained within -18 dB from 100 to 150 MHz.. Since the -20 dB port is resistive, you might expect it to remain fairly constant, and it does so from 50 to 250 MHz..

VSWR DETECTOR - LOW POWER

This VSWR indicator has seen yeomen work in our sweep testing of filters, first-cut antenna testing, and RF input matching. Although the resistive coupling limits the input power to a half a watt or so (due to the use of quarter-watt resistors), this little board has been in on the design of dozens of VHF antennas and amplifiers. (See Photo 4). For those of you with a neatness fixation, Photo 5 shows the circuit built into a "Hobby Shack" minibox. The circuit design is given in Schematic 3, along with a performance graph. Using all new parts, this bridge can be built for less than a dollar in components and less than $3 including connectors.

Those of you familiar with the literature on this bridge in the various radio amateur handbooks may be a bit surprised at the resistor values. Most of the articles in the handbooks use 50 ohm (47 ohm) resistors throughout the bridge; the values presented on the schematic have evolved over the years as the best compromise for open-short ratio and depth of null with a precision 50 ohm load. Once again, if you are using this bridge to make swept frequency measurements, the 10K - 50 pF time constant sets the upper audio frequency response limit. If you find that too much of your fine detail is missing from the sweep response curve, either slow the generator sweep speed down or reduce this time constant.

VSWR DETECTOR - HIGH POWER

When dealing with power amplifiers, it is nice to be able to drive a couple of watts into the input and check for match. Also, it is quite helpful to be able to take the 10 or 20 watts out of a power amplifier and check the VSWR of the antenna or load that you are driving into.

The VSWR detector shown in Photo 6 uses a microstrip directional coupler design (called a "Monimatch" by some old-timers) that first saw the light of day as a coaxial device made by inserting a thin piece of enameled magnet wire between the braid and center insulator of a piece of coaxial cable. Later refinements have allowed us to used etched circuit board and microstrip techniques to achieve the same results. See Photo 7.

The circuit and etching dimensions shown on Schematic 4 should allow the clever engineer the capability of reproducing this bridge for his own use. The open-short ratio is remarkably good for a device as simple as this one, and the bridge has been used from 20 to 200 MHz. with excellent results. Since the coupling between main line and coupled line is on the order of 20 dB., there is very little loss in the main line, and the bridge will actually work down to about a milliwatt (dependent a bit on frequency) in the main line. Upper power limit is a function of the diode breakdown voltage; using the specified IN270, I would feel uncomfortable with more than 100 watts at VHF in the main line. Using the parts list given, this bridge can be built for less than $20, not including the cost to etch the pc board.

R + jX BRIDGE (RX METER)

Although it is nice to know the input VSWR of your new design, there are times when it would be preferable to know the input impedance as it actually exists at the frequency you actually intend to use it. For instance, perhaps the data sheet does not cover the transistor you want to use in the mode you want to use it. You must then measure the device under actual operating conditions to characterize and analyze the little rascal. Another use of the RX bridge is to measure component values using actual lead lengths used in your circuit. You'd be surprised how many picofarads a 100 pF. capacitor at 100 MHz. measures with half-inch leads (it's darn near a short circuit). It is nice, also, to be able to drive a hundred milliwatts or so of RF energy into a class C amplifier transistor to be able to measure the input impedance under actual conditions.

Most articles in the handbooks use either war-surplus antenna tuning capacitors (WW II, that is), or an unusual "differential" capacitor made by the Hackensack Capacitor and Store Door Company of Horse Cave, Kentucky -- it is only available from Bill's Garage and Hi-Tek Component store in East Bumpoop, Tennessee, and then only on alternate Tuesdays. The one in this article uses one section of the RF tuning capacitor out of any standard FM pocket radio.

The resistive bridge is nothing more than our old friend the wheatstone, with as much of the stray reactance as possible removed from the circuit by means of heavy wire bonding and the use of a brass ground plane behind the front of the chassis. See Photo 8 and Schematic 5.

The reactance part of the bridge is also quite simple; it is a parallel resonant circuit comprised of the aforementioned FM radio tuning capacitor and an inductor wound from #18 wire and tapped so that it could be switch-selected to various inductance values.

Once again, most circuits of this type use a sensitive 50 uA meter as the null indicator. Not only are these meters expensive, but if you happen to put in a little too much RF and the bridge is badly unbalanced, you now have your meter needle neatly wrapped around the peg of what was your meter. I much prefer to use a garden-spec op-amp and limit the current out of the amplifier into a cheap 1 mA. meter to about 150% of full scale. It will still bang against the peg if overloaded, but it will not destroy itself in doing so. Not only that, but your sensitivity is about 10 times greater with the amplifier than with the straight meter.

Calibration of the bridge is rather simple. Input an RF signal at about one milliwatt at the lowest frequency for which full-scale CCW rotation of the tuning capacitor (maximum capacitance) is nullable at some setting of the inductor. For this particular bridge, that frequency happens to be 30 MHz.. Null the meter as best as possible and use carbon comp or carbon film resistors to calibrate the 500 ohm potentiometer. I have calibration marks from 10 ohms to 2.2K ohms. Then take 20 pF. capacitors and calibrate the tuning capacitor. With the specified capacitor, you will be able to get marks from 20 to 160 pF. at 30 MHz..

To use the bridge, simply input the desired RF signal and place the bridge tuning capacitor at mid-scale directly on one of the calibration marks. Turn the bridge potentiometer to infinity and adjust the inductor switch for best null. Slightly adjust both tuning capacitor and potentiometer for the deepest null obtainable. Then place the unknown load across the load terminals and adjust the capacitor and potentiometer for null. The resistive part of the load is read directly from the calibration marks of the potentiometer and the PARALLEL EQUIVALENT reactive part of the load is the DIFFERENCE between the starting point on the variable capacitor and the final null value. If you go clockwise, your load is that many picofarads capacitive, and if you go counterclockwise, the load is that many "picoferads" inductive. (For those of you working around digital engineers, just start talking about inductance as being measured in picoferads and watch the strange looks on their faces.)

The bridge rapidly loses accuracy above 100 MHz.. This is due to the rather wide spacing of the front-panel components (see Photo 9) and the resultant parasitic inductance of the wires necessary to connect the components together. As this bridge was meant for use on a 50 MHz. project, the frequency limitation was not a great problem. If it ever became necessary to increase the frequency range of the unit, I would probably do away with the switched inductor (the cause of most of the parasitic inductance) and simply build a bridge for each frequency band of interest. One fixed inductor with this capacitor ought to be able to cover an octave of useful range without a lot of trouble.

RF NOISE GENERATOR

In the design of low-noise RF "front ends", the device of choice for final design tweaking is the good old Noise Figure Meter. This is a rather large and expensive instrument that uses a vacuum tube (or a small expensive instrument that uses a solid-state noise source) to produce an exact amount of broadband noise that may be used for an exact calculation of noise figure. The noise generator in this article will NOT give you an exact noise figure measurement, but will give you a method of tweaking your RF stage for best noise performance. Given a very short equation and a couple of fairly easy measurements (which you will have to take anyway for making up the specifications), the noise figure may be easily calculated.

As those of us who thought we knew how to design power supplies found out, a diode in reverse breakdown (i.e. a "zener") that is unbypassed for RF makes a perfectly marvelous noise generator. This noise generator makes use of the fact that a zener is wonderfully noisy and amplifies that noise in a wideband amplifier to produce about 15 dB of "excess" noise. See photo 10 and Schematic 6.

The old way to use one of these noise generators was to set the volume control of the receiver under test to a reference level, input the excess noise source, and adjust the input amplifier conditions (bias, tuning, input match, etc.) for best ratio of reference level to level with the excess noise input. The only problem was that with input changes, so changed the reference level, and thus it became an iterative sort of process -- set the reference, tune, set the reference, tune, set the reference... . This got very old very quick.

This generator, though, uses an audio oscillator to gate the noise source on and off. Now the engineer has the choice of viewing the output of his receiver on an oscilloscope and be able to look at the reference level and the excess noise level at the same time. Not only that, but by a judicious choice of gate frequency (1000 Hz.), the old standby "S15" type of SWR indicator (which is nothing more than a very narrowband 1000 Hz. meter calibrated in decibels) can be used as an indicator of best noise figure. The entire noise generator is constructed on a single piece of scrap pc board (see Photo 11).

Of course, this generator cannot be used for absolute noise-figure measurements, but by knowing the bandwidth of the receiver and the input signal to produce a given signal-to-noise ratio, the noise figure may be easily calculated.

CONCLUSION

This paper was meant more as an introduction to the fledgling RF engineer into the wonderful world of making measurements on a shoestring than to the old-timer that has seen these circuits being used for years. I do NOT begrudge the purveyors of kilobuck test equipment the right to chuckle a bit at the homespun roughness of the cloth from which these test boxes were cut, but I would point out that making and using equipment like this just whets the appetite to get your hands on a really nice piece of gear.

Not only that, but it's more of fun to see just how close I can come with one engineer using hackysack parts to Bill and Dave's boxes that have hundreds of engineers using Mil-Spec pieces. You'd be surprised; try it, you'll like it!

BIBLIOGRAPHY

1. Widin, "SWR Bridge", Ham Radio, October 1971, pp 55-56

2. Keen, "A Simple Bridge For Antenna Measurements", Ham Radio, September 1970, pp 34-38

3. Kluge, "Noise Bridge Simplifies RF Measurements", EDN, July 1985, pp 61-62

4. Willmar K. Roberts, "A Guide To F.C.C. Equipment Authorizations", published by the author, W.K. Roberts - A637 Van Kleek Dr. -- New Smyrna Beech FL 32069 -- (904) 427-3612.

5 Helge O. Granberg, "Linear Amplifiers for Mobile Operation", Motorola applications note AN-762, 1976

6. "The ARRL Handbook", 42nd Edition (1965), "The Monimatch", pp 356, 357.

7. "An N-Way Hybrid Power Divider", IRE Trans MTT, Ernest Wilkinson, January 1960, pp 116-118.

PARTS SOURCES

1. Mouser Corporation, 11433 Woodside Ave., Santee CA 92071, (619) 449-2222. Suppliers of germanium diodes, resistors, capacitors, integrated circuits, FM radio tuning capacitors, rotary switches; general catalog available for the asking.

2. Calrad Electronics, 819 N. Highland Ave., Los Angeles CA 90038, (213) 465-2131. Suppliers of meters, chassis boxes, jacks, plugs, binding posts; general catalog available for the asking.

3. Radio Shack. Available in your own home town.

-30-

PHOTO CAPTIONS

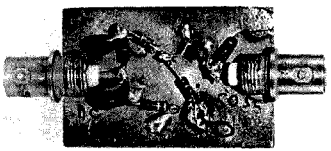


PHOTO 1 The basic, elementary form of the detector. This is Old Faithful. I've replaced her input resistor a dozen times, her diodes more than once, and she just keeps on chugging. Building this detector on a PC board scrap makes repair quite simple and frequency response excellent past 400 MHz.

PHOTO 2. When the outside world interferes with the the detector, the only answer is to shield it. A nickel's worth of brass prevents direct radiation into the diodes.

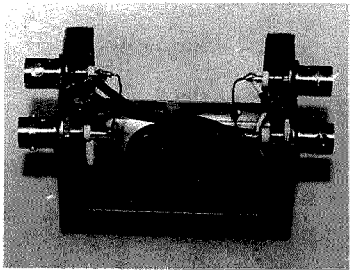


PHOTO 3. The splitter coax is shown rolled up to fit into the chassis.

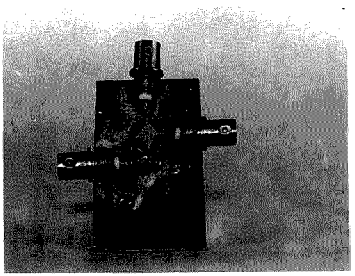


PHOTO 4. The innards of the homebrew VSWR bridge. Once again, the techniques of building homebrew circuits on scrap PC board material are illustrated.

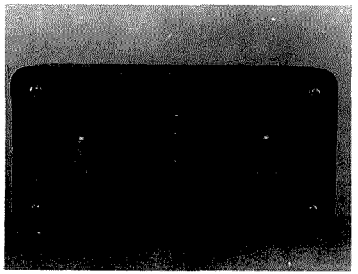


PHOTO 5. If the beamcounters want to see neat, clean programs, then show them these circuits dolled up in store-boughten housing.

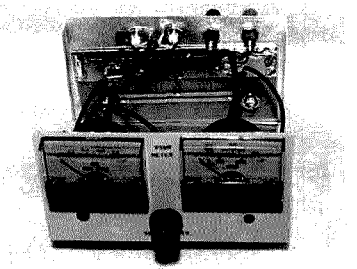


PHOTO 7 The RF coupling lines on the back of the chassis show how the microstrip design is implemented. The 39 ohm matching resistor is the central part of the photo.

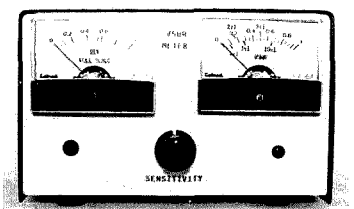


PHOTO 6. Dual meters on the faceplate make VSWR measurements a single knob task.

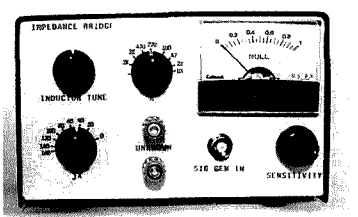


PHOTO 8. The Impedance Bridge will analyze parallel impedances from 20 pf to 10 ohms.

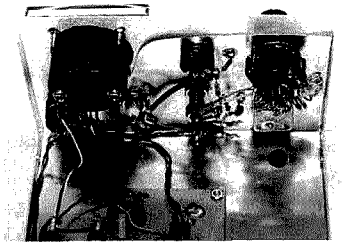


PHOTO 9 The front panel of the Impedance Bridge shows the brass ground plane below the RF front panel components. All RF ground connections are made to this brass plane.

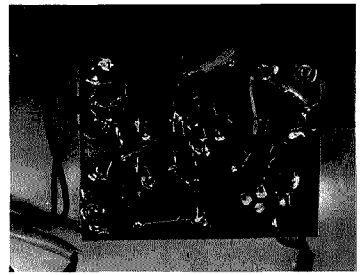


PHOTO 11 The home-brew circuit board of the noise generator. Note that all connections are made as short as possible, and that the scrap circuit board substrate is used to keep ground leads as short as possible.

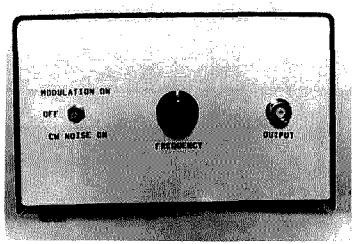
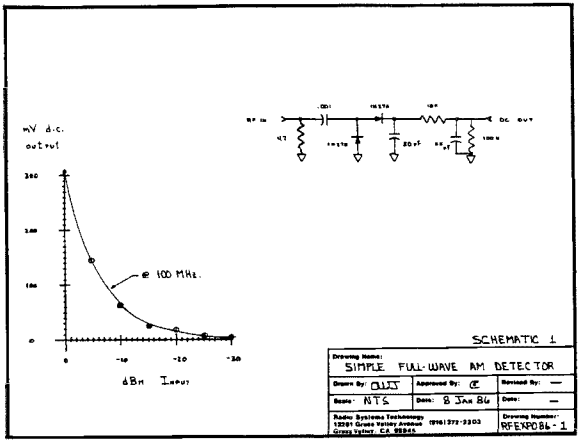
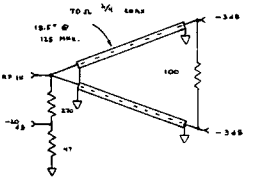


PHOTO 10 The front panel of the RF noise generator. Note that both continuous noise, modulated noise, and noise off can be selected by the front panel switch.



SCHEMATIC 1

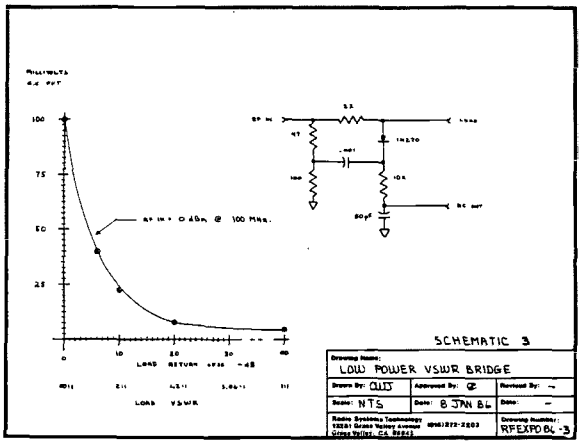
Drawing Name: SIMPLE FULL-WAVE AM DETECTOR			
Drawn By: CWJ	Approved By: CE	Revised By: —	
Scale: NTS	Date: 8 Jan 86	Date: —	
Radio Systems Technology 13241 Grass Valley Avenue Grass Valley, CA 95945 (916)272-3303		Drawing Number: RFEXPO86-1	

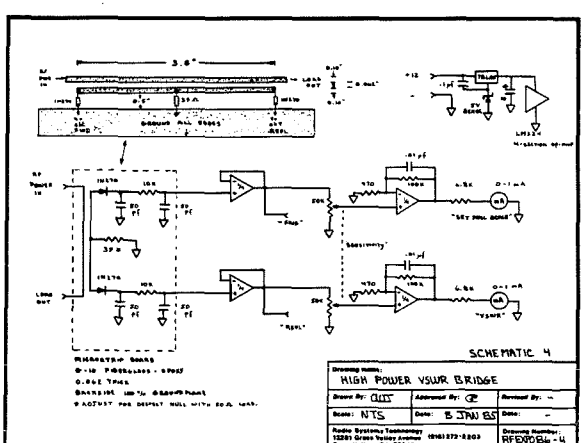


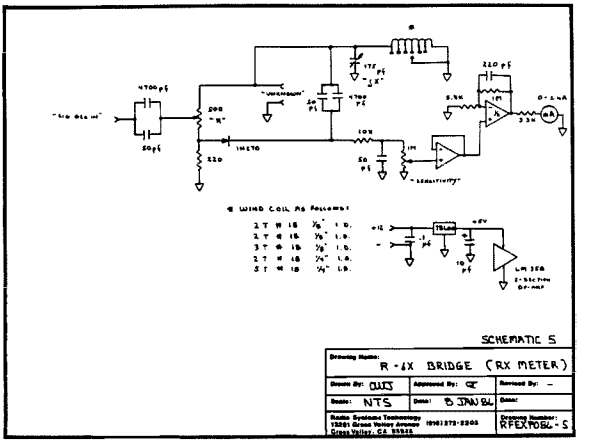
FREQ MHz.	INPUT VSWR	COUPLING @ -3dB	COUPLING @ -10dB
80	1.71	4.0	11
100	1.3	3.8	11
120	1.3	3.8	13
200	1.9	4.2	11
260	3.0	4.4	11
125	1.05	3.5	22

SCHEMATIC 2

Drawing Name: HYBRID POWER SPLITTER			
Drawn By: CWJ	Approved By: CE	Revised By: —	
Scale: NTS	Date: 8 Jan 86	Date: —	
Radio Systems Technology 13241 Grass Valley Avenue Grass Valley, CA 95945 (916)272-3303		Drawing Number: RFEXP86-2	

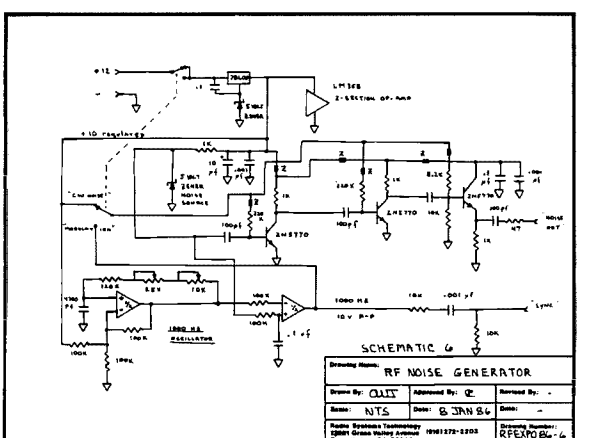

100
75
50
25
0
10
20
30
40
LOAD RETURN
LOAD VSWR
RF IN + 0.45n @ 100 MHz.
52
47
100
100K
50pF
RF OUT
SCHEMATIC 3
LOW POWER VSWR BRIDGE
Drawn By: CWS
Approved By: CE
Revised By: --
Scale: NTS
Date: 8 JAN 86
Date: --
Radio Systems Technology
12281 Grass Valley Avenue
Grass Valley, CA 95945
(916) 272-2803
Drawing Number:
RFEXPD86 -3


3.6"
SCHEMATIC 4
HIGH POWER VSWR BRIDGE
Drawn By: CWS
Approved By: CE
Revised By: --
Scale: NTS
Date: 8 JAN 86
Date: --
Radio Systems Technology
12281 Grass Valley Avenue
Grass Valley, CA 95945
(916) 272-2803
Drawing Number:
RFEXPD86 -4



SCHEMATIC 5

Drawing Name: R-jX BRIDGE (RX METER)		
Drawn By: CWS	Approved By: [illegible]	Revised By: -
Date: NTS	Date: 8 JAN 86	Date:
Radio Systems Technology 13201 Grass Valley Avenue Grass Valley, CA 95945 (916) 272-2203		Drawing Number: RFEXP86-5



SCHEMATIC 6

Drawing Name: RF NOISE GENERATOR		
Drawn By: CWS	Approved By: [illegible]	Revised By: -
Date: NTS	Date: 8 JAN 86	Date: -
Radio Systems Technology 13201 Grass Valley Avenue Grass Valley, CA 95945 (916) 272-2203		Drawing Number: RFEXP86-6

DISTRIBUTED 2-20 GHz MONOLITHIC GaAs FET AMPLIFIER DESIGN

by
Gary G. Hawisher, EEsof Incorporated, Westlake Village, CA
and
Tim Auat, Hughes Aircraft Company, El Segundo, CA

Introduction

Distributed or traveling-wave amplifier designs have come into new light with the advent of MMIC technology [1] [2] [3] [4]. The topology of a distributed amplifier, employing several active devices linked in a ladder structure, is practical and desirable to implement with FETs in GaAs MMIC technology. When properly designed, the distributed amplifier will have a gain-bandwidth product which exceeds the gain-bandwidth product of the individual FET devices. Considering also that the coupling structure required to tie several FET devices together is broadband, leads to amplifier designs which exceed decade bandwidth. Now with GaAs foundries becoming more popular, MMIC design is within reach of many small companies that formerly could not enter the monolithic arena.

Since tuning is generally limited on MMIC prototypes and the cost and time to build test circuits is high, the ability to accurately design and model the performance of a proposed monolithic design is vital. With highly accurate software now available on personal computers, many small companies can now afford the CAD tools available for circuit design which can greatly speed the design process, drastically reduce the cost of design, and improve circuit performance.

The purpose of this paper is to demonstrate computer-aided design techniques with the design of a monolithic distributed amplifier. Although the amplifier described here has never been built, similar designs are being pursued by several major contractors. Touchstone (TM, EEsof Inc.) is used to perform the circuit analysis and optimization.

Basic Design

The topology of the distributed amplifier (Figure 1) consists of an input (or gate) line, and an output (or drain) line, coupled together by several FET devices.

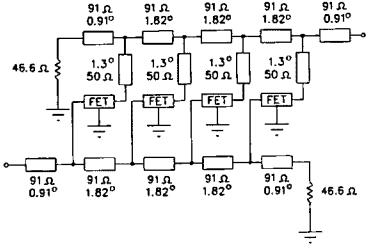


Figure 1. Basic topology of distributed amplifier showing final circuit values for 2 to 20 GHz amplifier

The gate and drain lines form artificial transmission lines, each section loaded by parasitics of a FET device. This is the key to the success of the distributed amplifier. The capacitive parasitics of the FET on both the gate and drain side are absorbed into the low pass structure of the transmission lines. This allows a very broadband match into the FET as long as the cutoff frequency of the low pass line can be made sufficiently high. The lumped inductors which normally form the series elements of the low-pass line are implemented as electrically short microstrip transmission lines. For the distributed amplifier to function correctly, the gate and drain lines must have the same phase velocity. This assures summing of the signals at the output. Requiring that the gate and drain lines have the same cutoff frequency guarantees this. [2]

The Constant-K Line

The constant-k transmission line model is chosen as the basis for the gate and drain lines. This lumped ladder filter is composed of several LC sections as shown in Figure 2, and exhibits a constant characteristic impedance along the line. The simplified FET model is shown in Figure 3.

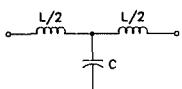


Figure 2. A section of constant-K transmission line.

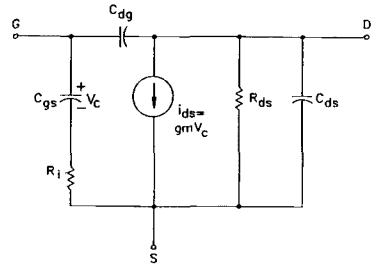


Figure 3. Simplified FET model.

If the model is split into gate and drain sections, each section can be incorporated into the gate and drain lines as the shunt capacitive portion of a transmission line section. The characteristic impedance and cutoff frequency of the constant-k line are given by (1) and (2) for an ideal line.

$$R = \mathrm{SQRT}(L/C) \quad (1)$$

$$Fc = 1 / (PI*\mathrm{SQRT}(L*C)) \quad (2)$$

The gate and drain lines will be lossy due to associated resistances of the FET. As mentioned before, the cutoff frequencies for the gate and drain lines should be the same, requiring that the LC product for the gate and dral lines be equal.

The FET Device

In designing an amplifier, one of the most important aspects is device characterization. Generally, a test device is developed and S-parameters are measured. These S-parameters can be used directly in the computer design, or a device model can be developed which behaves like the measured device. It can be very useful to predict the performance of a hypothetical device which is modeled by an equivalent circuit linked to the fabrication process. Computer modeling is used effectively for modification of FET design to fit the circuit application. [5] It is a major advantage in MMIC design to be able to tailor active devices to fit the application.

This paper will not explore techniques for modification of the FET design to improve circuit performance except to estimate the effect of changing the gate width of the device. A realistic FET model is shown in Figure 4.

This model is reported to match de-embedded S-parameters for a real 0.5 x 250 micron FET over the 1 to 18 GHz range. [1] Changes in the electrical parameters due to changes in gate width are generally understood and can be estimated by simple equations. The computer model to generate S-parameters for an arbitrary gate width FET is shown in Figure 5. The equation capability of Touchstone (TM) is used to relate the device parameters to the gate width.

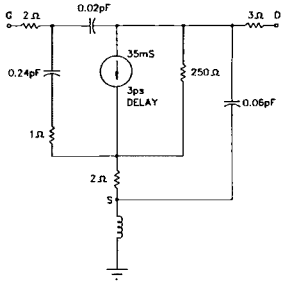


Figure 4. A realistic FET medal.

```
! Figure 5:  This file is used to generate single gate and dual gate FET
! parameters for arbitrary gate width FET devices.
! For more information on model, see W. Kennan, N. K. Osbrink, "Distributed
! amplifiers: Their time comes again" Part 2, Microwaves & RF, Dec 1984

  VAR
    GATE = 300                  ! gate width of device
  EQN
    GM  = 0.00014 * GATE        ! width dependent device parameters
    Cgs = 0.00096 * GATE
    Ri  =     250 / GATE
    Cdg = 0.00008 * GATE
    Rds =   62500 / GATE
    Rd  =     750 / GATE
    Cds = 0.00024 * GATE
    Cdi = 0.00008 * GATE
  CKT
  ! basic FET model structure
    RES 1 2 R=2
    CAP 2 3 C^Cgs
```

```
  RES 3 4 R^Ri
  RES 4 6 R=2
  CAP 2 5 C^Cdg
  VCCS 2 5 3 4 M^GM A=0 R1=0 R2^Rds F=0 T=3
  DEF3P 1 5 6 FETMOD
! single gate FET model
  FETMOD 1 2 3
  IND 3 0 L=.04
  CAP 2 3 C^Cds
  RES 2 4 R^Rd
  DEF2P 1 4 FET1 FET300   ! name of FET sparameter file
! dual gate FET model
  FETMOD 1 2 3
  IND 3 0 L=.04
  CAP 2 3 C^Cds
  RES 2 4 R^Rd
  FETMOD 3 5 4
  CAP 4 5 C^Cdi
  RES 5 6 R^Rd
  DEF2P 1 6 DFET ! DFET
OUT
  FET1 SPAR
! DFET SPAR
FREQ
  SWEEP 2 24 1
```

Figure 5. Computer model which generates S-parametera for FET device.

The simplified FET model is easily absorbed into the transmission lines, but does not consider feedback capacitance, which is a major contributor to performance degradation at high frequencies. The presumption here is that effective gate and drain capacitances for the realistic modal still allow the desired gate and drain line performance. For some devices this may not be ture, and limited bandwidth may be required by the gain-bandwidth limitations of the matching network or to maintain stability of the amplifier. If this is found to be true, an alternative device or design may be required to achieve the desired performance.

One approach to improving the design is to incorporate dual gate FETs, with the second gate electrically grounded at RF frequencies. This combination behaves as a two-stage cascode device, which exhibits lower equivalent gate and drain capacitances, and thus extra bandwidth. [1] The design approach will demonstrate the use of single gate FETs, then dual gate FETs will be substituted to illustrate the improvement.

Observations

Understanding the factors influencing the performance of the design helps knowing what to expect as the circuit is modeled and analyzed. It also uncovers clues to improving the design. A close look at the theory of distributed amplifiers shows relationships involving time constants at the gate and drain of the FET. [2] These relationships indicate that frequency response of the amplifier is heavily influenced not only by the cutoff frequency of the gate and drain lines, but by the attenuation on the gate line. DC gain, on the other hand, is influenced by the Gm of the FET and attenuation on the drain line. There is also a relationship between optimum gate width and optimum number of FET devices used in the amplifier. [2] This could indicate that there is an optimum total gate periphery for a given distributed amplifier.

The characteristics of the constant-k line deserve some thought also. For instance, the image impedance of the line is resistive below cutoff, and reactive above cutoff. Also, it is possible to maintain a constant cutoff frequency by holding the LC product of the line constant. These facts help in understanding how to tune the amplifier.

Forming the Computer Model

The first step in modeling the amplifier is to determine the equivalent shunt capacitance at the gate and drain of the FET for the desired operating conditions. This is easy to determine if the device is unilateral, or nearly so, since the equivalent capacitances can be read from the model directly.

Most FETs are not unilateral because of the drain-gate feedback capacitance, and in fact this usually causes the device to be conditionally stable. The effective gate and drain capacitances for a non-unilateral device are modified by the "Miller" effect, where the feedback capacitance is reflected into the gate and drain circuits for a particular load.

When the FET is not unconditionally stable, it is a bit tricky since the equivalent capacitances cannot be determined from the simultaneous match conditions. In fact, the amplifier must be designed so that a deliberate mismatch occurs at the gate and drain in order to ensure stable operation. This limits the desired performance of the distributed amplifier since the equivalent capacitances cannot always be totally absorbed into the gate and drain lines.

A look at the general stability of the 250 micron wide FET indicates some caution is in order. The device is conditionally stable at lower frequencies, but resistive terminations lie in the stable region on both the input and output planes. Using the computer to tune a rough matching circuit helps to visualize how the FET responds to various matching elements. Because of the difficulty in matching to the FET, full decade bandwidth will probably not be possible, at least not with good gain flatness.

The tuning procedure allows a rough estimation of the equivalent capacitances at the gate and drain, 0.275 pF and 0.06 pF respectively. If the goal is a 2 to 20 GHz amplifier, the cutoff frequency of the gate and drain lines must be set higher than that, say to 24 GHz.

To make the design simpler, two additional requirements are made. First, the image impedance of the gate and drain lines will be held near 50 ohms to facilitate a broadband match to a standard load.

Second, the series inductance of the lines is held constant, making all the lumped equivalent transmission lines the same impedance and length. This second restriction requires that the capacitances of the lines also be the same, so shunt capacitors of 0.215 pF must be added to the drains of the FETs. The inductance value of the constant-k line calculates to 0.625 nH. The inductors will actually be implemented as electrically short high impedance transmission lines, say 90 ohms, and the capacitors as electrically short low impedance transmission lines, say 50 ohms. Using the equations for a short and open circuited transmission line impedances, the electrical length of the

equivalent transmission lines is found to be 1.4 degrees at 1 GHz for the 50 ohm lines and 2.5 degrees at 1 GHz for the 90 ohm lines. Linecalc (TH) Is used to verify the reliability of the microstrip lines on 4 mil thick GaAs substrate.

The rough design of a complete amplifier can be put together and optimized for the desired performance. Four FETs are arbitrarily included in the circuit. The optimization criteria are chosen to flatten gain to a reasonable value, maintain a match to 50 ohm source and load, and to require gain rolloff and reflection coefficients less than unity above the band of interest. The schematic for the optimized circuit file is shown if Figure 1. The final circuit file description is shown in Figure 6.

```
! Figure 6:  This circuit file models a single gate FET distributed amplifier
! with 4 devices, with device parameters read from file FET250.S2P, 250 micron
    VAR
      L   \ 0.91455        ! length of constant-k half section inductor
      LEN \ 1.30722        ! length of drain capacitor
      Z1  \ 91.05647       ! impedance of constant-k inductance line
      R1  \ 46.59919       ! terminating impedance of constant-k line
    EQN
      LZ = 2 * L
      Z0 = Z1
      R2 = R1
    CKT
      TLIN 1 2 Z^Z1 E^L F=1
      S2PA 2 12 0 FET250
      TLIN 12 22 Z=50 E^LEN F=1
      TLIN 21 22 Z^Z0 E^L F=1
      RES Z1 0 R^R2
      TLIN 2 3 Z^Z1 E^L2 F=1
      S2PA 3 13 0 FET250
      TLIN 13 23 Z=50 E^LEN F=1
      TLIN 22 23 Z^Z0 E^L2 F=1
      TLIN 3 4 Z^Z1 E^L2 F=1
      S2PA 4 14 0 FET250
      TLIN 14 24 Z=50 E^LEN F=1
      TLIN 23 24 Z^Z0 E^L2 F=1
      TLIN 4 5 Z^Z1 E^L2 F=1
      S2PA 5 15 0 FET250
      TLIN 15 25 Z=50 E^LEN F=1
      TLIN 24 25 Z^Z0 E^L2 F=1
      TLIN 5 6 Z^Z1 E^L F=1
      RES 6 0 R^R1
      TLIN 25 26 Z^Z0 E^L F=1
      DEF2P 1 26 AMP
    OUT
      AMP DB[S21] GR1
      AMP DB[S11] GR1A
      AMP DB[S22] GR1A
    FREQ
      SWEEP 2 24 1
    GRID
      GR1 0 10 1
      GR1A -20 0 2
    OPT
    ! in band optimization
      RANGE 2 20
      AMP DB[S11] < -10
      AMP DB[S22] < -10
      AMP DB[S21] = 7
    ! out of band optimization
      RANGE 21 24
      AMP DB[S21] < 7 10
      AMP DB[S11] < 0 10
      AMP DB[S22] < 0 10
```

Figure 6. Final circuit file description.

Plots of the optimized results are shown in Figure 7, and a comparison with 3 and 5 FETs is shown in Figure 8. A comparison with 200 and 300 micron wide FETs shown in Figure 9.

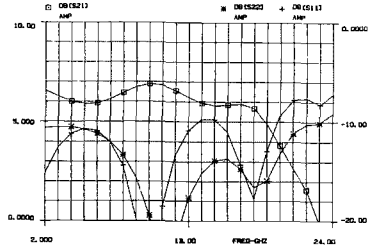


Figure 7. Single gate 2 to 20 GHz, 250 micron design, 4-FET amplifier results

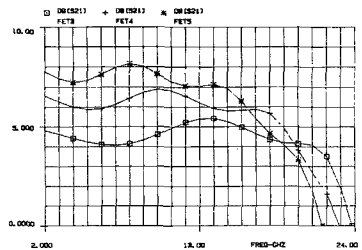


Figure 8. Three-, four-, and five-FET amplifier gain .

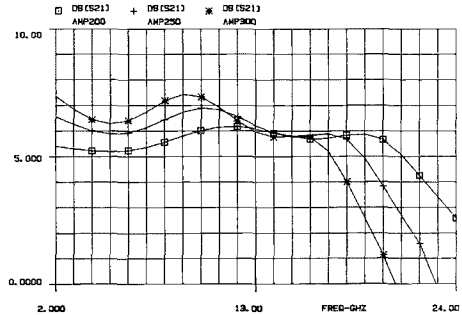


Figure 9. 200, 250, and 300 micron FET amplifier gain.

The overall bandwidth and gain flatness are indeed less than desirable. The total gain is low compared to what would be expected with a narrow band single state design, but this is normal for a distributed amplifier. The narrower bandwidth can be attributed to problems on the gate line. The gain and gain flatness can be attributed to problems on the drain line. There seems to be some tradeoff between improving the gate and drain lines. To achieve more reasonable gain flatness, the bandwidth is reduced to 2 to 14 GHz and the circuit is re-optimized. The results are shown in Figure 10.

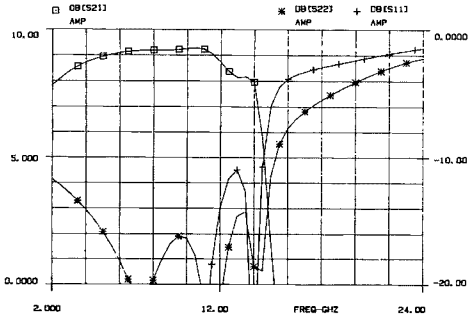


Figure 10. 2 to 14 GHz single gate amplifier results.

In an attempt to improve both the gain and flatness, dual gate FET parameters are used in the design. The dual gate FET also has the advantage of gain control by adjusting the bias voltage on the second gate. The FET parameters are generated from an expansion of the single gate FET model into a two-stage cascode model. The gate width was reduced to 200 microns to make the device more stable. Since the overall gain and bandwidth were much better, the design goals were set to 9 dB gain and 2 to 24 GHz passband. The optimized results are shown in Figure 11.

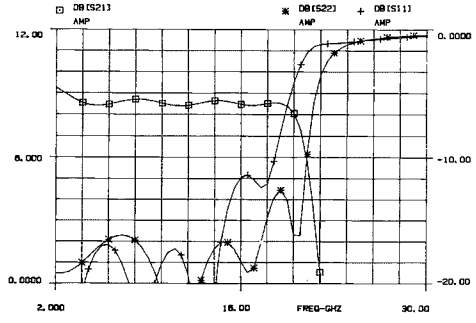


Figure 11. Dual gate amplifier results.

What About Stability

Stability is often a very difficult thing to prove. In order to properly prove stability on the amplifiers designed here, each interface of a FET to the gate and drain lines should be examined to determine the loads that each FET sees looking into the gate and drain lines. These loads can be plotted on the input and output planes for the FET to determine if they lie in stable regions. Looking at the amplifier response, the gain response and reflection coefficients at the input and output seem well-behaved, thus there is not firm reason to expect a near oscillating condition. There would be

cause for worry if there was unusual gain peaking or reflection coefficients greater than 1 at the input or output.

Conclusion

A glimpse has been given into how an engineer can use computer tools to increase the speed of design and quality of circuitry. The techniques shown are applicable to state-of-the-art amplifier designs -- a mere taste of what the powerful tools available in computer-aided design can do for you.

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